



HAL
open science

Early-stage HF-EMC Simulation Analyses of Common-Mode Current in SiC-Based Motor Drive System for Modern Aircraft Applications

Gregory Almeida, Marc Cousineau, Nicolas C. Rouger, Sébastien Serpaud,
Victor Dos Santos, Bernardo Cougo, Davin Guedon, Olivier Crepel, Richard
Perraud

► **To cite this version:**

Gregory Almeida, Marc Cousineau, Nicolas C. Rouger, Sébastien Serpaud, Victor Dos Santos, et al.. Early-stage HF-EMC Simulation Analyses of Common-Mode Current in SiC-Based Motor Drive System for Modern Aircraft Applications. IEEE Transactions on Transportation Electrification, 2023, pp.1-1. 10.1109/TTE.2023.3311621 . hal-04255888

HAL Id: hal-04255888

<https://hal.science/hal-04255888>

Submitted on 24 Oct 2023

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

Early-stage HF-EMC Simulation Analyses of Common-Mode Current in SiC-Based Motor Drive System for Modern Aircraft Applications

Gregory Almeida, *Senior Member, IEEE*, Marc Cousineau, Nicolas Rouger, Sébastien Serpaud, *Member, IEEE*, Victor Dos Santos, Bernardo Cougo, Davin Guedon, Olivier Crepel, and Richard Perraud

Abstract—In modern aircraft applications, an electrical powertrain based on silicon carbide (SiC) modules is a promising technology for achieving commercial roadmap targets. However, the high switching speeds and parasitic elements associated with SiC-based power converters bring up drawbacks in terms of electromagnetic compatibility (EMC). Furthermore, during the early-stage design of a system, the prediction, optimization, and fast simulations to analyze EMC performances are not always easy tasks. It requires accurate models and is still continuously being treated in the literature. This article discusses and highlights the key elements responsible for EMC issues, in a typical common-mode (CM) current signature. A discussion and methodology on how several aspects of EMC, in terms of power energy, can be predicted in advance are also presented. A modeling approach through an improved equivalent CM circuit (ECMC) is introduced, providing satisfactory results and good computational time versus accuracy trade-off, even with ringing effects. The analyses presented here are suitable for EMC pre-compliance tests. Simulation results of a 2-level SiC-MOSFET prototype under development are presented to validate theoretical approaches. Experimental EMC tests in a 50 kW electromechanical chain with 70 kVA SiC-MOSFET prototype are presented for validation purposes.

Index Terms—Electromagnetic Compatibility, Silicon-Carbide, More-Electric Aircraft, Modeling.

I. INTRODUCTION

THE emerging concepts of All-Electric Aircraft [1] and More-Electric Aircraft systems [2] using SiC-based powertrain experience difficult trade-offs and worldwide challenges [3], [4]. For instance, the high switching speed of the latest SiC-based power modules has provided benefits in terms of semiconductor losses and power density [5]. On the other

hand, for each switching transient event experienced at the switching node, a critical CM current is generated and will circulate via parasitic elements. This leads to an increase in conducted emissions and produces a negative EMC impact, as emphasized in [6]. Hence, such interdependence between efficiency and electromagnetic interference (EMI) issues is one of the most essential trade-offs in this area [2], [7], [8].

The power electronic-based motor drive systems used in aircraft applications face challenges due to growing power demand and strict safety and EMC rules. Electric aircraft power systems must work reliably in different conditions, which is a big challenge. As mentioned in [9], the electric and more-electric aircraft industry needs even more powerful and reliable electrical systems than the automotive industry.

Several aspects can contribute to the failure of an EMC compliance test (e.g., constraints to integrate high-temperature decoupling capacitors, very low gate-driver resistances, high parasitic inductance values, simulation models with time-accuracy issues, etc.). Hence, special attention should be paid during the early-stage EMC (pre-compliance stage) analyses. Such investigations are essential to assist design teams, by warning critical points before designing the passive (or active) EMI filters. The literature highlights efforts related to EMC and improvements of fast switching transient issue in [7], [10]–[16]. In summary, most papers can be grouped as: i) switching speeds compensation techniques [11]–[13], [17], [18], ii) ringing mitigation [16], [19], [20], iii) layout rules-of-thumb or techniques to reduce parasitic elements [10], [15], [21], and iv) modeling approaches with good computational-efficiency ratio [22]–[26]. This latter group highlights the attention to be paid to modeling, either for more efficient models in terms of calculation or terms of accuracy.

Accurate models faithful to theoretical studies can help to confidently predict main HF perturbations in such a way that mitigation techniques can be chosen properly. However, making a full system simulation model for time-domain analysis as accurate as possible increases its complexity and vulnerability to modeling errors (losses, for example). As a consequence convergence problems can come up. In addition, prohibitive simulation time (i.e., tens of hours) are also observed. Hence, other approaches i.e. [8], [25], [27], [28], are better options to avoid these problems. Among them, approaches based on common-mode equivalent circuits stand out as suitable and well-accepted in the literature [25], [29], [30]. However, one observes a lack of study in the aircraft domain that clearly

Manuscript received 06 March 2023; revised 21 June 2023; accepted 23 August 2023. These results have been obtained in the framework of the IRT Saint Exupéry's research project OCEANE. Authors acknowledge the financial and in-kind support (background knowledge and services) from the IRT Saint Exupéry's, industrials and academic members as well as the financial support of the French National Research Agency.

G. Almeida, M. Cousineau, and N. Rouger are with the static converters research group of LAPLACE laboratory, Université de Toulouse, LAPLACE, CNRS, UPS, INPT, Toulouse, France (e-mails: gregory.almeida@ieec.org, cousineau@laplace.univ-tlse.fr, rouger@laplace.univ-tlse.fr).

S. Serpaud and B. Cougo are with More Electrical Aircraft (MEA) Department of the French Institute of Technology (IRT Saint-Exupéry), Toulouse, France.

Victor Dos Santos is with the Electronic and Electricity Team of Safran Tech, Magny-Les-Hameaux, France. He is also seconded part time to the MEA Department of IRT Saint-Exupéry, Toulouse, France.

D. Guedon, O. Crepel, and R. Perraud are with Electrification Technologies (XRE) of AIRBUS Central Research and Technology, Toulouse, France.

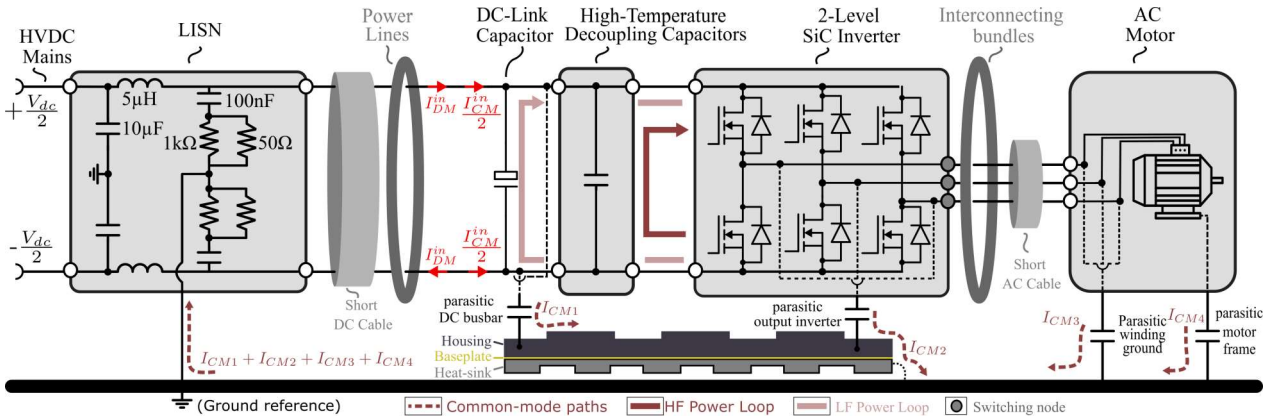


Fig. 1. Studied 3 Φ motor-drive system in EMC pre-compliance stage to analyze conducted EMI emissions issues, according to DO-160 standard.

states a methodology to identify the critical elements involved in a well-defined HF common-mode model, and supported by a set of analyses considering different scenarios.

This paper investigates useful HF-EMC modeling and simulation analyses focused on the CM current spectrum (CMCS) for a typical SiC-MOSFET-based three-phase (3 Φ) motor drive system applied in more-electric aircraft systems, as depicted in Fig. 1. A methodology for extracting essential information (i.e., parasitic elements identification, analysis of high-temperature decoupling capacitors, oscillations characterization, etc.) is proposed. Such a methodology considers a common-mode simplified model which is capable to reproduce the CMCS profile very close to the one obtained by simulating the 3 Φ model (including all elements of the overall systems). Furthermore, the proposed methodology provides faster simulations. Further, focusing on aircraft applications, the issue to integrate high-voltage and high-temperature (e.g., 150-200 $^{\circ}$ C) decoupling capacitors with only low-value capacitors available on the market is highlighted. This work comprises early-stage design studies for a high-power and high-temperature motor control unit (MCU-HT) demonstrator, carried out by an aircraft manufacturer.

The present work is divided as follows: in Section III, a general description of the studied system is presented. Next, the modeling and main equations are introduced to support the capability to predict key EMI effects. In Section IV, an equivalent common-mode model able to reproduce ringing effects is presented. The results, and discussions of this work comprise two scenarios as case studies. The first one considers a module under development and is covered in Section V. The second case covered in section VI considers experimental and simulation results for a 50 kW electromechanical chain system with a 70 kVA SiC-inverter prototype developed at IRT-Saint Exupéry. The DO-160 standard [31] is considered to quantify the failure margin. Finally, conclusions are presented.

II. SYSTEM DESCRIPTION AND EMI BASICS

The system modeling discussed in this work is based on a typical 3 Φ motor drive system, depicted in Fig. 1. Such a system represents a basic setup used in the EMC pre-compliance tests to comply with the DO-160 standard. It is

composed of a line impedance stabilization network (LISN), DC and AC cables, current measurement at DC-side (i.e., power lines), dc-link capacitors, optional high-temperature decoupling capacitors, inverter, current measurement at AC-side (i.e., interconnecting bundles), and AC motor. If short cables are used, a low impact on the common-mode current spectrum (CMCS) is expected [32], [33], thus they can be omitted in the early-stage analysis.

A. EMI source

The main EMI source here is the conducted EMI emission, which is generated mainly due to the switching behavior of the SiC-MOSFET. This is addressed mainly to the high dV/dt (or dI/dt) experienced by the inverter outputs that can propagate through common-mode (CM) and differential-mode (DM) paths. Such transients with considerably high-value parasitic elements will create a critical CM current path.

B. CM and DM Modeling Hypothesis (transfer of mode)

There are cases where the CM and DM spectra may not be fully decoupled, and the phenomenon of transfer of mode may take place. It means that a contribution of the DM current may appear in the CM current, mainly due to a dissymmetry in the propagation path. More details about the transfer of mode can be observed in [34]. However, even if the conducted EMI can be investigated by means of CM and DM circuits (i.e., by superposition principle), in this paper, we assume that the conducted emissions are dominated by CM only. It is shown experimentally at section VI-B the DM/CM influence that confirm this assumption.

C. EMI basics - switching voltage approximation

Once the switching behavior of SiC-MOSFET is the main EMI source, the CM voltage V_{CM} is a function of them. Additionally, V_{CM} can be seen as a piecewise-linear waveform carrying the transient behavior of drain-source voltage V_{ds} at the switching node of each phase. Then, V_{CM} can be assumed as a linear combination of pole-voltages in each phase. This can be easily observed by using linearity, time shifting, and

differentiation properties of the Fourier series from the theory of signals and systems.

In a first approximation, let assume V_{CM} as just a trapezoidal waveform with amplitude $0.5V_{dc}$, duty cycle d , equal rise and fall times $t_r = t_f$, and period $T_s = 1/f_s$. Its corresponding spectrum envelope in the frequency domain is given as

$$|V_{CM}(\omega)| \simeq \underbrace{V_{dc} \cdot d}_{0 \text{ dB/dec}} \cdot \underbrace{\left| \text{Sinc}\left(\frac{\omega T}{2}\right) \right|}_{-20 \text{ dB/dec}} \cdot \underbrace{\left| \text{Sinc}\left(\frac{\omega t_r}{2}\right) \right|}_{-40 \text{ dB/dec}} \quad (1)$$

where $\tau = d \cdot T_s$, $\omega = 2 \cdot \pi \cdot f$, and $\text{Sinc}(x) \triangleq \sin(x)/x$.

Its spectral characteristic has a DC gain and a product of two *Sinc* functions. This spectrum can be seen as a series of linear asymptotes having 0dB/dec, -20dB/dec, and -40dB/dec, respectively. At high frequency, attenuation with a slope at -40dB/dec is obtained after a cut-off frequency dependent on the switching rising and falling times (t_f and t_r). Additionally, the dV/dt are also inversely proportional to switching times as detailed in [35]. Note that some fixed parameters play an important role. Indeed, they will impose critical values that may not be flexible to be attenuated in EMC pre-compliance.

III. MAIN CONTRIBUTORS FOR EMC MODELING

In the early-stage EMC design (i.e., a system without EMI filters), the system of Fig. 1 may reproduce a CMCS signature quite similar to the one indicated in Fig. 2. In such a hypothetical scenario, some critical points associated with resonance peaks can be observed as shown by the circled numbers. To have a better understanding of such a profile, the first step is to analyze it: (i) by using techniques or methodologies based on the theory of signals and systems, (ii) by verifying the origins of peak resonance, and (iii) by finding key elements (or effects) that are contributing to this.

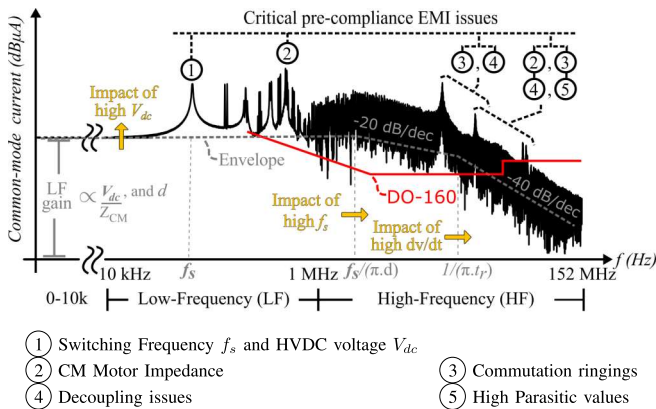


Fig. 2. Hypothetical CMCS of a typical high-power motor drive system for aircraft applications. The red curve depicts CM current I_{CM} limits allowed by the DO-160 standard. Circled numbers are possible contributors to EMI issues. Yellow arrows indicate where high values can have an impact on the CMCS.

In this work, the CMCS is divided into two frequency ranges: i) low-frequency (LF) from 10kHz up to 1MHz, and ii) High-frequency (HF) from 1MHz up to 150MHz. The LF EMC issues can be associated with cable, AC machine LF

characteristics, and PWM strategies. The HF issues can be probably due to some HF machine resonances or ringings inherent from high switching speeds of SiC-MOSFETs where constraints are more critical to be treated in aircraft applications. Based on the example of Fig. 2, the designer teams should be aware of five effects that play an important role in the CMCS profile:

- 1) *Switching frequency f_s and HVDC voltage V_{dc}* : The CMCS is associated with CM voltage and CM impedance such that $I_{CM} \simeq V_{CM}/Z_{CM}$. From (1), note that f_s and V_{dc} impose a high LF gain (i.e., $\propto |V_{dc} \cdot d|$) and move the first corner frequency ($f_{c\tau} = f_s/(\pi \cdot d)$) of the CMCS to the right side, increasing the bandwidth of the conducted emission.
- 2) *CM motor impedance*: The capacitive motor impedance (e.g., stray capacitance from stator to ground) providing a path for the CM current circulation is a common issue and can be verified through simulations via impedance-frequency characteristic analysis.
- 3) *Ringings on switching nodes*: The resonance peaks are due to the high switching speeds of the SiC-MOSFET power module under the presence of local parasitic components involved in the power loop. High parasitic values together with switching speeds can impose critical ringings. Indeed, switching speeds dI/dt and dV/dt associated with turn-off and turn-on, respectively, have a strong impact on the magnitude of the HF spectral lines (HF envelope). This will be more evident under high asymmetries scenarios. Also, external gate resistances can slow down the switching transients at the cost of increasing the switching losses as detailed in [13], [35].
- 4) *Decoupling issues*: The sizing design and placement of high-voltage and high-temperature decoupling capacitors on the board have a strong impact on the reduction of parasitic components and resonances. Their inappropriate sizing can lead to their inefficiency. In addition, if only low-value commercialized capacitors are available, another EMC issue can come into account.
- 5) *Parasitic values*: Depending on the geometry and routing layout of the power module's internal board, high-value parasitic components are identified and their effects on HF are observed, allowing optimization measures to be taken.

In this work, the HF-EMC coupling paths will be mainly observed from parasitic elements in two types: *i) Capacitive coupling* - associated with metallic structure references, internal SiC-MOSFET structure (dielectric and junction-capacitances), heat-sink, ground-winding motor connections, which is responsible for the common-mode current flow and/or *ii) Inductive coupling* - associated with PCB traces, busbar, and/or terminals involved in the power loop area of the switching cells responsible for very HF radiated emission.

Limited and low values for high-temperature capacitors available on the market may limit the decoupling factor and even the choice of using an arrangement with a series-parallel connection may be unfeasible. This way, when high-temperature decoupling capacitors are considered, two loops

should be considered: i) HF power loop, and ii) LF power loop, as it can be seen in Fig. 1. Some HF-EMC performances can be deduced based on a commutation cell (C-cell) analysis described next.

A. Analysis Based on the Commutation Cell (C-cell)

From the EMC analysis point of view, in a typical motor drive system, as shown in Fig. 1, each pole-voltage commutates between $\pm 0.5V_{dc}$ in a much shorter time compared to the AC motor winding current time constant, and also than the pulse-width modulation (PWM) period, as experimentally observed in [36]. Indeed, during the switching transients, the motor current magnitude should barely change compared to the changes in pole-voltage and HF CM current magnitude. Therefore, during each PWM switching period, the magnitude of AC motor current can be approximated by a constant current source with amplitude equal to the average value of the 3 Φ -system current. Taking that into account, the C-cell shown in Fig. 3 can be considered to provide a good approximation for the HF-EMC analysis.

The main parasitic elements of the C-cell are highlighted in Fig. 3. Such a structure can be seen as a fourth-order circuit if the parasitic elements of the "busbar", "high-temperature decoupling capacitors" and "SiC-MOSFET with N -dies in parallel" are considered. Therefore, it should be noted that, for a step transient response, there is basically a cascade of two resonant circuits that will interact with each other. The main purpose of the high-temperature decoupling capacitors is to drastically reduce the influence of the parasitic inductance L_p responsible for the overvoltage appearing across the switching nodes. For that reason, they are placed as close as possible to the C-cell. Then, if their values are high enough, the fourth-order system can be approximated by a second-order circuit.

In this work, the system under development (case study 1) discussed in Section V is being designed such C_{wg} , the motor-ground parasitic capacitance, can be considered with a higher value than C_p , the busbar parasitic capacitance, and C_{ih} , the inverter-heatsink parasitic capacitance, respectively (i.e., $C_{wg} \gg C_{ih} \gg C_p$). However, there may exist other

cases in which the parasitic capacitances associated with the heatsink and busbar may not be neglected as it is treated in case study 2, briefly discussed in section VI.

From this equivalent circuit, it is possible to extract important insights in terms of HF-EMI problems:

(i) The fourth-order system may produce two oscillating signals' superposition. Hence, the switching node voltage V_{ds} can be approximated by a trapezoidal waveform with two sinusoidal damped signals present at each switching transient. Details on the analytical approach are found in [20].

(ii) Both turn-on (TON) and turn-off (TOFF) events may induce ringing involving parasitic inductance and capacitance within the power loop [13]. However, for SiC-MOSFET switching under high current, the TOFF event (implying transistor overvoltage due to the parasitic inductance of the power loop) may be more representative in terms of EMI issues than the TON event (which implies transistor overcurrent) [16].

When the low-side (LS) SiC-MOSFET arrives at the end of the TOFF and high-side (HS) SiC-MOSFET is OFF, the C-cell circuit of Fig. 3 can be simplified into an equivalent circuit as shown in Fig. 4, leading to an analysis in the Laplace domain.

4th-order frequency analysis at the end of TOFF:

Considering a positive current flowing into the switching node, the LS TOFF equivalent impedance characteristic circuit is considered and shown in Fig. 4. Note that internal parasitic elements of high-temperature decoupling capacitors were not considered for simplification purposes which will give already a good amount of insights in terms of EMC analysis.

Parasitic capacitances C_{gs}^{HL} and C_{gd}^{LH} can be neglected in a first approach since their values do not imply a strong impact if compared to the $C_{oss}^{f(V)}$ value. The equivalent circuit of Fig. 4 is useful to extract and predict at which frequency the ringing will occur.

In the Laplace-domain, one can observe that the impedance $Z_t(s)$ seen by this commutation process and their resonance frequencies can be respectively approximated as

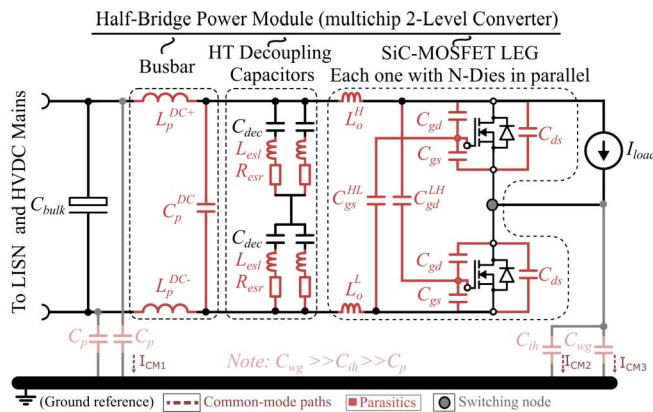


Fig. 3. Commutation cell (C-cell) circuit with parasitic elements. The three blocks highlighted with dashed lines are: busbar, high-temperature decoupling capacitors and SiC-MOSFET leg with N -dies in parallel.

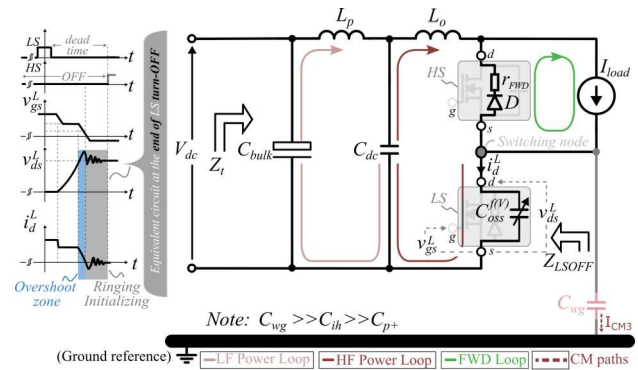


Fig. 4. Equivalent circuit at the end of the turn-off (TOFF) event of the low-side (LS) MOSFET, where $L_p = L_p^{DC+} + L_p^{DC-}$, $C_{dc} = C_{dec} + C_p$, $L_o = L_o^H + L_o^L$, $C_{oss}^{f(V)} = C_{gd} + C_{gs}$ as a function of V_{ds} , and $C_{bulk} \gg C_{dc}$. Z_t is the total impedance seen by the circuit input circuit, and Z_{LSOFF} is the impedance seen across the LS MOSFET terminals.

$$Z_t(s) = \frac{s^4 k_2 + s^2 k_1 + 1}{s^3 (C_{oss}^{f(V)} C_{dc} L_o) + s (C_{oss}^{f(V)} + C_{dc})} \quad (2)$$

$$\text{and } f_{osc1,2} = \frac{1}{4\pi} (\sqrt{\zeta} \pm \sqrt{\gamma}), \quad (3)$$

where, $\zeta = \frac{k_1}{k_2} + 2\sqrt{\frac{1}{k_2}}$, $\gamma = \frac{k_1}{k_2} - 2\sqrt{\frac{1}{k_2}}$, with $k_1 = C_{oss}^{f(V)} L_o + C_{oss}^{f(V)} L_p + C_{dc} L_p$, and $k_2 = C_{oss}^{f(V)} L_o C_{dc} L_p$.

Also, note that the $C_{oss}^{f(V)}$ value considered in this case (i.e., at the end of TOFF) is the one obtained at high-voltage from the non-linear AC capacitance characteristic of the transistor.

Ringling and duty cycle relationship:

The ringling phenomenon of Fig. 4 will be more evident for small duty-cycle cases (i.e., $d \leq 10\%$), as detailed in [37].

B. Motor capacitive coupling and higher-order circuit

When the AC motor is coupled with the C-cell, the current source must be replaced by an RLC-lumped parameter HF-model. This way, in HF Zone, any value close to a few nano Farad for parasitic capacitances between the switching node and the ground (e.g. C_{wg}) can have a strong impact and lead to failing in EMI compliance. Such a capacitive coupling may result in additional ringling in the analyses.

The additional ringling may increase the order of the system (from 4th- up to 8th-order), leading to analyses even more complex in time- or Laplace-domain. Indeed, as similarly discussed in [38], for HF-range, it becomes more difficult to obtain a general mathematical expression associating all elements impacting in the conducted disturbances and the EMI source. However, if the principle of superposition cannot be used in this case, a methodology based on the impedance-frequency characteristic curve analysis of the system can be considered. More details about this can be found in [36].

C. Switching Considerations for 3Φ-PWM Inverter

The three-phase 2-level SiC Inverter has eight switching states (2^3) in its PWM operation. Among them, six perform active vectors ([100],[010],[001],[110],[101],[001]) and two perform zero vectors ([000],[111]). Active vectors impose common-mode voltage V_{cm} equals to $\pm V_{dc}/6$ whereas the zero vectors impose $\pm V_{dc}/2$. This can be verified by considering further equation 4.

In terms of EMI, the 3Φ-PWM pattern will impose similar switching transients. Indeed, the disturbance current path generated by the CM interference sources of the three-leg-based inverter is symmetrical in terms of CM paths [38]. Then, any switching states can be considered for a study case. The relevant aspect here to keep in mind is that for each period of the PWM, there will always be three legs (one for each phase) excited, enabling circulating paths of CM currents with identical behavior. This can be assumed for a three-phase symmetrical/balanced case.

IV. EQUIVALENT COMMON-MODE CIRCUIT (ECMC)

Compared to some existing solutions in the literature [29], an improved ECMC is presented in Fig. 5(a). The ECMC is useful for two study cases discussed in this work. To provide accurate results, it considers the ringling effects due to TON/TOFF transients. The ECMC model includes the most important elements in terms of EMI represented by the studied system (i.e., CM motor-side, CM LISN, and CM Voltage source). The CM voltage (CMV) source represents the contribution of the three C-cells. It includes the ringling generation, discussed next.

A. CMV implementation with ringling

The CMV with ringling generation is implemented as shown in Fig. 5(b). The ringling voltage signal V_{ring} is added to the ideal modulated signals for each phase (i.e., V_u , V_v , and V_w). For example, phase-U voltage $V_{ph,u}$ will be composed of two superimposed signals: i) the ringling from V_{ring} and the ideal PWM modulated signal from V_u . This way, the CM voltage V_{CM} can be obtained from this association as well as considering homopolar (i.e., zero-sequence component) voltage generation from Park transformation, defined by

$$V_{CM} = \frac{V_{ph,u} + V_{ph,v} + V_{ph,w}}{3} \quad (4)$$

The ringling effects in the disturbance source (i.e., V_{CM}) were emulated by adding a stimulus during each switching transient in a simulation model, as shown in Fig. 5(b). In a SPICE simulator such as LTspice, to guarantee that the ringlings will be synchronized with each switching transients, the trigger function can be used.

B. Overshoot (Δ_V) and Switching Speeds (dV/dt) Implementations

The ringling carries important information associated with overshoot (Δ_V) and it can be implemented with a combination of the superimposed damped sinusoidal waveforms as illustrated in Fig. 5(c). To generate the PWM voltages properly as well as avoid convergence issues, switching speeds must be considered. In the SPICE simulation environment, one way to generate such a waveform chosen in this work is by using dependant voltage sources by considering the hyperbolic tangent function (i.e., $\tanh(x)$). Such implementation provides smooth transitions carrying the information of dV/dt in voltage transient implementation (or dI/dt if the current transient is implemented) and can be useful for a more accurate approximation. Note from Fig. 5(d) that parameter $g = f(dV/dt)$.

C. Considerations about PWM

In this work, the PWM implementation is based on the conventional sinusoidal PWM (SPWM) approach [39]. It is worth noting that, other PWM strategies or converter topologies can be considered focusing on CM voltage reduction, to evaluate their impact on EMC in the HF range, [40]–[42].

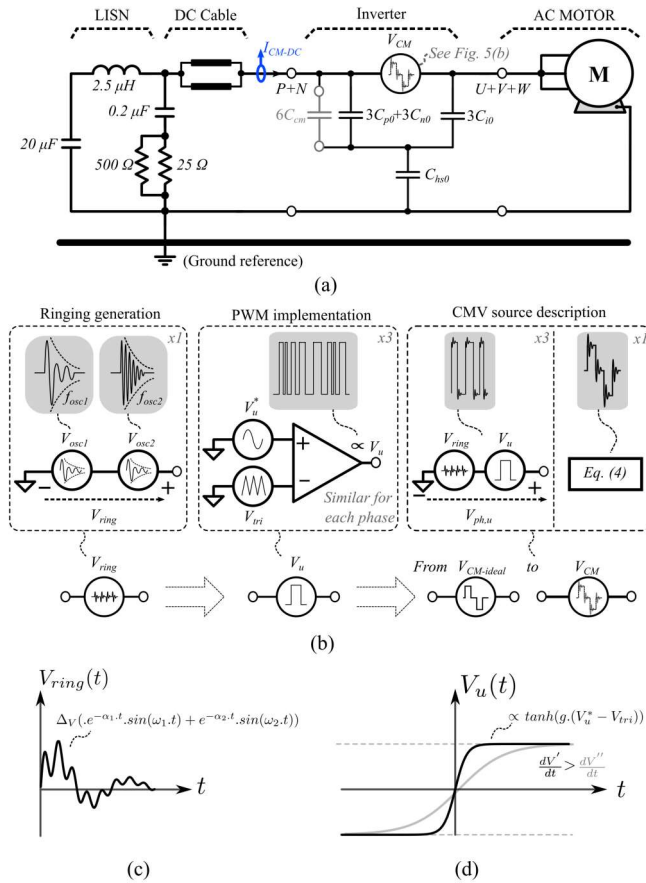


Fig. 5. Proposed equivalent common-mode circuit (ECMC). (a) Circuit. (b) Description of implemented blocks. (c) An example of V_{ring} signal with two superimposed damped sinusoidal carrying overshoot information and oscillation frequencies. (d) An example of V_u signal carrying switching speed informations.

D. Impact of parasitic capacitances coupled with inverter

The additional ringing may occur when the AC motor model is coupled. This will depend on values of parasitic elements, mainly stator-winding capacitance C_{wg} . To emulate this, additional sources V_{osc3} , and V_{osc4} can be added and series-connected in the ringing generation block of Fig. 5(b). Moreover, optimized designs for the cooling system considering the material/shape/area/geometry of baseplate (BP) and/or heatsink (e.g. the thickness/permissivity of the thermal interface material or TIM), may help to reduce the impact of parasitic capacitances C_{p0} , C_{n0} , C_{i0} , C_{hs0} compared to C_{wg} . Note that part of these capacities can be strongly impacted by the implementation of the converter on the vehicle, thus increasing the difficulty in estimating the value of these capacities.

E. Impact of Common-mode filtering capacitance C_{cm}

Common-mode capacitors C_{cm} , highlighted as grey in Fig. 5(a), can be intentionally included in order to attenuate/mitigate CM issues.

The theoretical approaches, expectations, and modeling considerations are verified for early-stage HF-EMC analyses in two studies of cases, as discussed next.

V. CASE STUDY 1 (SYSTEM UNDER DEVELOPMENT)

The under-development module is based on SiC-MOSFETs with 10 dies in parallel for each MOSFET and body-diode. The studied system was implemented and simulated with LTspice and MATLAB[®]. Two sets of simulation results are presented next.

A. Simulation Analysis: C-cell (10-Dies in parallel per switch)

The analysis presented here concerns the commutation process of a C-cell half-bridge. It emulates the switching transient in phase-U of the 3Φ-system, under a given current level. Such a current level is the value obtained when their corresponding modulating signal is close to its maximum/minimum value. The LS MOSFET switching is then considered assuming the current direction as the one shown in Fig. 4. In terms of power scaling and modularity requirements, figures of merits concerning high current and high power capability are effectively achieved by considering the multi-chip (N -dies in parallel) operation design for the half-bridge power module. Each SiC-MOSFET has 10 bare dies connected in parallel.

Table I summarizes the main parameters and specifications for this first set of results. The V_{dc} is rated as 800 V and it corresponds to a standard and trend value for transportation and electrification applications. The nonlinearities of SiC-MOSFET parasitic capacitances (e.g., C_{gd} , C_{gs} , C_{ds}) were implemented intrinsically from LTspice by means of VDMOS model. For instance, $C_{gd} = f(\tanh(V_{gd}))$ if $V_{gd} > 0$ or $C_{gd} = f(\arctan(V_{gd}))$ if $V_{gd} < 0$. For more details, see [43]. The value of C_p^{dc} is directly proportional to the physical dimensions of the busbar and to the permittivity of the dielectric, and inversely proportional to the dielectric thickness. Equations to estimate them can be found in [44].

TABLE I
PARAMETERS FOR SIMULATION RESULTS WITH C-CELL.

General parameters		
Parameters	Value	Description
f_{sw}	50 kHz	Switching frequency
d	5 %	Minimum duty cycle
I_{load}	150 A	RMS Load current
V_{dc}	800 V	HVDC DC-link voltage
C_{dec}	2.2 nF	High-temperature decoupling capacitors
$V_{gs}^+ V_{gs}^-$	+22 V -5 V	Gate driver voltages
$R_{g,on} R_{g,off}$	1 Ω 3.3 Ω	External gate resistors
Parasitics		
Parameters	Value	Description
$L_p^{dc+} L_p^{dc-}$	16.05 nH 16.05 nH	Busbar inductance
C_p^{dc}	76 pF	Busbar capacitance
N	10	Dies-count per MOSFET
$L_{o}^{HL} L_{o}^{LL}$	38.15 nH 32.10 nH	Inductance (dies 1-10)
$C_{gs}^{HL} C_{gs}^{LL}$	1.36 pF 0.12 pF	Capacitance (dies 1-10)
C_{gs}, C_{gd}, C_{ds}	$f(V)$ Non-linear*	Junction capacitances

*all-inclusive values from VDMOS MOSFET model at LTspice.

Fig. 6(a) shows simulation results of C-cell during the commutation process. Note that the V_{ds} at LS MOSFET has a higher resonance at the turn-off (TOFF) compared to the turn-on (TON) event. Further, the two superimposed damped and sinusoidal signals previously described are observed with

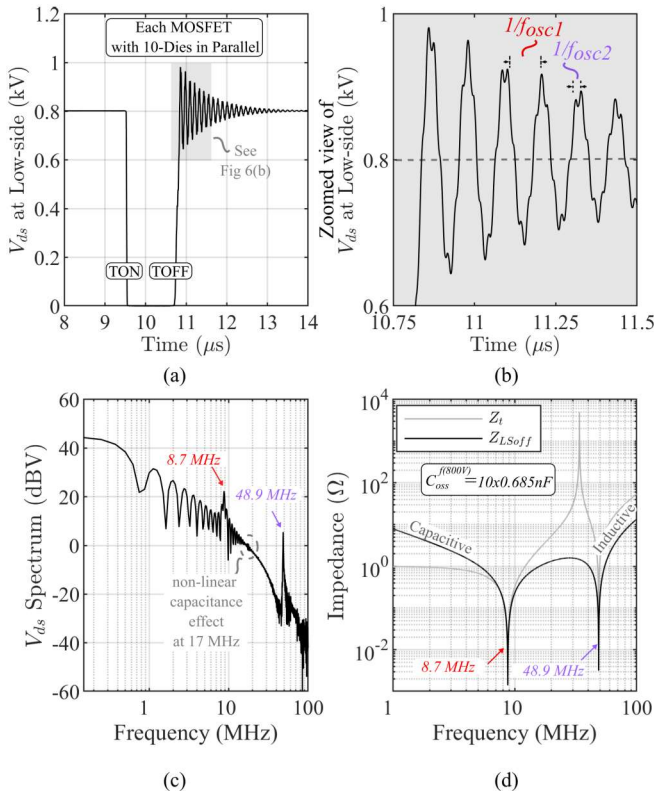


Fig. 6. Simulation result. (a) Ringing analysis at LS V_{ds} with C-cell. (b) Zoom on the beginning of TOFF oscillation. (c) FFT of V_{ds} . (d) Impedance-frequency characteristic curve analysis based on circuit of Fig. 4.

two different frequencies (i.e., f_{osc1} , and f_{osc2}), as shown Fig. 6(b). In addition, from the spectrum curve of Fig. 6(c), a third frequency f_{osc3} at 17 MHz appears, which is due to non-linear capacitance.

Estimation validation: To validate the theoretical estimations, a frequency-domain analysis is considered. From V_{ds} spectrum of Fig. 6(c), which is produced by the FFT of the time-domain simulation presented in Fig. 6(a), or by using equation (3), one can compute the two oscillation frequency values. The theoretical values are very close to the ones observed in simulations as summarized in Table II (the difference between them is less than 1.5 %).

TABLE II
COMPARISON OF RINGING FREQUENCIES.

Values comparison from theoretical and simulation estimations		
Variable	Value from Eq. (3)	Value from Fig. 6(c)
f_{osc1}	8.8 MHz	8.7 MHz
f_{osc2}	49.5 MHz	48.9 MHz

Impedance-frequency analysis: Another way to determine the ringing positions can be done differently from the explanation in the previous paragraph (i.e., not based on Fig. 6(a)-(c)). Alternatively, we can have the same result with simulations based on the impedance-frequency study (i.e., small-signal simulation in frequency domain). It performs an AC simulation analysis of the equivalent circuit depicted in Fig. 4. The corresponding simulation result is shown in Fig.

6(d).

B. Simulation Analysis: 3 Φ motor drive system (60-Dies)

This set of simulations takes into account the original and complete model (OCM) of 3 Φ system of Fig. 1. The simulated OCM has a 3 Φ half-bridge power module with 60 SiC-MOSFET dies (i.e., 20 dies connected in parallel per phase, with 10 for the HS and 10 for the LS). Table III presents the main parameters considered for this set of simulations. Two analyses are performed: 1) Accuracy comparison between OCM and ECMC models, 2) impact evaluation of the key parasitics in the CMCS before and after optimization, as discussed next.

OCM and ECMC model accuracy comparison:

The OCM model considers a full description of the system at the transistor level as depicted in Fig. 7 whereas the ECMC is based on the equivalent common-mode circuit of Fig. 5. Thus, OCM is the complete model from the bottom-up modeling approach whereas ECMC is a simplified model from the black-box modeling approach.

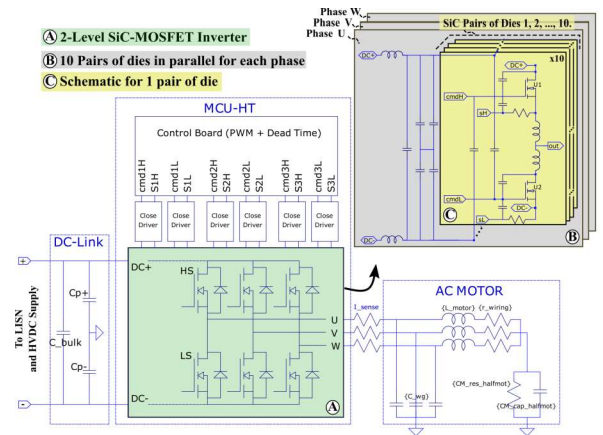


Fig. 7. Parts of LTspice schematic for OCM representing the whole 3 Φ -system. Main parameters are listed in Table III.

Fig. 8 shows the comparison of simulations using both models in which the AC motor equivalent circuit is considered. These simulations show that the approach using the ECMC model (with fitting adjustments) is capable to reproduce with accuracy, in a few tens of seconds (since it is based on simplified circuits with reduced elements count), a result very similar to the one obtained with the complete system model (OCM), requiring hours of simulation time since it uses several elements (including their non-linearities) several switching transients.

Note that four HF-resonance peaks are observed with their respective oscillating frequencies noted f_{osc1} , f_{osc2} , f_{osc3} , and f_{osc4} . This is typically the behavior of an 8th-order system in this frequency range. The four oscillating frequencies highlighted in Fig. 8 can be interpreted as follows:

f_{osc1} and f_{osc2} : These frequencies are correlated together. They are due to the resonances involved by the parasitic components present at the end of TOFF in the SiC-MOSFET. Note that they are exactly the same as the ones presented in

TABLE III
SIMULATION PARAMETERS FOR 3 Φ MOTOR DRIVE SYSTEM. OTHER PARAMETERS NOT LISTED HERE ARE SIMILAR AS IN TABLE I

AC Motor (rated at 100 kW 150 A RMS)			2-Level SiC MOSFET Inverter (continuation)		
Parameters	Value	Description	Parameters	Value	Description
f_o	800 Hz	Output frequency of the motor	$L_{o3,8}^H$ $L_{o3,8}^L$	36.37 nH 32.09 nH	Inductance (dies 3 and 8)
L_{ph} R_{ph}	175 μ H 1.45 Ω	Phase Inductance and resistance	$L_{o4,7}^H$ $L_{o4,7}^L$	35.76 nH 32.38 nH	Inductance (dies 4 and 7)
C_{wg} C_{hm}	1.2 nF 3.6 nF	Motor-ground capacitances	$L_{o5,6}^H$ $L_{o5,6}^L$	35.23 nH 32.78 nH	Inductance (dies 5 and 6)
2-Level SiC MOSFET Inverter (rated at 1.2 kV)			Driver and other specifications		
Parameters	Value	Description	Parameters	Value	Description
PWM m	SPWM 0.95	PWM method and mod. index	DT	200 ns	Dead time
MOSFETs count	60	10 pairs of dies HS-LS per phase	R_{gon}	1.0 Ω	Ext. TON gate resistance
$L_{o1,10}^H$ $L_{o1,10}^L$	38.15 nH 32.10 nH	Inductance (dies 1 and 10)	R_{goff}	3.3 Ω	Ext. TOFF gate resistance
$L_{o2,9}^H$ $L_{o2,9}^L$	37.17 nH 32.04 nH	Inductance (dies 2 and 9)	D_{stk}	D0452A	Schottky diode model

subsection V-A. The commutation loop involves $L_{o1-5,10-6}^H$, $L_{o1-5,10-6}^L$, L_p^{dc+} , L_p^{dc-} , C_{dec} and $C_{oss}^{f(0.8kV)}$. The asymmetry between the values of each parasitic inductance indicated in Table III (i.e., $L_{o1-5,10-6}^H$, $L_{o1-5,10-6}^L$) contributes to the appearance of some asymmetries and sub-harmonics around f_{osc2} .

f_{osc3} : The spectral line at this frequency is due to the effect of the non-linearity of the output capacitance $C_{oss}^{f(V)}$ during the TOFF which is also associated with the zero-bias body diode junction capacitance C_{j0} . This event is even worst under high voltage overshoot when the HS and the LS operate in complementary modes (e.g., DC-AC). More details about this phenomenon can be seen in Fig. 8 of [45].

f_{osc4} : This HF spectral line is mainly due to the capacitance C_{wg} which resonates with other parasitic elements. The commutation loop involves basically L_p^{dc+} , L_p^{dc-} , $L_{o1-5,10-6}^H$, $L_{o1-5,10-6}^L$, C_{dec} and C_{wg} . To identify in more detail the root-causes of the HF-EMC issues related to the frequencies f_{osc3} and f_{osc4} , it is suggested to perform impedance-frequency simulation-based analysis.

Extraction and Impact of Parasitic elements:

The values of the parasitic components associated with

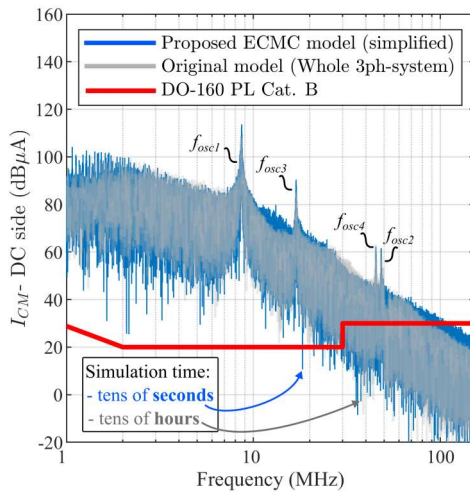


Fig. 8. Simulation result. Models comparison between The OCM (i.e., with 60 SiC MOSFETS) and proposed EMC. The original OCM is the complete model from the bottom-up modeling approach. The proposed EMC is a simplified model from the black-box modeling approach.

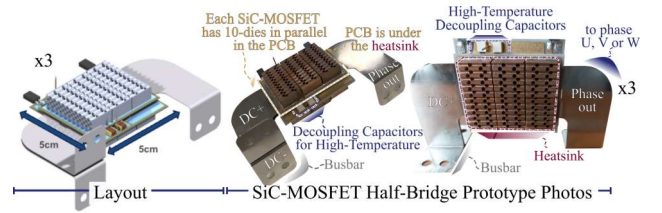


Fig. 9. Layout and prototype photos of 2-level SiC-MOSFET Module.

the busbar and the PCB layout of the board involving the half-bridge power modules have a strong impact on several ringings during a switching event. They must be considered in the early-stage of the EMC study. To provide some rules-of-thumb, an overview of the multichip layout is presented next.

i) Multichip power module prototype (preliminary version):

Fig. 9 presents the layout and photos of a one-phase sample for a multichip 2-level SiC-MOSFET half-bridge. For a 3 Φ converter, three identical modules are used. Such a preliminary layout version is very useful to determine the first issues associated with overestimated parasitic components and not-optimized routing methods as well as geometry and other coupling effects (e.g., busbar effect). Then this part must be carefully revised during the early-stage of the design process. The parasitic values were extracted by using Ansys Q3D considering the worst cases.

ii) Impact of parasitic component values:

To evaluate the influence and impact of parasitic values in the common-mode current spectrum (CMCS), a simulation was performed considering the worst case and an optimized case, see Fig. 10. The worst case considers high parasitic values as listed in Table III, whereas an optimized case considers parasitic inductance values reduced by a factor of ten. It is worth noting that initially high values of the worst case were extracted considering connections without the busbar effect. The optimized case is expected since this busbar effect and reduction of parasitic MOSFET inductance are now considered. Note that the HF ringings are drastically reduced, which simplifies the EMI filter design.

VI. CASE STUDY 2 (TESTS WITH A 50 kW SYSTEM)

This scenario considers an experimental EMC test with a SiC-based 70 kVA prototype designed and mounted at IRT-Saint Exupery Laboratory. Fig. 11 shows the main parts of

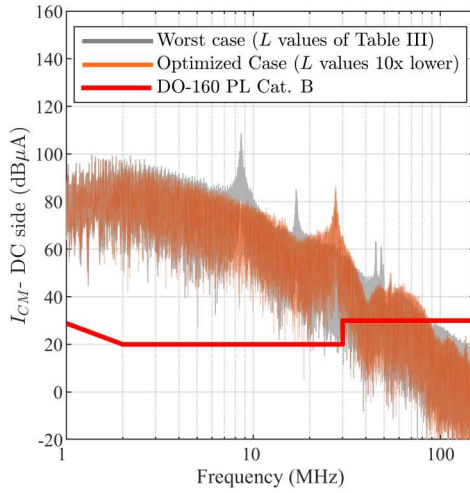


Fig. 10. Simulation result. Analysis of parasitic elements influence in CMCS.

such a prototype. The converter overview in Fig. 11(a) includes three SiC-MOSFET half-bridges modules commercialized by Wolfspeed (HT3201-RV-B/CAS325M12HM2), sensors boards, optical interface to PWM and conditioning signals, heat-sink, and PCB board with filtering capacitors. Such a board was designed namely to include decoupling DM and CM filtering capacitors, see Fig. 11(b). More details can be found in [46]. Fig. 11(c) shows an external overview for one half-bridge module whereas the internal view can be seen in Fig. 11(d). The internal design allows us to observe that it has seven dies SiC-MOSFETs (Gen2 CPM2-1200-0025B) and six SiC Schottky Barrier Diodes (SiC SBDs CPW5-1200-Z050B) per switch position.

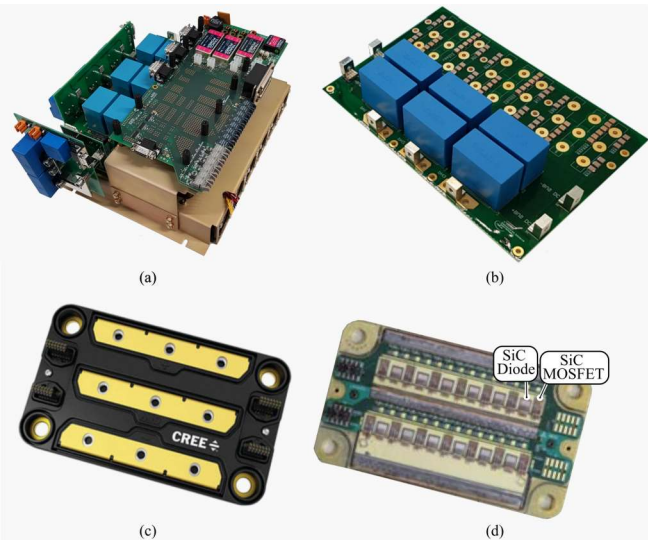


Fig. 11. 70 kVA prototype designed at IRT-Saint Exupery. (a) Overview. (b) PCB with Decoupling DM and CM capacitors. (c) Half-bridge module HT3201-RV-B from Wolfspeed. (d) De-capsulated top view (adapted from [47]).

The 70 kVA SiC converter is used in a 50 kW electromechanical chain. This setup is commonly used to perform EMC compliance tests accordingly to aircraft standards (e.g., DO-



Fig. 12. Overview of the experimental setup for EMC tests.

TABLE IV
PARAMETERS FOR EXPERIMENTAL TESTS.

General parameters		
Parameters	Value	Description
f_{sw}	15 kHz	Switching frequency
V_{dc}	540 V	HVDC DC-link voltage
f_o	533.33 Hz	Machine frequency
n	8,000 rpm	Machine speed
T	40 N.m	Machine Torque
C_{bulk}	6x20 μF	DC-link capacitance
C_{dm}	12x100 nF	DM filtering capacitors per phase
C_{cm}	2x6x1 nF	CM filtering capacitors per phase
$V_{gs}^+ V_{gs}^-$	+18 V -5 V	Gate driver voltages
N_{MOSFET}	7	MOSFET Dies per switch
N_{SBD}	6	SBD Dies per switch

160), seen Fig. 12. The main parameters considered for the experimental EMC tests are summarized in Table IV. The experimental data is shown in oscillogram form (i.e., points of the oscilloscope and/or EMI receiver have been saved and plotted through MATLAB).

A. Electromechanical chain characterization

The characterization of the chain was made through several impedance measurements (Z_{meas}) of each part. The goal is to build behavioral circuit-type models to be simulated at LTspice. The lumped equivalent circuit for characteristic impedances (CM and DM) are fitted according to experimental measurements obtained via an impedance analyzer (Keysight E4990A). Then, the following impedance measurements are obtained: $Z_{LISN}(f)$, $Z_{cable-dc}(f)$, $Z_{inverter}(f)$, $Z_{motor}(f)$. For instance, Fig. 13 shows that the simulated model for the AC machine has a good correlation with the impedance characterized. Fig. 14 shows the comparison between simulation and measurements in order to prove that the DC-

cable topology used in the simulated model is well-fitted with impedance measurements.

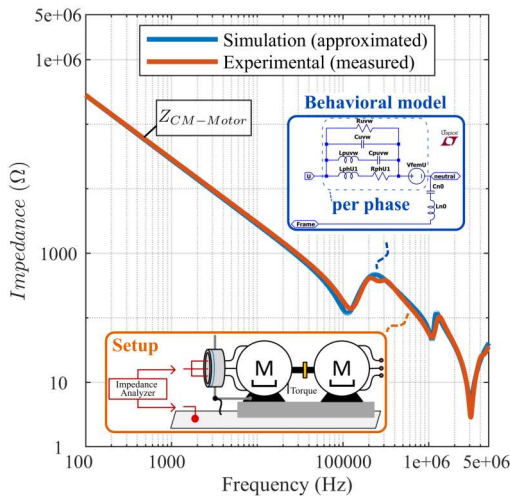


Fig. 13. Experimental result. CM Impedance measurement of the AC motor (Z_{motor}). Comparison between experimental and simulation results.

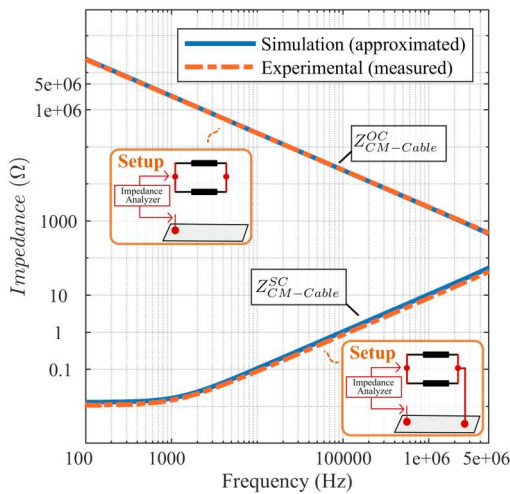


Fig. 14. Experimental result. CM Impedance measurement of the DC cable (Z_{cable}). Comparison between experimental and simulation results for two setups of configurations (i.e., short-circuit $Z_{CM-Cable}^{SC}$ and Open-circuit $Z_{CM-Cable}^{OC}$).

B. Dominant Mode Analysis

The model hypothesis we considered for CM currents is based on the assumption that all CM currents are exclusively due to an EMI source dominated by CM noise. However, it is necessary to question possible mode transfers (in this case, DM \rightarrow CM) that may make the model less relevant, and if CM current is greater than DM current. The CM and DM can be observed by measuring the currents at the input of equipment terminals. In other words, the currents are measured at the DC-

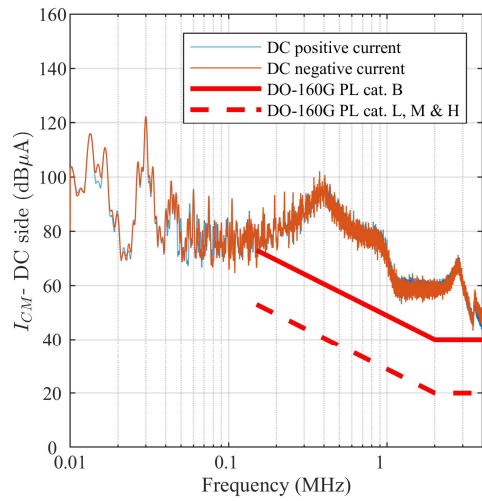


Fig. 15. Experimental result. Mode transfer analysis. Comparison of the DC(+) and DC(-) currents at the DC-side.

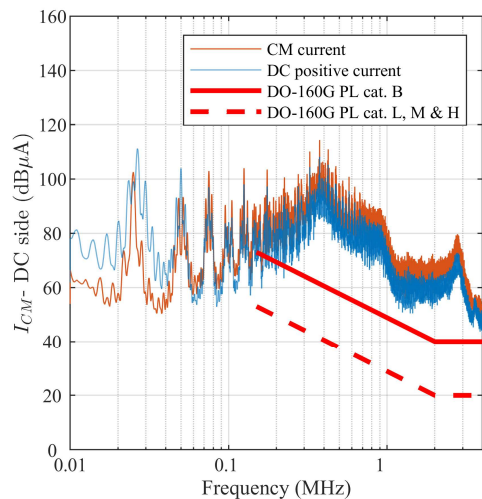


Fig. 16. Experimental result. Dominant mode on the high-frequency range. Comparison of the DC(+) current and CM current at the DC-side.

side named Power lines (PL) in Fig. 1. More details about this methodology can be found in [28].

Fig. 15 shows an experimental analysis to evaluate any modes of transfer. As a result, it can be seen that mode transfers become negligible at the observed sensitivity frequencies. Indeed, it can be seen that the spectrum of measured currents of Power Lines currents at DC+ and DC- of schematic in Fig. 1 are virtually the same, which means that the system does not present asymmetries. Finally, Fig. 16 shows an experimental analysis to evaluate the dominant mode on the studied frequency range. It can be seen by comparing the DC+ current, which is equal to $i_{DC+} = i_{DM} + \frac{i_{CM}}{2}$, to the CM current that the CM is higher in the entire frequency range of interest.

C. Comparison of Experimental with Simulation Results (CM voltage)

Fig. 17 shows a comparison of CM voltage, obtained experimentally, with CM voltage obtained from simulation by using the ECMC model. Some essential information such as switching speed dV/dt and critical oscillations were considered to improve the accuracy. For this, dV/dt and overshoot are collected for each commutation of an entire period of the output current. An algorithm based on linear interpolation presented in [8] was considered based on experimental results. The higher switching speed computed is around 15 V/ns. The overshoots are observed as well, the highest also close to 336 V (from 270 V). Thanks to DM and CM capacitors connected externally in the prototype, relatively low values of overshoots and ringings reductions are observed in the experimental tests. Note that the result of the simulation model is representative, providing satisfactory performance of the real system.

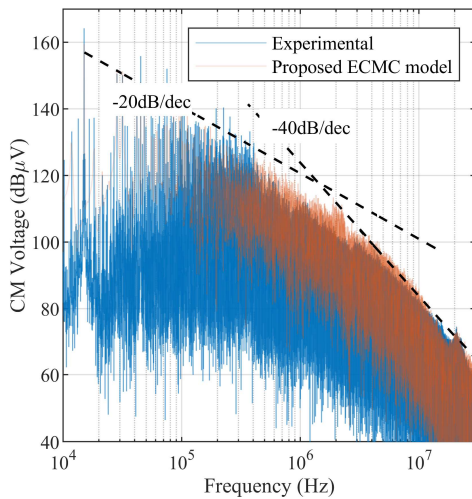


Fig. 17. Experimental result. Comparison of CM voltage obtained from Experimental test and obtained from Simulation via LTspice.

D. Comparison Experimental with Simulation (CM Current)

Fig. 18 shows a comparison of CM current at the DC-side, obtained experimentally, with the one obtained from simulations (CM voltage obtained from simulation by using the (ECMC model). Note that the model is representative providing lower than 5 dB of differences. Further analyses considering a more accurate model for DC cable and other elements not included in the LTspice could help to better fit the result.

VII. CONCLUSIONS

This work discussed the main aspects impacting the CMCS failure in DO-160G at the early-stage of an HF-EMC study. Analysis of the disturbance sources in the common-mode current spectrum is carried out. Then a simplified model allowing to quickly obtain accurate simulation results in a large range of frequency is proposed. This model is based on the extraction of some parasitic components surrounding the

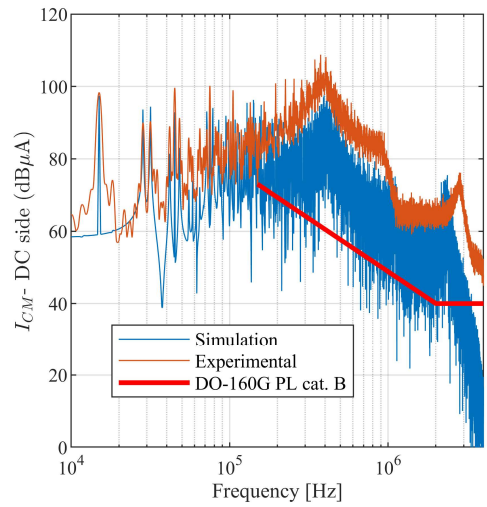


Fig. 18. Experimental result. Comparison of CM current obtained from Experimental test and obtained from Simulation via LTspice.

switching cell as well as is capable to reproduce the switching oscillations into common-mode voltage sources.

Then, estimation of the key performance parameters can be made thanks to the proposed ECMC model in tens of seconds instead of hours. Finally, the relevance of the model is checked on a real application case in two scenarios: i) case study 1 concerning module under development, and ii) case study 2 by using commercialized module showing benefits to reduce the ringing and overshoots when using CM and DM capacitors as well as having low parasitic inductances in the power loop (compared to case study 1). This approach makes it possible to have a practical tool for predicting EMC disturbances from the start of the design of a complex system and to optimize the routing of the board and the 3D assembly in compliance with the rules of the DO-160 aeronautic standard. Then, in this work it was possible to start early-stage analysis in a worst-case having very high parasitic values and not optimized filtering capacitors (i.e., study case 1) to a case with very low parasitic inductance with CM and DM filtering capacitors. Practical tests in case study 2 were presented for validation purposes. Practical tests of a 2-MW MCU-HT demonstrator based on a SiC-MOSFET inverter may be covered in future publications.

ACKNOWLEDGMENT

The authors acknowledge the financial and in-kind assistance from the IRT Saint Exupery members, industrial members (AIRBUS Central Research and Technology, STMicroelectronics, Deep Concept, Wolfspeed, and ANSYS), academic members (LAPLACE), and the financial support of the French National Research Agency. Also, the authors acknowledge industrial partners for sharing not-commercialized transistors SPICE models.

REFERENCES

- [1] H. Schefer, L. Fauth, T. H. Kopp, R. Mallwitz, J. Friebe, and M. Kurrat, "Discussion on electric power supply systems for all electric aircraft," *IEEE Access*, vol. 8, pp. 84 188–84 216, 2020.

- [2] A. Barzkar and M. Ghassemi, "Electric power systems in more and all electric aircraft: A review," *IEEE Access*, vol. 8, pp. 169 314–169 332, 2020.
- [3] J. Benzaquen, J. He, and B. Mirafzal, "Toward more electric powertrains in aircraft: Technical challenges and advancements," *CES Transactions on Electrical Machines and Systems*, vol. 5, no. 3, pp. 177–193, 2021.
- [4] B. Sarlioglu and C. T. Morris, "More electric aircraft: Review, challenges, and opportunities for commercial transport aircraft," *IEEE Transactions on Transportation Electrification*, vol. 1, no. 1, pp. 54–64, 2015.
- [5] E. Robles, A. Matallana, I. Aretxabaleta, J. Andreu, M. Fernández, and J. L. Martín, "The role of power device technology in the electric vehicle powertrain," *International Journal of Energy Research*, vol. n/a, no. n/a.
- [6] B. Zhang and S. Wang, "A survey of EMI research in power electronics systems with wide-bandgap semiconductor devices," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 1, pp. 626–643, 2020.
- [7] V. Perdikakis, M. J. Scott, K. J. Yost, C. Kitzmiller, B. Hall, and K. A. Sheets, "Comparison of Si and SiC EMI and efficiency in a two-level aerospace motor drive application," *IEEE Transactions on Transportation Electrification*, vol. 6, no. 4, pp. 1401–1411, 2020.
- [8] V. D. Santos, B. Cougo, N. Roux, B. Sareni, B. Revol, and J.-P. Carayon, "Trade-off between losses and EMI issues in three-phase SiC inverters for aircraft applications," in *2017 IEEE International Symposium on Electromagnetic Compatibility Signal/Power Integrity (EMCSI)*, 2017, pp. 55–60.
- [9] K. Rajashekara, "Parallel between more electric aircraft and electric-hybrid vehicle power conversion technologies," *IEEE Electrification Magazine*, vol. 2, no. 2, pp. 50–60, 2014.
- [10] B. Cougo, H. H. Sathler, R. Riva, V. D. Santos, N. Roux, and B. Sareni, "Characterization of low-inductance SiC module with integrated capacitors for aircraft applications requiring low losses and low EMI issues," *IEEE Transactions on Power Electronics*, vol. 36, no. 7, pp. 8230–8242, 2021.
- [11] M. Guacci, D. Bortis, I. F. Kovačević-Badstübner, U. Grossner, and J. W. Kolar, "Analysis and design of a 1200 v all-sic planar interconnection power module for next generation more electrical aircraft power electronic building blocks," *CPSS Transactions on Power Electronics and Applications*, vol. 2, no. 4, pp. 320–330, 2017.
- [12] S. Yin, K. J. Tseng, R. Simanjorang, Y. Liu, and J. Pou, "A 50-kw high-frequency and high-efficiency sic voltage source inverter for more electric aircraft," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 11, pp. 9124–9134, 2017.
- [13] G. Aulagnier, M. Cousineau, T. Meynard, E. Rolland, and K. Abouda, "High frequency EMC impact of switching to improve dc-dc converter performances," in *2013 15th European Conference on Power Electronics and Applications (EPE)*, 2013, pp. 1–9.
- [14] N. Oswald, B. H. Stark, D. Holliday, C. Hargis, and B. Drury, "Analysis of shaped pulse transitions in power electronic switching waveforms for reduced emi generation," *IEEE Transactions on Industry Applications*, vol. 47, no. 5, pp. 2154–2165, 2011.
- [15] D. N. Dalal, N. Christensen, A. B. Jorgensen, J. K. Jorgensen, S. Beczkowski, S. Munk-Nielsen, and C. Uhrenfeldt, "Impact of power module parasitic capacitances on medium-voltage sic mosfets switching transients," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 1, pp. 298–310, 2020.
- [16] T. Liu, R. Ning, T. T. Y. Wong, and Z. J. Shen, "Modeling and analysis of SiC MOSFET switching oscillations," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 3, pp. 747–756, 2016.
- [17] K. Sun, E. Raszmann, J. Wang, X. Lin, R. Burgos, D. Dong, and D. Boroyevich, "Modeling, design, and evaluation of active dv/dt balancing for series-connected sic mosfets," *IEEE Transactions on Power Electronics*, vol. 37, no. 1, pp. 534–546, 2022.
- [18] Y. Wu, S. Yin, Z. Liu, H. Li, and K. Y. See, "Experimental investigation on electromagnetic interference (emi) in motor drive using silicon carbide (sic) mosfet," in *2020 International Symposium on Electromagnetic Compatibility - EMC EUROPE*, 2020, pp. 1–6.
- [19] Y. Zhu, H. Li, C. Luo, Y. Liu, C. Wan, and J. Ma, "Influence of paralleled sic mosfet on turn-off gate voltage oscillation," in *2020 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2020, pp. 683–689.
- [20] Y. Wu, S. Yin, H. Li, and W. Ma, "Impact of r_c snubber on switching oscillation damping of sic mosfet with analytical model," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 1, pp. 163–178, 2020.
- [21] B. Liu, W. Li, D. Meng, L. Diao, Y. Ma, T. Qiu, and L. Diao, "Low-stray inductance optimized design for power circuit of sic-mosfet-based inverter," *IEEE Access*, vol. 8, pp. 20 749–20 758, 2020.
- [22] B. DeBoi, A. Lemmon, B. Nelson, C. New, and D. Hudson, "Modeling and validation of medium voltage sic power modules," in *2020 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2020, pp. 1964–1971.
- [23] B. W. Nelson, A. N. Lemmon, S. J. Jimenez, H. A. Mantooth, B. T. DeBoi, C. D. New, and M. M. Hossain, "Computational efficiency analysis of sic mosfet models in spice: Dynamic behavior," *IEEE Open Journal of Power Electronics*, vol. 2, pp. 106–123, 2021.
- [24] B. W. Nelson, A. N. Lemmon, B. T. DeBoi, M. M. Hossain, H. A. Mantooth, C. D. New, and J. C. Helton, "Computational efficiency analysis of sic mosfet models in spice: Static behavior," *IEEE Open Journal of Power Electronics*, vol. 1, pp. 499–512, 2020.
- [25] A. N. Lemmon, A. D. Brovont, C. D. New, B. W. Nelson, and B. T. DeBoi, "Modeling and validation of common-mode emissions in wide bandgap-based converter structures," *IEEE Transactions on Power Electronics*, vol. 35, no. 8, pp. 8034–8049, 2020.
- [26] P. Yang, W. Ming, J. Liang, I. Lütke, S. Berry, and K. Floros, "Hybrid data-driven modeling methodology for fast and accurate transient simulation of sic mosfets," *IEEE Transactions on Power Electronics*, vol. 37, no. 1, pp. 440–451, 2022.
- [27] M. Amara, C. Vollaïre, M. Ali, and F. Costa, "Black box emc modeling of a three phase inverter," in *2018 International Symposium on Electromagnetic Compatibility (EMC EUROPE)*, 2018, pp. 642–647.
- [28] V. D. Santos, "Modélisation des émissions conduites de mode commun d'une chaîne électromécanique. optimisation paramétrique de l'ensemble convertisseur filtres sous contraintes cem," Ph.D. dissertation, Institute National Polytechnique de Toulouse (INPT), 2019.
- [29] H. H. Sathler, B. Cougo, J.-P. Carayon, F. Costa, and D. Labrousse, "Modeling of common-mode voltage source for multilevel inverter topologies," in *2020 International Symposium on Electromagnetic Compatibility - EMC EUROPE*, 2020, pp. 1–3.
- [30] C. Li, "Adaptive EMC design for wide bandgap (wbg) power converters in aviation applications," <https://events.vtools.ieee.org/m/309629>, 2022.
- [31] Radio Technical Commission for Aeronautics (RTCA), DO-160 G, Dec. 8, 2010.
- [32] A. von Jouanne, H. Zhang, and A. Wallace, "An evaluation of mitigation techniques for bearing currents, EMI and overvoltages in ASD applications," *IEEE Transactions on Industry Applications*, vol. 34, no. 5, pp. 1113–1122, 1998.
- [33] V. D. Santos, N. Roux, B. Revol, B. Sareni, B. Cougo, and J.-P. Carayon, "Unshielded cable modeling for conducted emissions issues in electrical power drive systems," in *2017 International Symposium on Electromagnetic Compatibility - EMC EUROPE*, 2017, pp. 1–6.
- [34] F. Costa, C. Vollaïre, and R. Meuret, "Modeling of conducted common mode perturbations in variable-speed drive systems," *IEEE Transactions on Electromagnetic Compatibility*, vol. 47, no. 4, pp. 1012–1021, 2005.
- [35] K. Abouda, G. Aulagnier, E. Rolland, and M. Cousineau, "Analytical approach to study electromagnetic emission eme contributors on dc/dc applications," in *2015 10th International Workshop on the Electromagnetic Compatibility of Integrated Circuits (EMC Compo)*, 2015, pp. 77–82.
- [36] L. Jaroslaw, *High Frequency Conducted Emission in AC Motor Drives Fed By Frequency Converters*. John Wiley Sons, Ltd, 2018.
- [37] R. Phukan, X. Zhao, P. Asfaux, D. Dong, and R. Burgos, "Investigation of staggered pwm scheme for ac common mode current minimization in sic-based three-phase inverters," *IEEE Transactions on Transportation Electrification*, vol. 8, no. 4, pp. 4378–4390, 2022.
- [38] L. Zhai, G. Hu, C. Song, M. Lv, and X. Zhang, "Comparison of two filter design methods for conducted emi suppression of pmsm drive system for electric vehicle," *IEEE Transactions on Vehicular Technology*, vol. 70, no. 7, pp. 6472–6484, 2021.
- [39] E. R. C. da Silva, E. C. dos Santos, and B. Jacobina, "Pulsewidth modulation strategies," *IEEE Industrial Electronics Magazine*, vol. 5, no. 2, pp. 37–45, 2011.
- [40] M. Baiju, K. Mohapatra, R. Kanchan, and K. Gopakumar, "A dual two-level inverter scheme with common mode voltage elimination for an induction motor drive," *IEEE Transactions on Power Electronics*, vol. 19, no. 3, pp. 794–805, 2004.
- [41] D. Jiang, J. Chen, and Z. Shen, "Common mode emi reduction through pwm methods for three-phase motor controller," *CES Transactions on Electrical Machines and Systems*, vol. 3, no. 2, pp. 133–142, 2019.
- [42] J. d. A. Wanderley, R. M. L. Magalhães, G. A. d. A. Carlos, and I. R. F. M. P. da Silva, "Common-mode reduction svpwm for flexible series/parallel motor drives," in *2021 Brazilian Power Electronics Conference (COBEP)*, 2021, pp. 1–6.
- [43] B. Gilles, *THE LTSPICE XVII SIMULATOR: Commands and Applications*. Adolf Würth GmbH Co. KG, 2021.

- [44] M. Caponet, F. Profumo, R. De Doncker, and A. Tenconi, "Low stray inductance bus bar design and construction for good emc performance in power electronic circuits," *IEEE Transactions on Power Electronics*, vol. 17, no. 2, pp. 225–231, 2002.
- [45] A. Apelsmeier, C. Rettner, and M. März, "Model for conducted emission of sic power modules for automotive traction inverter-comparison to behaviour-based model," in *2020 IEEE 21st Workshop on Control and Modeling for Power Electronics (COMPEL)*, 2020, pp. 1–8.
- [46] D. H. Tran, B. Cougo, G. Segond, and H. H. Sathler, "Optimal design of a three-phase 540v/70kva sic inverter for aircraft applications," in *2023 IEEE International Conference on Electrical Systems for Aircraft, Railway, Ship Propulsion and Road Vehicles International Transportation Electrification Conference (ESARS-ITEC)*, 2023, pp. 1–6.
- [47] A. O. Adan, H. Nakagawa, Y. Kakizaki, and L. Burgyan, "Benchmarking power transistors and power modules for high-temperature operation (tj200°C)," in *2017 IEEE Transportation Electrification Conference and Expo (ITEC)*, 2017, pp. 662–667.