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Static and Dynamic Characterization of a 1.2 kV SiC MOSFET in Third Quadrant

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Index Terms—SiC MOSFET, Device characterisation, Experimental testing, Double pulse test, DC-DC power converter.

Abstract—In this paper, the 3rd quadrant behavior of a 1.2 kV SiC MOSFET without additional anti-parallel diode is investigated. More specifically, the effect of the gate-source voltage on the reverse conduction is presented, and shows a strong dependency even for a gate voltage varying below the threshold voltage. The static characterization is compared to three other types of MOSFETs that present a stronger reverse current path due to their architectures. A dynamic characterization is also performed to describe the transition between the body-diode conduction and the channel reverse conduction within the 3rd quadrant (a.k.a. synchronous rectification). Both static and dynamic behaviors are compared to the device's LTspice™ model and highlights the differences between experiment and simulation in 3rd quadrant as the gate voltage below the threshold voltage is not taken into account in this model. Insights towards a more precise modeling for this operating region are discussed at the end of the article.

I. INTRODUCTION

Silicon Carbide (SiC) devices seem to be becoming massively used in power application like railway and automotive traction inverters due to their multiple benefits (e.g. high temperature, high mobility, high voltage, fast transient, low losses etc.). One drawback though is the low performance of the body diode in the 3rd quadrant operation region, compared to equivalent silicon devices. The internal reverse diode presents a higher forward voltage [1], [2], and may lead to reliability issues after an extended use [3]. The use of an external antiparallel junction barrier Schottky (JBS) diode may partially resolve this problem, but it is costly and takes extra surface area. Power devices architectures

integrating a Schottky Barrier Diode (SBD) are under development [4]. However, their performance, robustness and reliability still need to be evaluated. Power converter designers are moving towards diode-less architectures which require precise dead time management with the aim of reducing the body-diode conduction time at a minimum, while guaranteeing a safe operation throughout the operating cycle. It is therefore essential to rely on comprehensive 3rd quadrant characteristics to develop active dead-time control circuits, while introducing accurate modeling of the impact of the body-diode conduction versus the channel conduction at the system level.

This paper provides an experimental 3rd quadrant characterization of a third generation SiC MOSFET, including static and dynamic behaviors study. Except when explicitly noted, all tests presented hereafter have been performed using a C3M001612K SiC MOSFET (Wolfspeed) rated at 1.2 kV and 115 A with an on-resistance of 16 mΩ (25°C). This transistor does not contain any antiparallel SBD diode, so its body diode is used as a freewheeling diode.

II. LIMITATIONS OF MODELS

SiC device manufacturers do not provide extensive characterizations of the 3rd quadrant operation of their components, as they do with 1st quadrant operation. The understanding and modeling of the reverse conduction mechanism is critical in the design of high power converters [5].

Fig. 1 presents the static and dynamic behavior of the C3M0016120K Spice model in reverse conduction. Unlike what is found in 3rd quadrant characterization literature [6], [7], the simulation model does not produce any variation of the static curve for the gate-to-source voltage varying below the threshold voltage (i.e. 2.6 V for this model). As a consequence, the dynamic behavior

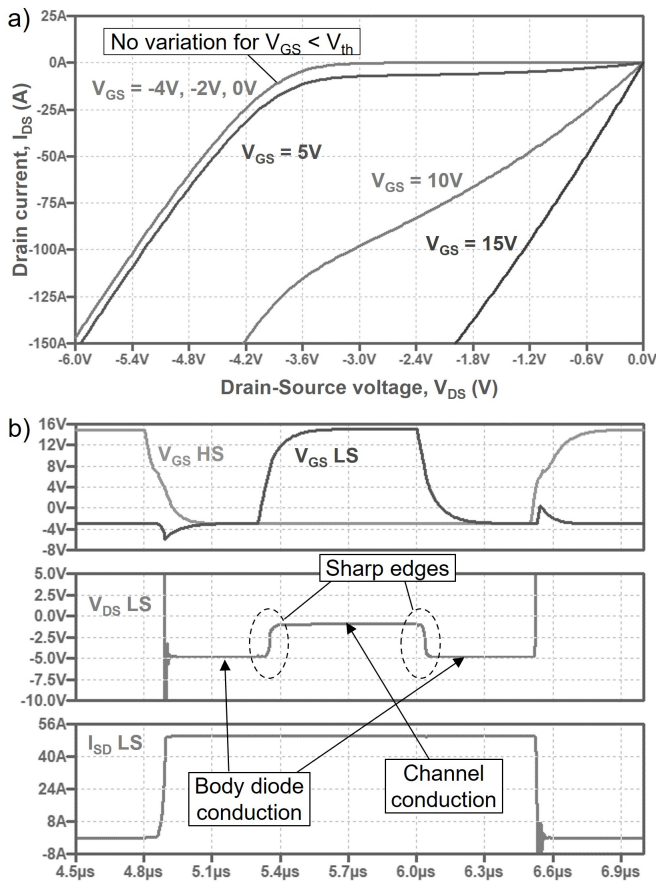


Fig. 1. Simulated C3M0016120K Spice model provided by the manufacturer. a) 3rd quadrant characteristic at $T=20^{\circ}\text{C}$ and b) dynamic 3rd quadrant behavior ($V_{BUS} = 800\text{ V}$, $I_{load} = 50\text{ A}$, $T = 20^{\circ}\text{C}$, $V_{Driver} = -3\text{ V} / +15\text{ V}$, $R_{gate} = 5\ \Omega$)

of the transition from diode conduction mode to channel conduction mode (and vice versa) is not completely described in the 3rd quadrant operation. The sharp edges given by the simulation can lead the power converter designers to make mistakes in the dead-time management and the accurate losses estimation.

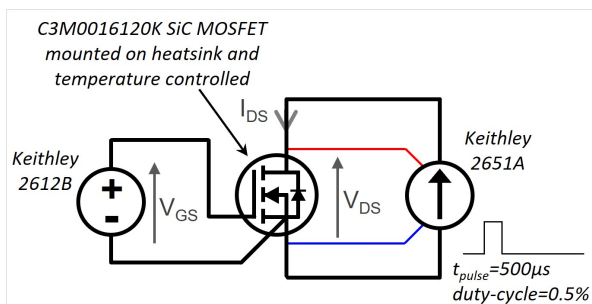


Fig. 2. Static characterization setup

III. STATIC CHARACTERIZATION

This section focuses on the observation of the real behavior of power devices that involve both a body diode and a reverse channel conduction mechanism as presented in [8]. Components with similar voltage and current ratings with different technologies are compared to analyze their respective behavior in reverse operation.

The third quadrant characterization has been performed with two source-meter units (SMU) as shown in Fig. 2. The Keithley 2651A power SMU provides drain current pulses up to 50 A and measures the drain voltage with two dedicated Kelvin sense wires. The Keithley 2612B SMU biases the gate at the desired voltage level. The current pulses duration has been set to 500 μs with a duty cycle of 0.5% to avoid the junction self-heating. The gate voltage is stepped, starting at -4 V and up to +15 V. The transistor case is mounted on a

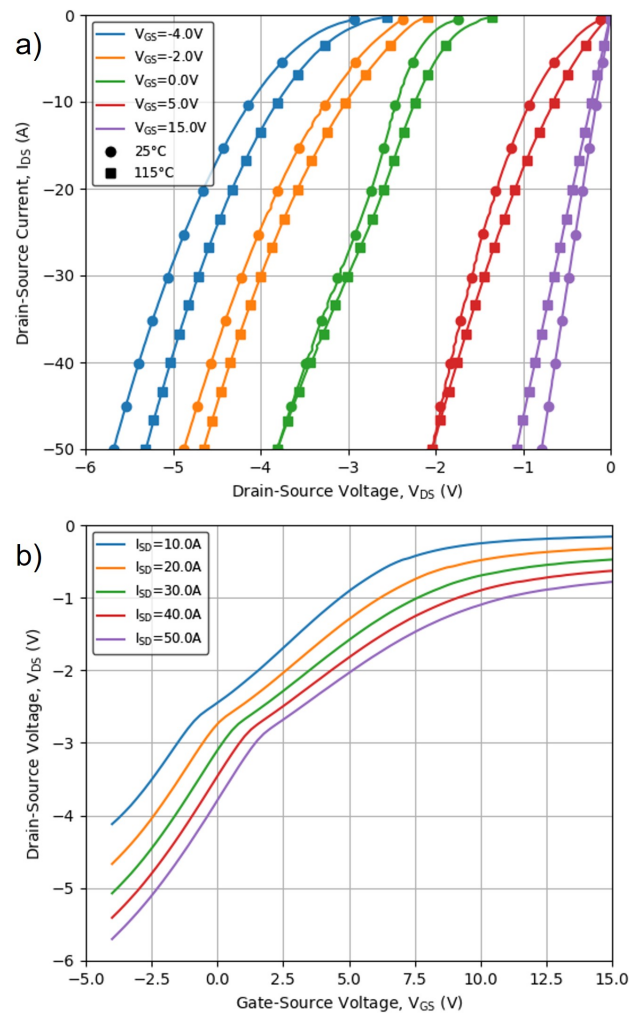


Fig. 3. a) Measured third-quadrant characteristic of the C3M0016120K device at 25°C and 115°C b) Measured V_{DS} with V_{GS} at 25°C

TABLE I
OVERVIEW OF THE 4 TESTED DEVICES

Model Name	Device type	Ratings
C3M0016120K	3 rd generation SiC MOSFET	1.2 kV, 115 A
APT60N60BCS	Super junction Si MOSFET	600 V, 60 A
TW083N65C	3 rd gen. SiC MOSFET with built-in SBD	650 V, 30 A
CPM2-1200-0025B CPW5-1200-Z050B	2 nd gen. SiC MOSFET + SiC Schottky diode on the same package	1.2 kV, 98 A

temperature-controlled heatsink.

The experimental 3rd quadrant I-V curve is presented in Fig. 3 a). It exhibits the variation of the characteristic for gate voltages below the threshold. The measurement of the drain-source voltage relative to the gate-source

voltage (Fig. 3 b) gives us an indication of the current path in the third quadrant. At a low gate bias the current flows mainly through the internal PN junction with a high forward voltage, as a consequence of the high built in potential due to the wide bandgap of SiC. At a high gate bias, the channel is fully formed and the current flows through the channel completely. The reverse conduction voltage gradually varies with the gate voltage over its entire range.

A. Comparison of four different technologies in 3rd quadrant

The same experiment has been realized with three other power devices to compare the 3rd quadrant behavior for various technologies. The table I summarizes the devices considered and their key specifications. Fig. 4 depicts the characterization results of the four

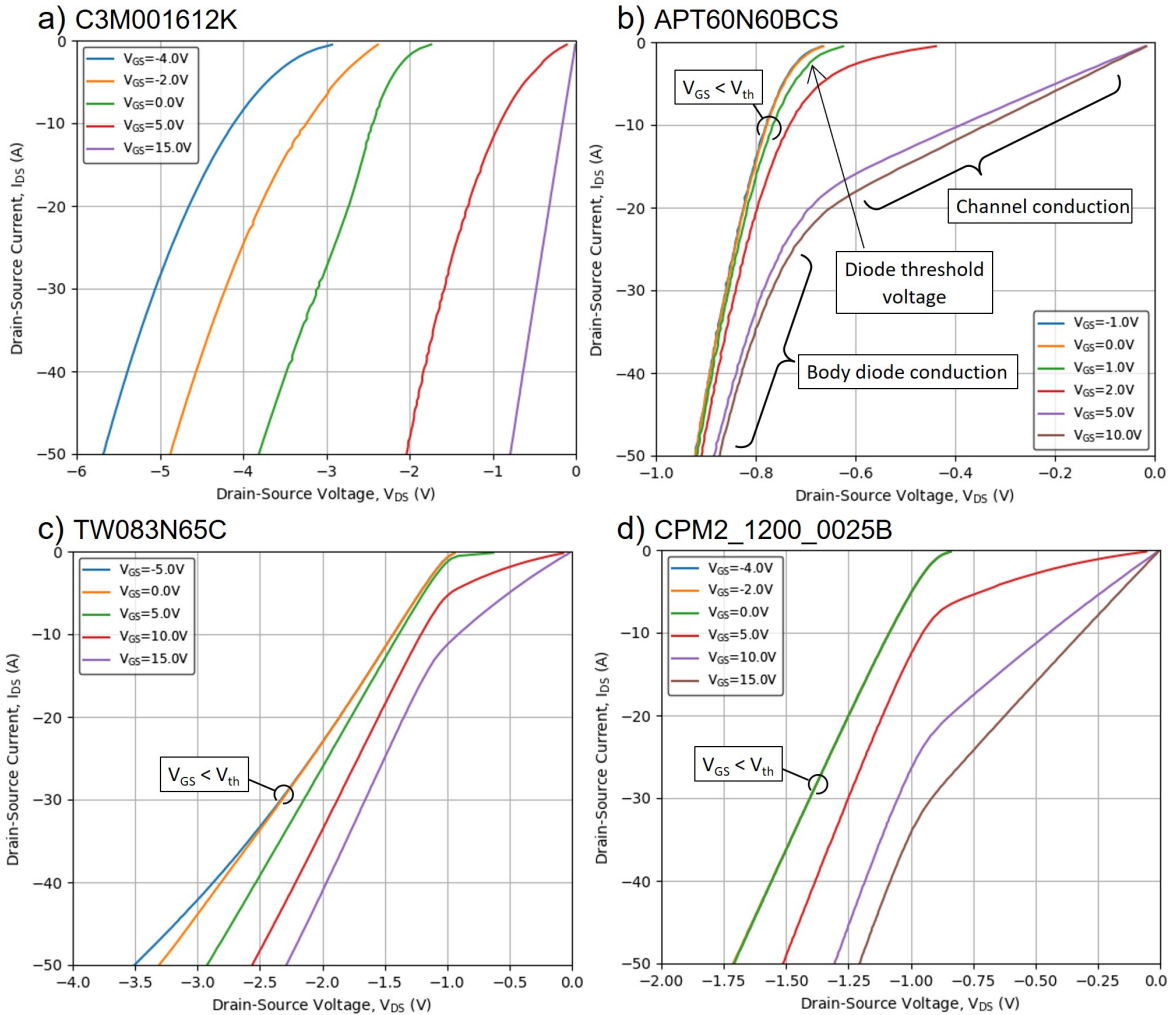


Fig. 4. Static 3rd quadrant characterization. Comparison between a) C3M0016120K , b) APT60N60BCS , c) TW083N65C , and d) CPM2_1200_0025B. All test performed at 20°C

components with different behaviors, which are mainly due to the specific reverse current path they provide. The C3M0016120K present a higher 3rd quadrant body-diode drop-voltage (between two times and six times higher than the three other devices) at the lowest gate-source bias voltage. Its apparent body-diode knee voltage is also highly dependent on the applied gate voltage even below its threshold voltage. Rather, the following three power switches offer a well-defined diode knee voltage (0.62 V for the APT60N60BCS, 1 V for the TW083N65C, and 0.85 V for the CPW5-1200-Z050B) which is independent on the applied gate voltage. For high reverse currents in the three last transistors, the current path is dominated mainly by the diode, even if the channel is fully on (at the highest gate voltage). One can notice that the gate voltage below the MOSFET threshold voltage has almost no influence on the third quadrant behavior.

IV. DYNAMIC CHARACTERIZATION

A. Double-pulse setup for 3rd quadrant dynamic characterization

One popular method of characterizing switching-state power devices is the Double Pulse Test (DPT). It allows to measure the dynamic turn-on and turn-off behaviors and losses under full load current and high input voltage, while avoiding an increase in the junction temperature [9], [10]. The reverse recovery losses related to the body diode conduction are widely covered in the literature [11]. This study focuses on the dynamic behavior within the 3rd quadrant. For our purpose, the DPT is used to characterize the transition from the body-diode conduction mode to the channel conduction mode (and vice versa) in 3rd quadrant. This dynamic characterization of synchronous rectification is not typically presented in high power electronics.

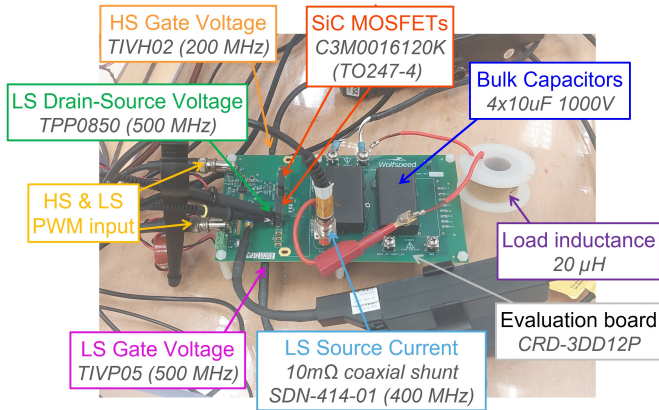


Fig. 5. Double pulse testing setup

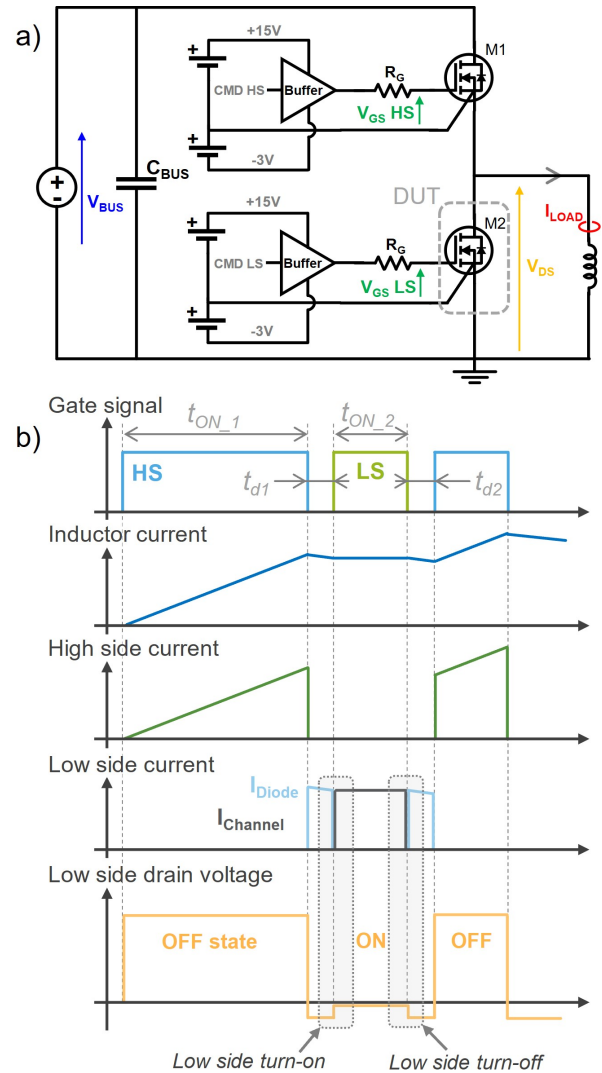


Fig. 6. DPT for 3rd quadrant characterization. a) setup schematic and b) timing diagram including synchronous control of the low side switch

The classical DPT has been adapted with complementary transistor control capability to characterize the reverse conduction mode. As presented in Fig. 6, the high side switch is activated during t_{ON_1} to build up the inductor current. Then the low side switch (DUT) is controlled to characterize the 3rd quadrant behavior considering both body-diode and channel conduction mode.

The DPT measurements were performed using a Tektronix 5 Series MSO scope which provide 12-bit of vertical resolution at 1GHz bandwidth. The drain-source voltage of the power switch is measured with a Tek TPP0850 800 MHz 1 kV x50 passive probe. The vertical scale for the V_{DS} channel is set to few volts per division to capture accurately the reverse conduction

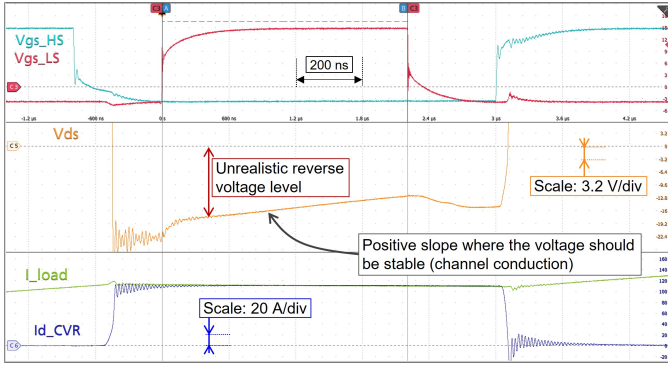


Fig. 7. Illustration of the saturation of the scope front-end with the classical DPT under full bus voltage (i.e. 800 V) in third quadrant. V_{DS} is measured with a 800 MHz, 1 kV, x50, passive probe at scale 3,2 V/div

channel voltage and the body diode forward voltage. The scope input circuitry becomes highly saturated before the high side transistor turns off. The V_{DS} of the low side transistor is indeed equal to the DC bus voltage (i.e. 800 V in nominal operating conditions). The typical overdrive recovery time of the scope is greater than $10 \mu\text{s}$ in these conditions. For that reason, the V_{DS} signal depicted in Fig. 7 is distorted and cannot be used for dynamic characterization of the third quadrant transient behavior. To overcome this limitation, an on-state measurement circuit including an off-state voltage clamping mechanism may be used [12]. This solution adds complexity to the setup and may cause timings issues. For our experiments, a special DPT under reduced DC-bus voltage has been developed to better characterize the 3rd quadrant operation of power switches, under a similar load current level.

B. Dynamic characterization under reduced DC bus voltage and nominal current load

It has been found that with a DC bus voltage of 50 V the VDS measurement is no longer affected by saturation problems. The time t_{ON_1} during which the inductor is charged has to be increased significantly to

TABLE II
DOUBLE-PULSE SETUP CONDITIONS

Param	Description	Value
V_{BUS}	Bus voltage	800 V
I_{SD}	Nominal test current	50 A
L	Load inductance	20 μH
V_{driver}	Gate driver supply	+15 V / -3 V
R_G	External gate resistance	4 Ω
t_{on_1}	Inductor charging time	18.7 μs
t_{on_2}	Low side synchronous control time	2.75 μs
t_d	Dead-time	1.5 μs

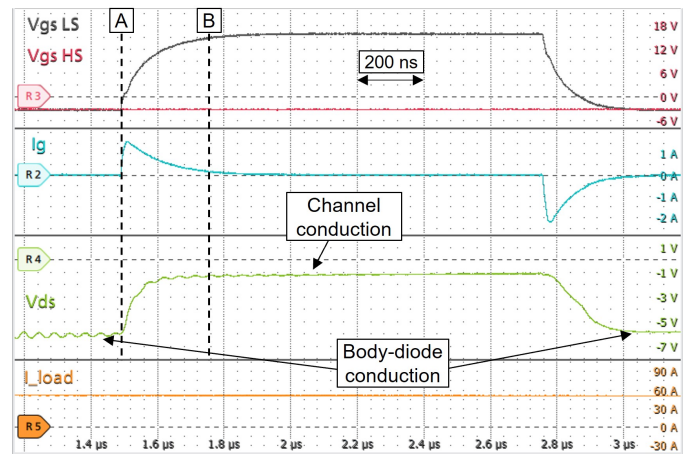


Fig. 8. Double-pulse measurements in 3rd quadrant under reduced DC-bus voltage ($V_{BUS} = 50 \text{ V}$, $I_{SD} = 50 \text{ A}$, $V_{driver} = +15 \text{ V} / -3 \text{ V}$, $R_G = 4 \Omega$, $T = 20^\circ\text{C}$). Zoom on low-side turn-on and turn-off

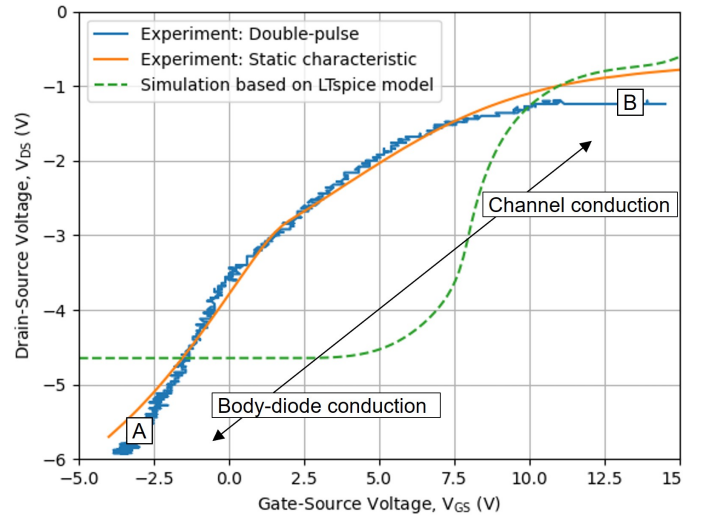


Fig. 9. V_{DS} vs. V_{GS} comparison between static (orange) and dynamic (blue) characterization and the Spice model (green) at $T = 20^\circ\text{C}$ and $I_{SD} = 50 \text{ A}$

reach the nominal current but it has no influence on the temperature of the DUT. All parameters are presented in table II.

The relation between the gate-source voltage and the drain-source voltage is extracted from DPT results (waveforms as a function of time) and plotted on Fig. 9 (blue curve). The measured static characteristic is superimposed (orange curve) to compare the two characterization methods. The match of the static and dynamic curves implies that parasitic elements have almost no effects on 3rd quadrant switching. The drain-source voltage variation is in fact much slower in 3rd quadrant with a dv/dt of 0.058 kV/ μs compared to 32 kV/ μs in 1st quadrant switching. Thus, the dynamic

behavior of the transistor is mostly related to the speed of the gate voltage rising in this operating region. The Spice model simulation (green curve) is compared to the experiment to show the difference in behavior in the 3rd quadrant modeling. The model does not show any variation of the conduction for the gate-source voltage lower than the threshold voltage, as one also expects from Fig 1.

V. TOWARDS IMPROVED MODELS

The Spice model presented in the first part and provided by the manufacturer is based on Enz-Krummenacher-Vittoz (EKV) method. This model has the ability to describe MOSFET behavior over weak, moderate and strong inversion regions with a single equation [13], [14], but it does not characterize the body diode contribution directly. The static and dynamic characterizations described previously make it clear that the body diode modeling cannot be done independently of the MOSFET channel. In the case of SiC MOSFET there is no clear distinction between the diode conduction and the channel conduction when the gate voltage varies. The 2D TCAD numerical simulations presented in [6] and [15] highlight the existence of a reverse resistive current path in addition to the body diode, even for gate voltage lower than the MOSFET threshold voltage.

Even if the accurate modeling of the 3rd quadrant behavior is not the aim of this article, a first approach may nonetheless be proposed. The circuit structure of the model is shown in Fig. 10. The drain current is the contribution of two currents, the forward and reverse currents $I_{D,f}$ and $I_{D,r}$ represented by the expressions (1) and (2). It is based on the modified EKV model proposed in [14] for the modeling of a SiC MOSFET. It is adapted and specifically extended with additional parameters to fit the 3rd quadrant curves and to describe the reverse conduction voltage variation relative to the gate source voltage. In one hand, (1) indicates the value

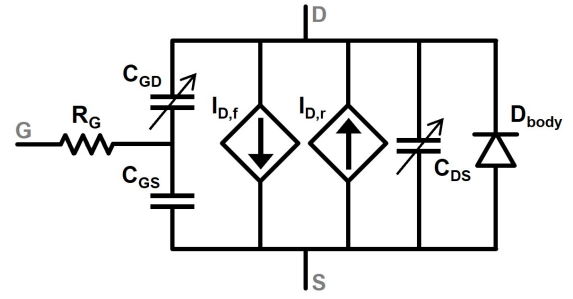


Fig. 10. Behavioral model of SiC MOSFET

of the forward current in the saturation region which is driven by the gate-to-source voltage when the potential $V_{GS} - V_{th}$ is positive.

$$I_{D,f} = 2g_m \Phi_t^2 k_s \left[\ln \left(1 + e^{\frac{V_{GS} - V_{th}}{2k_s \Phi_t}} \right) \right]^k (1 + \lambda V_{DS}) \quad (1)$$

On the other hand, (2) provides the value of the reverse current to describe both the linear region and the 3rd quadrant operation.

$$I_{D,r} = 2g_m \Phi_t^2 k_s \left[\ln \left(1 + e^{\frac{V_{GS} - V_{th} - n_{sgn}(V_{DS}) |V_{DS}|^a}{2k_s \Phi_t}} \right) \right]^k \times (1 + \lambda V_{DS}) \quad (2)$$

In the original expression of the EKV model, parameters a and n are added to fit the transistor curves in the linear region. In our case, in order to offer more flexibility to describe the behavior in the 3rd quadrant, the parameter n becomes dependent of the voltage V_{DS} .

$$n(V_{DS}) = (n_a - n_b) \frac{1 + \tanh(V_{DS} + v_d)}{2} + n_b \quad (3)$$

Now, thanks to (3), depending on the sign of the signal $V_{DS} + v_d$, either the value n_a or n_b is taken into account for the parameter n allowing to fit curves both in the linear region and in the channel reverse conduction region. The parameter v_d is introduced to control the transition between these two modes. Table III provides the nature and the values of the parameters used the model to fit the characteristics of the transistor C3M0016120K.

One can notice a good match between the model and the experimental results in Fig. 11. As expected, in 3rd quadrant, the model provides characteristics that are correctly shifted depending on the value of V_{GS} and the admittance of the conducting channel is well represented. Finally, at high level of negative drain current, when the knee voltage of the body diode is reached, its contribution becomes significant and it imposes the drain-source voltage law.

TABLE III
PARAMETERS USED IN MODIFIED EKV MODEL

	Description	Value	Unit
g_m	Transconductance	1.52	A/V ²
V_{th}	Threshold voltage	3.8	V
Φ_t	Thermal voltage	1.02	V
k_s	Subthreshold slope parameter	0.38	
k	Law exponent	2.07	
λ	Channel length modulation	0.081	V ⁻¹
a	Triode region parameter	0.918	
n_a	1 st quadrant slope parameter	1.175	
n_b	3 rd quadrant slope parameter	2.75	
v_d	Reverse path shift parameter	1.92	V

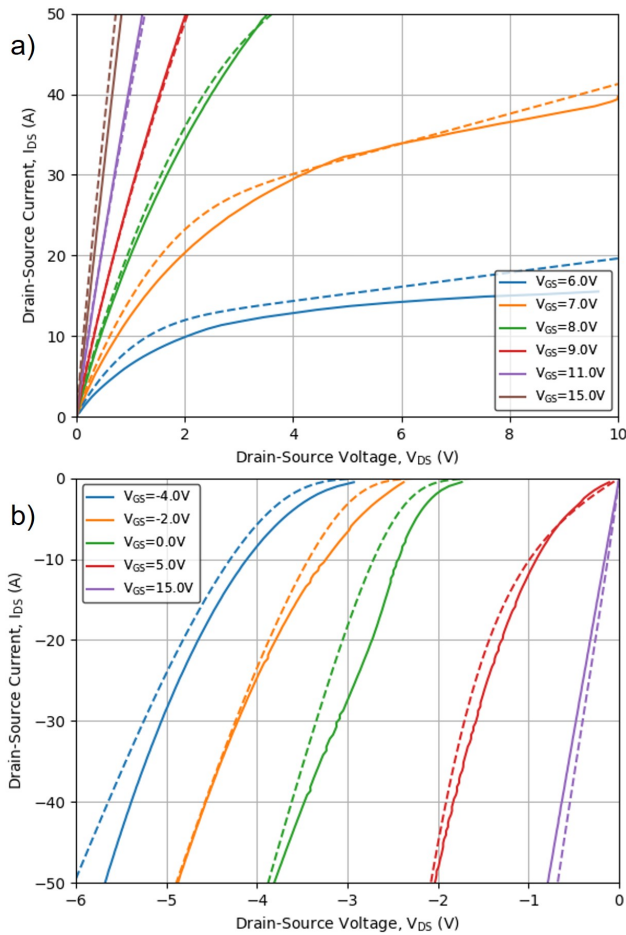


Fig. 11. Comparison between the C3M0016120K static characteristics (solid line) and the proposed modified EKV model (dashed line) in a) the 1st quadrant and b) the 3rd quadrant at $T=20^{\circ}\text{C}$

VI. CONCLUSION

The characterization of the 3rd quadrant behavior for a third generation SiC MOSFET without any additional reverse diode has been investigated. The comparison with the existing Spice model shows the need to consider the gate voltage in this operating region. Differences are due to the absence of a modeling for the reverse resistive current path in sub-threshold gate-source voltage operation. According to the experimental static characterization, the body-diode knee voltage shows a strong gate-source voltage dependence. This static characteristic has been compared with three other devices that demonstrate a stronger body diode capacity and therefore a well-defined diode knee voltage.

A 3rd quadrant characterization under dynamic conditions has been performed using a special double pulse setup. The dynamic characterization confirmed the results obtained in the first part. These results emphasize the importance of the gate driver negative

rail choice when designing a power converter using SiC MOSFETs. Indeed, a higher gate voltage during 3rd quadrant body-diode conduction may reduce losses and the stress on the body-diode.

Based on these experimental results, a first modeling approach for this operating region has been proposed. The EKV model is slightly modified to describe the role of the gate voltage below the threshold in 3rd quadrant. An additional and more detailed analytical study will be conducted to propose a simple behavioral model based on EKV, along with a discussion from the device physic perspective to describe accurately the 3rd quadrant behavior and its difference with 1st quadrant.

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