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SiC Power MOSFET Overload Detection, Short-Circuit Protection and Gate-Oxide Integrity Monitoring Using a Switched Resistors Dual-Channel Gate-Driver

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Abstract

The main factor still hindering a wide industrial adoption of SiC power MOSFETs is essentially a global reduced ruggedness in comparison to their Si counterparts. The proposed gate driving architecture leverages fault-induced gate voltage disturbances and enhances them to facilitate their detection through two dedicated commutated gate resistors. This approach combines switching dynamics and enhanced ON-state fault sensitivity. This architecture, affording innovative short-circuits and overload detections, as well as gate-oxide integrity monitoring, was validated on a 600V short-circuit power test bench using commercial 1200V/36A SiC MOSFETs.

1. Background, previous work and contribution

If SiC power MOSFETs are reaching industrial maturity, their deployment in critical applications still requires research efforts on their reliability and robustness in extreme abnormal operation. Short-circuit protection methods currently adopted in the industry essentially rely on a drain-source voltage (V_{DS}) or drain current (I_{DS}) integrated monitoring. These methods are relatively invasive and costly as they require the use of a large high voltage desaturation diode [1], non-integrable in an analog IC. In the automotive field, some particular Si power transistors' chips are equipped with an embedded current sensor in compliance with Automotive Grade (AG) standards, but still not standardised yet on SiC substrates (except in [2]). In addition to improvements in chip architecture design, another approach consists in functionalising the gate-driver to efficient short-circuit / over-current handling and dedicated gate-oxide health monitoring – conditioning strategies. Among the previous work of the authors on discrete 1.2kV and 1.7kV SiC power MOSFETs, it was shown in [3] [4] that the reduction of the short-circuit power density to 4kW/mm² made it possible to exceed the threshold of 10 μ s short-circuit withstand time capability (T_{SCW}) and to bring the chip to a safe gate-source short and drain-source open failure mode (Fail-to-Open FTO mode). Other authors have confirmed this property [5]. However, this requires a strong and permanent reduction in the gate voltage (V_{GS}) to 12V

or even 10V, which obviously leads to an increase in drain-source on-state resistance ($R_{DS(ON)}$) of at least 30%.

To avoid this penalty while keeping a simple gate-driver structure, we propose in this paper to naturally produce the reduction in the gate voltage only when the short-circuit occurs. This is achieved by dynamically inserting a high value gate resistance only during the ON-state operation, between turn-on and turn-off sequences. Indeed, the Schottky Emission (SE) thermionic gate leakage current is able to reduce the gate voltage enough to obtain both increased T_{SCW} and FTO properties [6]. Then, a dual-channel gate-driver architecture has been developed to manage the dedicated gate resistors, for switching and ON-state, with high ratio and accuracy. The proposed architecture, previously introduced in [7] by the authors, can be further functionalised to support fast short-circuit detection and many other experimentally validated functions such as overload current detection and gate-oxide damage detection. The proposed article is organized as follows: in section 2) the dual-channel gate-driver is presented to extend T_{SCW} and obtain the FTO mode on a 1.2kV - 80m Ω gen. II SiC power MOSFET; in section 3) a gate voltage threshold and blanking time set is introduced to quickly detect Hard Switching Faults (HSF) and Faults Under Load (FUL). Overload (Over-Current Protection OCP) events are tackled in section 4). Finally, in section 5) a Gate-Oxide Damage

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(GOD) detection is shown based on the proposed dual-channel gate-driver structure.

2. Dual-channel gate-driver structure, first application to T_{SCW} extension and unique drain-source FTO mode

The core of the proposed innovation is based on a 2-channel gate-driver as illustrated in Fig. 1a and was the subject of a patent application [8]. A first channel named *Fast-lane* only manages the turn-on and the turn-off through a low gate resistance value R_{FAST} . A second parallel channel named *Slow-lane* handles the monitoring of the SE gate leakage current occurrence through a high gate resistance value R_{SLOW} during HSF events. As illustrated in Fig. 1b, an *Enable* control signal quickly activates the *Fast-lane* only right before each switching transition with a tuned timing in order to stabilize the gate voltage transient and to reduce the crosstalk in an inverter leg operation. The *Slow-lane* is directly controlled by the PWM signal and will be the only active lane during the ON-state through its R_{SLOW} gate resistance. The other buffers are put in a high impedance state (Hi-Z).

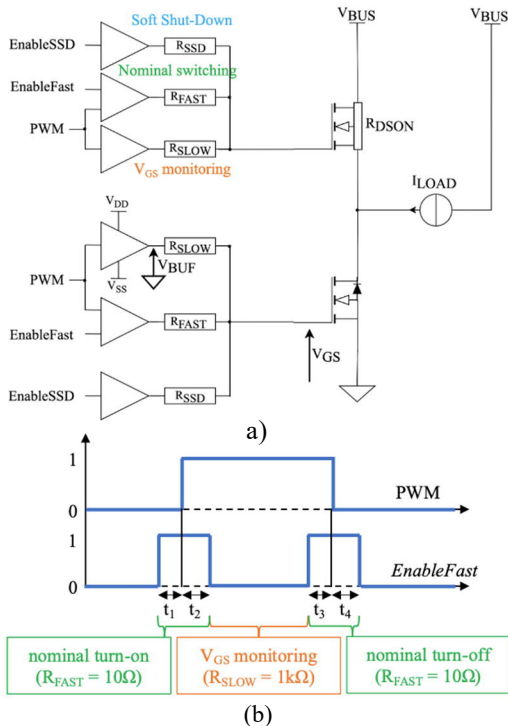


Fig. 1: a) Proposed parallel 2-channel Fast-lane and Slow-lane SiC MOSFET gate-driver, b) Enable and PWM control signals ($t_1 = t_3 = 50\text{ns}$, $t_2 = t_4 = 830\text{ns}$).

Fig. 2 gives out the global setup used, based on a previously developed 600V-200J short-circuit 3-lead TO-247 device test bench [3], including the new dual-channel gate-driver for the low-side DUT. During the

characterisation process, the high-side is equipped with a standard gate-driver. This proposed gate-driver board is plugged into the short-circuit test bench and is driven by a FPGA board and a touchpad set for control settings, as depicted in Fig. 1b ($t_{1/2/3/4}$ parameters, duty cycle and switching frequency).

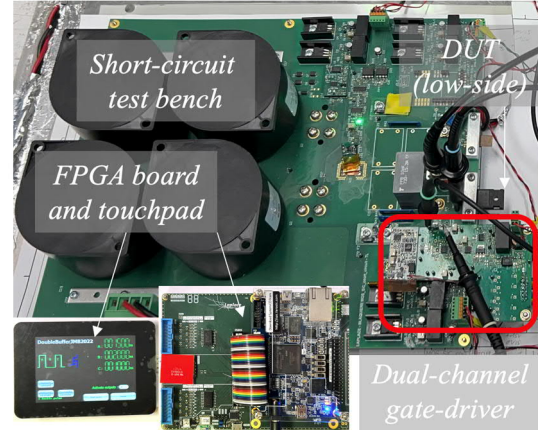


Fig. 2: 600V short-circuit test bench including the new gate-driver, further introduced in [7].

The experimental results in HSF operation are presented in Fig. 3.

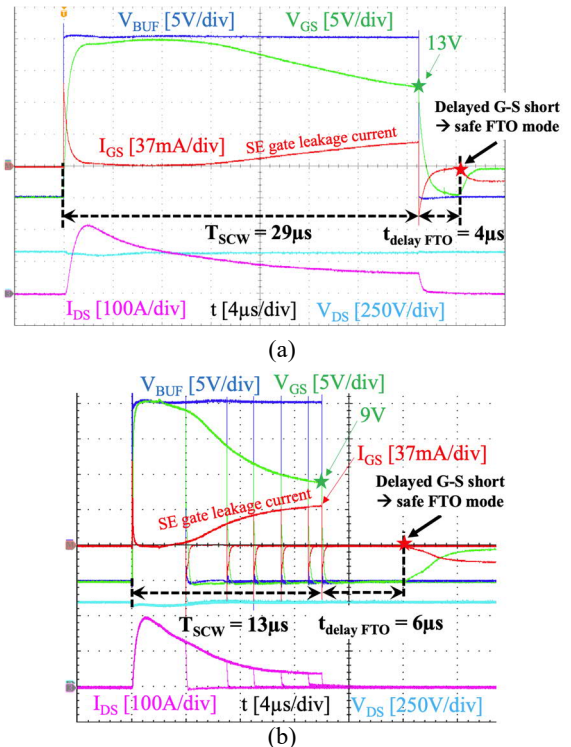


Fig. 3: HSF operation with safe FTO mode illustrations, $V_{DD} = 20\text{V}$, $V_{SS} = -5\text{V}$, a) traditional single-channel gate-driver ($R_{GATE} = 270\Omega$, $V_{DS} = 333\text{V}$), b) dual-channel Fast/Slow gate-driver architecture for different pulse durations until the appearance of the FTO mode ($R_{FAST} = 47\Omega$, $R_{SLOW} = 4.3\text{k}\Omega$ at a high voltage of $V_{DS} = 600\text{V}$).

For all tests, the gate-driver power supply voltage is [-5V/20V] in order to minimize $R_{\text{DS(ON)}}$ value during the ON-state operation. In Fig. 3a, a preliminary test at a low V_{DS} (333V) is illustrated in a standard single-channel gate-driver configuration.

In order to bring the SiC MOSFET to a safe FTO mode, a high value gate resistor $R_{\text{GATE}} = 270\Omega$ is used. A deep ohmic-type gate-source voltage drop appears, caused by the SE gate-oxide leakage current at high temperatures. Such operation leads to a reduction of the power density applied to the chip and therefore, to a reduction of the junction temperature rise.

For $T_{\text{PULSE}} = 29\mu\text{s}$ (T_{SCW}), a delayed drain-source safe FTO failure mode appears. It is caused by the gate-source short $t_{\text{d_FTO}} = 4\mu\text{s}$ after the turn-off [9]. However, considering such a high gate resistance value, the turn-on speed is clearly unacceptable. In Fig. 3b, to overcome this limitation the proposed dual-channel gate-driver is used in Fast/Slow mode according to the proposed structure and the dedicated control signals depicted in Fig. 1. $R_{\text{FAST}} = 47\Omega$ effectively handles the fast turn-on and turn-off while $R_{\text{SLOW}} = 4.3\text{k}\Omega$ is introduced the rest of the time. This high R_{SLOW} value causes a spectacularly strong gate-source voltage drop which leads to the final safe FTO failure mode. At a nominal drain-source voltage of 600V, a high R_{SLOW} value must be used to reduce the gate-source voltage deeply and effectively, thus "triggering" the safe FTO mode before the chip thermal runaway appears. Finally, it should be noted that the effective T_{SCW} is clearly increasing, from $8\mu\text{s}$ in a standard gate-driver [10] to $13\mu\text{s}$ (+62%) with the proposed new gate-driving strategy while considering the same drain and gate bias (600V, 20V). This property allows a possible slower protection and therefore less sensitive to noise with a lower risk of false detection.

3. Application to HSF and FUL protections

The gate of the MOSFET being in a quasi-flying state ($R_{\text{SLOW}} = 1\text{k}\Omega$) during the ON-state, the aforementioned types of faults show a significant impact on V_{GS} . Their respective simplified signatures are depicted in Fig. 4a.

These gate voltage fluctuations are made detectable by comparing the ON-state V_{GS} to a pair of high (V_{HT}) and low (V_{LT}) thresholds after a blanking time as illustrated in Fig. 4b. The comparison result is then processed and triggers the Soft Shut-Down (SSD) protection.

3.1. HSF and FUL detection

- HSF shorts are characterized by an undesirable turn-on leading to an inverter leg short as shown in Fig. 5b. The MOSFET then saturates under the full bus voltage V_{BUS} . This generates an extreme temperature rise in the chip. The resulting SE leakage current from gate to source decreases V_{GS} through the R_{SLOW} -induced voltage drop (as shown in Fig. 4a in the red colour line).

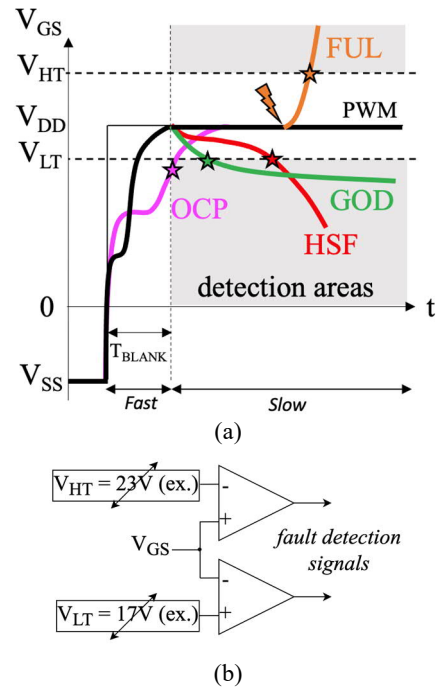


Fig. 4: a) Illustration of different fault signatures on V_{GS} ($T_{\text{BLANK}} = 830\text{ns}$), b) double threshold fault detection principle.

- FUL shorts cause an intense drain current rise through a transistor in its ON-state. In internal FUL, this di/dt is only limited by the switching loop stray inductance and the faulty switch slew rate. Two phenomena arise in favour of a fast detection. The faulty dI_{DS}/dt is passing through the transistor's drain-source ON-state resistance ($R_{\text{DS(ON)}}$) which allows a dV_{DS}/dt to appear across drain and source. The capacitive coupling between C_{GD} and the dv/dt then injects charges from the drain back to the driver, through R_{SLOW} . Meanwhile, the strong di/dt also excites the chip's source stray inductance (L_{S}) resulting in an inductive voltage that increases the gate electrical potential. Both these properties, ohmic and inductive, participate in increasing V_{GS} with a very high dynamic as shown in Fig. 4a in the orange colour line and in Fig 6a.

External FUL (caused by the appearance of an inductive path: motor winding insulation fault for

instance) are similar to internal ones, only the fault dynamics differ.

The phenomena governing HSF and FUL shorts are further explained in [7] by the authors. Based on the protection delay results in HSF mode in Fig. 5c, a compromise between protection speed and robustness is brought out under $R_{SLOW} = 1k\Omega$. This can be solved by increasing R_{SLOW} to further decrease V_{GS} and ensure a fast and robust protection.

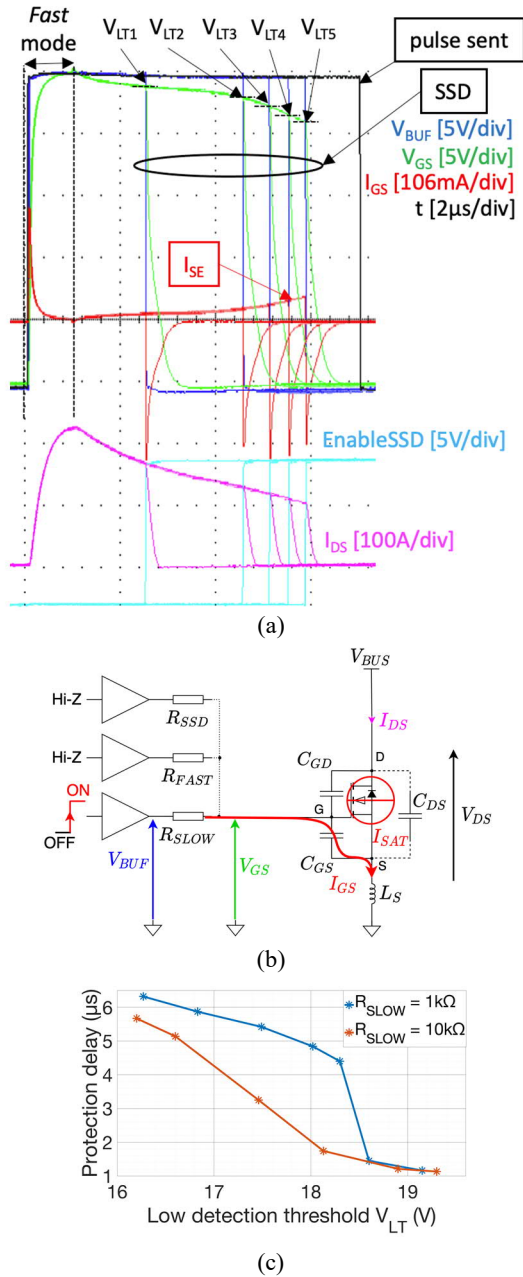


Fig. 5: a) Experimental HSF waveforms for different low detection thresholds V_{LT} , b) HSF equivalent schematic, c) parametric protection delay measured between the faulty turn-on and the activation of the SSD signal.

Using this V_{GS} monitoring architecture, the inverter leg is protected against HSF shorts only 1.2 μ s (15% of $T_{SCW} = 8\mu$ s [10]) after their appearance (Fig. 5c).

According to Fig. 6c, based on FUL mode experimental data, the inverter leg is protected against internal FUL only within 250ns after the fault appearance. A clamp (V_{CLAMP}) is used on the gate so that V_{GS} does not exceed the absolute maximum rating (30V) during FUL events. The clamping strategy is further detailed in [7].

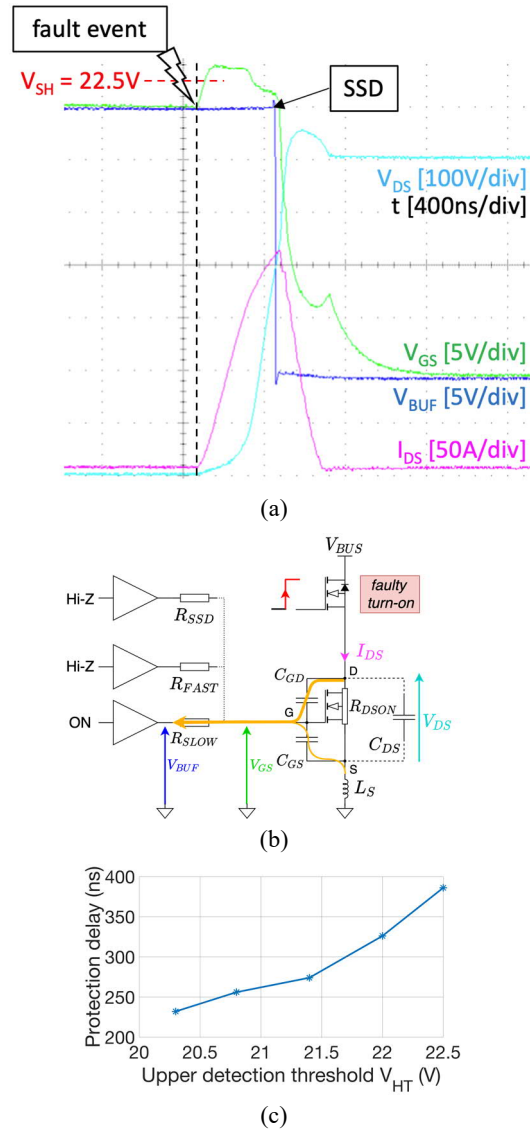


Fig. 6: a) Experimental FUL waveforms, b) internal FUL equivalent schematic, c) protection delay measured between the faulty appearance and the activation of the SSD signal.

The difference in protection times between HSF and FUL modes is attributable to the thermal origin of the signature on V_{GS} of the fault in HSF mode which makes it intrinsically slow. Whereas FUL signatures

on V_{GS} are remarkably faster as they only rely on electrical phenomena.

3.2. Complementarity of high and low-side protections

Now considering the inverter leg as a whole, some interactions arise between high-side and low-side protections.

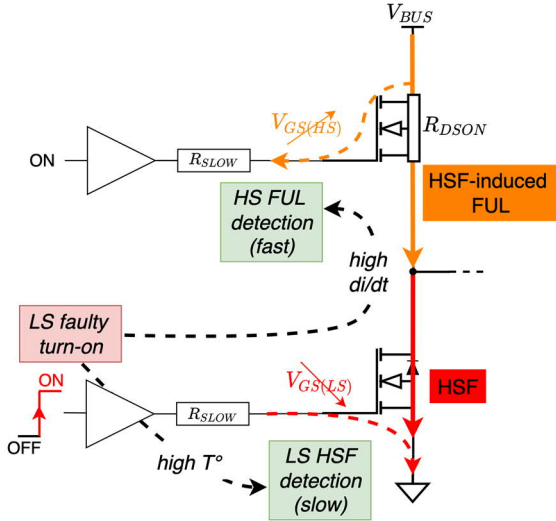


Fig. 7: Illustration of the complementarity of high and low-side protections in an inverter leg configuration.

As depicted in Fig. 7, a HSF event, on the low-side (LS) switch here, causes an extreme current rise in the inverter leg until the LS MOSFET reaches its saturation point. This current is undergone by the complementary switch which makes it detectable by the high-side (HS) protection circuitry. This complementarity either allows the detection of HSF shorts with the same dynamics as FUL shorts in a few hundred nanoseconds or can also allow both protections to operate simultaneously with their respective outputs connected to a logical ‘AND’, confirming each other, to prevent a false triggering of the protection. This property adds a layer of robustness against undesirable detections of HSF shorts.

3.3. FUL double detection: Analysis

Now the impact of a faulty LS turn-on (HSF) on the HS gate voltage is further considered as depicted in Fig. 7. In this case, the HS switch is ON and no current is flowing out of the inverter leg. The fault-induced drain current rise is also seen by the HS switch’s channel. As explained in paragraph 3.1., before the HS switch reaches saturation, its V_{GS} rises (Fig. 8 in the orange colour line) due to the coupling of V_{GS} to the dI_{DS}/dt .

Once the HS switch reaches saturation, the drain current stops rising and the coupling between dI_{DS}/dt and V_{GS} disappears. The HS switch’s V_{DS} also rises. The resulting high power density imposes a strong thermal stress to the chip.

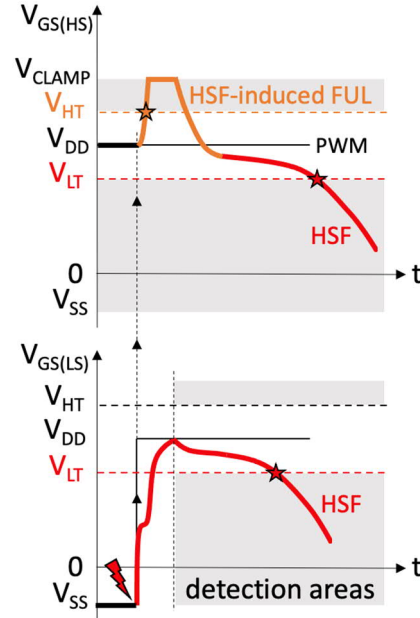


Fig. 8: Simplified illustration of the impact of a low-side HSF short on LS and HS gate voltage waveforms.

The local temperature rise makes V_{GS} drop through the SE leakage current (paragraph 3.1.). This behaviour is reminiscent of the HSF phenomenon. Indeed, an undetected FUL will result in the appearance of a HSF. Both HS and LS transistors are now saturating. Since they share the same gate bias (V_{DD}) and drain current (no load), they are experiencing the same V_{DS} of half the bus voltage as demonstrated in Fig. 9. This advantageous property affords an equal distribution of the thermal stress by halving it on both chips. It then allows a 4-fold increase in T_{SCW} thanks to the quadratic relation of time to the junction temperature elevation as shown in eq. (1), all parameters being defined in [11].

$$\Delta Tj_{max}(t) = \frac{2V_{DS}J_{SAT}}{\rho c \sqrt{\pi \alpha}} \sqrt{t} \quad (1)$$

In sum, with the same gate bias and drain current conditions, a FUL gives way to a symmetrical HSF. While in the presence of a load current, the operating conditions are now asymmetrical between the LS and HS switches. The transistor that drives this current will reach saturation, while the remaining one will stay in its linear region. The thermal stress is now condensed and localized on one chip only.

It is thus demonstrated that a single HSF short is made detectable by three different threshold crossings with V_{LT} and V_{HT} as illustrated in Fig. 8. This property further allows a robust protection against false detections of faults in an inverter leg.

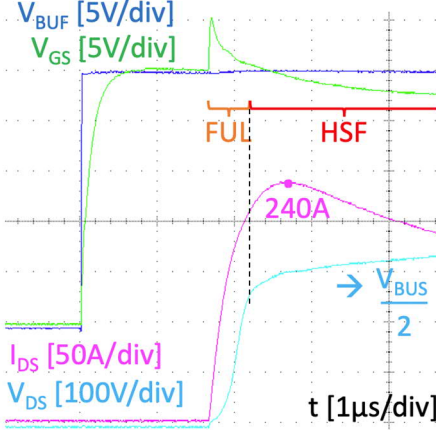


Fig. 9: Highlight of the high-side FUL-HSF sequence subsequently to a low-side HSF.

4. Application to OCP protection

The principle of the OCP protection relies on the correlation between the load current and the gate charge of C_{GS} dynamics. Indeed, in the case of an overload event (Fig. 11a in the yellow colour line), in comparison to a nominal current (Fig. 11a in the green colour line), both the duration and amplitude of the gate Miller plateau voltage are increased.

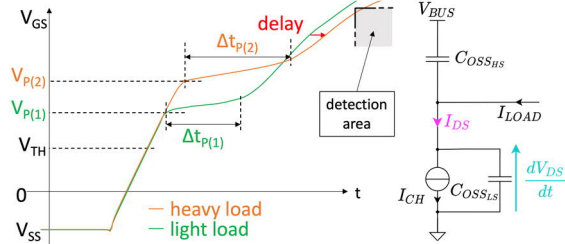


Fig. 10: Simplified illustration of the impact of the load current on V_{GS} dynamics, equivalent schematic.

- In point of fact, in comparison to a no-load turn-on, a higher gate polarisation is required to activate the MOSFET's channel in heavy load conditions. Consequently, the dV_{DS}/dt is slightly delayed as the effective commutation starts at a higher V_{GS} than in a no-load condition as depicted in Fig. 10. The plateau voltage amplitude then increases with the load current as shown in eq. (2).

$$V_P(t) \approx V_{TH} + \frac{I_{LOAD}}{G_{FS}} + \frac{2C_{OSS}}{G_{FS}} \frac{dV_{DS}}{dt} + f(\lambda V_{DS}(t)) \quad (2)$$

With λ representing the temporal oblique evolution of

the plateau voltage (similar to the Early effect in bipolar transistors) and G_{FS} the MOSFET's transconductance. This particular plateau voltage form is due to the specific short-channel effect on SiC MOSFETs.

- An approximate relation between switching speed and load current is described in eq. (3).

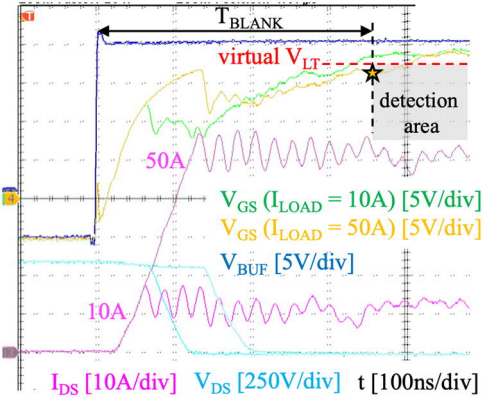
$$\frac{dV_{DS}}{dt} \approx \frac{I_{CH} - I_{LOAD}}{2C_{OSS}} \quad (3)$$

Hence a relation linking the duration of the plateau voltage to the load current in eq. (4).

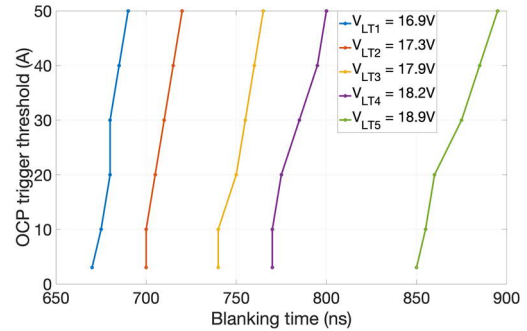
$$\Delta t_P \approx \frac{2C_{OSS}V_{BUS}}{I_{CH} - I_{LOAD}} \quad (4)$$

It appears that the duration of the plateau voltage increases with the load current.

Both these phenomena delay the gate charge and make it possible for V_{GS} to enter the fault detection zone as illustrated in Fig. 4a in the magenta colour and in Fig. 10.



(a)



(b)

Fig. 11: a) Double pulse tests under two different load current levels I_{LOAD} [10A; 50A] - highlight of the OCP principle of detection (detection inhibited), b) experimental parametric results on the impact of the blanking time on the OCP trigger threshold for different V_{LT} ($R_{FAST} = 47\Omega$, $V_{DD} = 20V$, $V_{SS} = -5V$, $V_{BUS} = 600V$).

As shown in Fig. 10, the OCP protection depends on a vertical intersection with the detection area. On the contrary, all other types of fault signatures on V_{GS} enter the detection areas horizontally. This allows a tuning of the OCP trigger level independently of the other protection functions.

5. Application to gate-oxide damage monitoring and detection

Short-circuit stress impose an extreme on-chip power density leading to a strong temperature rise. In the case of Fig. 3a, a power density reduction is provided by the proposed gate-driving architecture, thus allowing to avoid a thermal runaway. The gate region's thermomechanical stress is then the phenomenon governing the chip's main failure mechanism [4][5] should no protection be used or if repetitive shorts are applied [12].

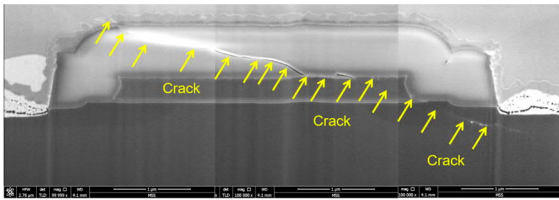


Fig. 12: Dielectric crack between the source metallization and the SiC substrate, through the ILD area (between the aluminium source contact and polysilicium gate contact) and through the gate-oxide region, from [14].

Moreover, to compensate for a decrease in channel carrier mobility in SiC MOSFETs in comparison to their Si counterparts, their SiO_2 gate-oxide layer is processed much thinner (typically 50nm) [13]. The gate-oxide region is thus more mechanically fragile.

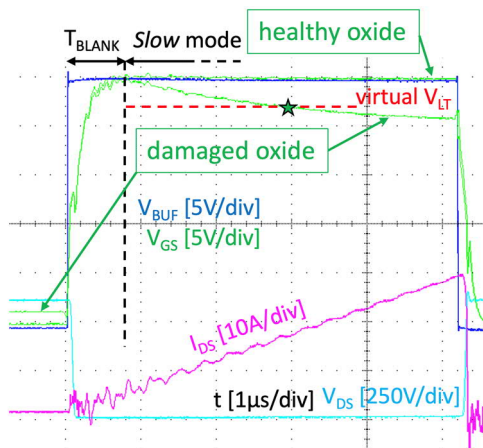


Fig. 13: Experimental highlight of healthy and damaged oxides' impact on V_{GS} ON-state waveform. The DUT with a damaged oxide underwent consequent thermomechanical stress due to several short-circuit and overload tests before the appearance of a significant gate-oxide leakage current.

As illustrated in Fig. 12, a gate damage is clearly shown between the Titanium layer and the Internal Layer Dielectric (ILD). The dielectric crack from the ILD corner to the polysilicium likely proves the low resistance path between gate and source. Such failure leads to a gate-source leakage current made detectable through the enhancing action of R_{SLOW} on V_{GS} (Fig. 13). Even though these cracks may not totally impede the operation of the transistor, they will deteriorate its behaviour and significantly shorten its lifetime.

Fig. 13 proves the detectability of gate-oxide failures due to repetitive thermomechanical stress by comparing the decreasing V_{GS} to a fixed voltage threshold V_{LT} .

5. Conclusion

It was demonstrated that, in extreme operating conditions, SiC power MOSFETs can naturally enter into a safe failure mode characterized by a gate-source short. This mode is accessible and guaranteed using a large gate resistor value, which produces an important fault-induced gate-voltage drop. This voltage drop can now be used to detect the short-circuit before the failure of the device by comparing the ON-state V_{GS} to a fixed threshold reference. The proposed dual-channel gate-driver combines high dynamics during switching events with ON-state fault monitoring through high and low-value switched gate resistors. The proposed multi-functional gate-driving architecture was validated on a short-circuit test power bench and made possible a detection of HSF shorts in 1.2 μs , of FUL shorts in 250ns. Overload events are also detectable and independently tuneable. An integrity monitoring of the MOSFET's gate-oxide, and a detection of its degradation is provided as well. This fault detection gate-driving architecture only relies on low voltage signals, which makes it highly integrable in an IC. Finally, this highly functionalised gate-driving structure could lay the foundations for a smart gate-driver approach.

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