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# Short-Channel Effect Immunity and Current Capability of Sub-0.1-Micron MOSFET's Using a Recessed Channel

Paul-Henri Bricout, *Member, IEEE*, and Emmanuel Dubois, *Member, IEEE*

**Abstract**—Sub-0.1- $\mu\text{m}$  planar and gate recessed MOSFET's are investigated using both drift-diffusion and Monte Carlo simulations. In nonplanar devices, the influence of the gate corner explains that the threshold voltage roll-off can be almost suppressed. A steeper subthreshold slope (low swing) is also obtained for a channel length shorter than 50 nm when the recessed channel MOSFET is compared to its planar counterpart. The influence of the corner effect on high-current performances is also considered in relation with the electric field profile along the Si/SiO<sub>2</sub> interface.

## I. INTRODUCTION

THE search for higher performances of integrated circuits has led to the scaling of MOSFET's down to the 0.1- $\mu\text{m}$  range. The main justification of this miniaturization is the gain in integrability and speed. However, some drawbacks have to be considered: short-channel effects may affect the electrical performances, and hot carrier phenomena are critical in terms of device degradation. Improved current drive capabilities and low parasitic resistances and capacitances are also crucial issues for the speed performances of MOS devices. Large efforts are currently devoted to face the difficulties associated with deep submicrometer dimensions. The optimization is guided by rules derived from scaling laws, and by the some technological considerations, as follows:

- 1) The decreasing of device dimensions causes the so-called short-channel effects: threshold voltage roll-off and degradation of the subthreshold slope, that in turn increases the off-current level and power dissipation.
- 2) The gate oxide thickness has to be reduced in concert with other dimensions. There is, however, a limit imposed by direct tunnelling and technical constraint, which is commonly estimated as about 30 to 35 Å [1].
- 3) The gate induced drain leakage, which is a band-to-band tunnelling current due to the vertical electric field in the gate-drain overlap region gives a limit to the electric field and therefore to the bias voltages.
- 4) The reduction of the junction depth is also prescribed by usual scaling laws [3]. Shallow junction with a weak lateral spreading are desirable for the control of short-channel effects while the source and drain resistances

must be kept as low as possible. However, practical realizations are limited by the present technological possibilities, and for conventional MOSFET's, a trade-off is necessary between the search for very shallow junctions and degradation of access resistances.

- 5) Hot carrier phenomena are related to high electric field. Thus, the reduction of the supply voltage as prescribed in a full scaling law may significantly reduce such effects [4]. Various studies have shown that decreasing both channel length and supply voltage allows for a reduction of the electron energy. This should increase the hot electron reliability.
- 6) As supply voltage is lowered, the threshold voltage must be reduced too in order to preserve an appropriate gate voltage overdrive, but its value has to be strictly controlled to preserve the noise margins and to limit off leakage current.
- 7) The current drive capabilities are altered by some phenomena such as the mobility reduction induced by high doping levels. A way to improve the current performances could be the use of the velocity overshoot effect [5]. Velocity overshoot is obtained when a strong lateral electric field is present in the channel, due to the drain source voltage. The drawback is that short-channel effects could also increase because of the influence of the drain in the channel region even at low bias.
- 8) The geometry of the device retained for the scaling of MOSFET down to the 0.1- $\mu\text{m}$  range should not require too many additional and expensive process steps. This eliminates, for the moment, original structures as gate-all-around transistors [2], [6], although very good performances in term of short-channel effects and current drive capabilities were demonstrated, due to the excellent control of the gate on the channel.

A solution proposed to reduce the lateral extension of the drain influence toward the channel is to modify the device geometry. In a review of the technology requirements for sub-0.1- $\mu\text{m}$  MOSFET's, Fiegna *et al.* [2] studied different conventional structures with uniform, buried or epitaxial channel and also single and double gate SOI devices, but overlooked the investigation of structures with elevated source and drain. These device architectures have recently attracted much attention for their low sensitivity to the short-channel effects [7]–[11]. In this paper, a comparison of the grooved-

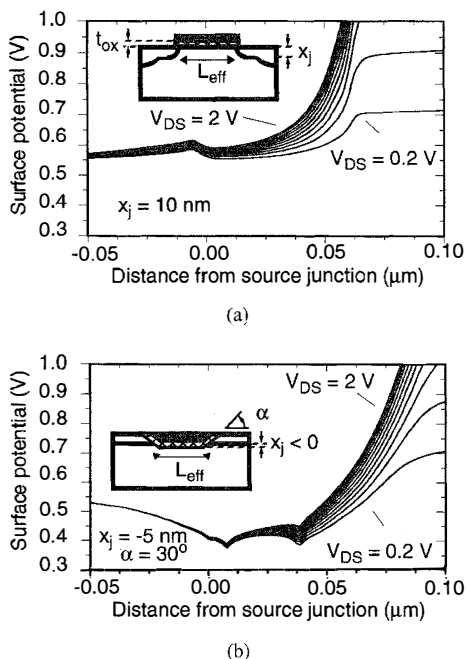


Fig. 1. Surface potential along the Si/SiO<sub>2</sub> interface for (a) planar and (b) recessed devices.  $t_{\text{ox}} = 2.8$  nm,  $N_{\text{sub}} = 2 \cdot 10^{17}$  cm<sup>-3</sup>,  $V_{\text{GS}} = V_{\text{TH}}$ .

gate MOSFET with its conventional planar counterpart has been carried out using both drift-diffusion and Monte Carlo simulations [12]–[14]. The simulated transistors are described in the Section II, as well as the main points related to the simulation methods. Section III gives a detailed discussion on the respective advantages of planar and recessed channel MOSFET's from the short-channel effects and current capabilities viewpoint.

## II. DEVICE STRUCTURES AND SIMULATION TOOLS

### A. Device Geometry

The simulated devices are described by the schematic cross section in Fig. 1. The gate oxide thickness is denoted  $t_{\text{ox}}$ , for both devices. The effective channel length  $L_{\text{eff}}$  corresponds here to the metallurgical channel length, taken along the gate oxide. For the conventional planar nMOSFET, an LDD like structure is used. A double ion implantation is used for the formation of a shallow junction near the channel region, and thicker source and drain diffusion toward the contacts, thus limiting the access resistances. The maximum concentrations at the surface are  $10^{20}$  cm<sup>-3</sup> for the main source and drain implantations and  $10^{19}$  cm<sup>-3</sup> for the extensions. The junction depth  $x_j$  is about 10 nm, which is close to the present state of the art [15]. For the nonplanar device, the junction depth may be positive or negative as the Si/SiO<sub>2</sub> interface is higher or lower than the junction. The sharpness of the corner is described by the angle  $\alpha$  between the horizontal and oblique parts of the interface. Maximum concentration in the source and drain region of the recessed structure is also  $10^{20}$  cm<sup>-3</sup>.

### B. Simulation Methods

For the well-known drift-diffusion method, carriers are considered in equilibrium with the semiconductor crystal, allowing a very robust and fast resolution. This method gives an accurate evaluation of device performances as far as carriers heating is negligible. Drift-diffusion simulations can thus be used to simulate the subthreshold behavior and extract the threshold voltage for low  $V_{\text{DS}}$  bias. As the drain voltage increases, drift-diffusion models may only give a qualitative insight into the electrical performances, as hot electron phenomena are ignored. A now widely used tool for simulation of high-biased devices is the Monte Carlo method, that includes the electron heating and related phenomena such as velocity overshoot and transconductance higher than predicted by saturation models. The Monte Carlo program developed in our laboratory [14] is compatible with the drift-diffusion device simulator IMPACT [16] as they use the same description of the device in terms of mesh and concentrations. The result of a drift-diffusion simulation is used as a starting point for Monte Carlo calculations, allowing a faster procedure. For the electron energy band structure and the scattering processes, the models and values proposed in references [17] are used. Interactions of electrons with the interface are considered either as specular collisions or diffusions: the energy is preserved and the direction of the velocity is either reflected against the interface following usual reflection laws or randomly selected. Both simulation tools have been used to compare conventional bulk transistors and nonplanar devices.

## III. RESULTS AND DISCUSSION

### A. Corner Effect

The threshold voltage is defined for long-channel MOSFET's as the gate voltage that causes the channel inversion and then enables conduction. For short devices, the channel depletion region is influenced by source-bulk and drain-bulk junctions. The threshold voltage then depends on geometrical parameters such as effective length and junction shape. For simplicity, we denote  $V_{\text{TH}}$  the gate to source voltage that allows a source to drain current of 10 nA in a 1- $\mu\text{m}$ -wide device.

The benefits of the recessed structure in terms of short-channel effects are mainly due to the potential barrier generated at the gate corners, as pointed in [10], [16]. This is illustrated by Fig. 1, in which the surface potential is plotted along the Si/SiO<sub>2</sub> interface. For the planar MOSFET, the potential is strongly perturbed by the drain voltage and the potential barrier is removed in the channel region, in contrast to the grooved channel device for which the potential barrier is only slightly affected in the drain region. Thus, the corner effect acts against the DIBL effect.

### B. Short-Channel Effects Through Low Bias Simulations

An accurate knowledge of the evolution of the threshold voltage and of the subthreshold slope  $S$  with the channel length reduction is essential for device optimization. As this

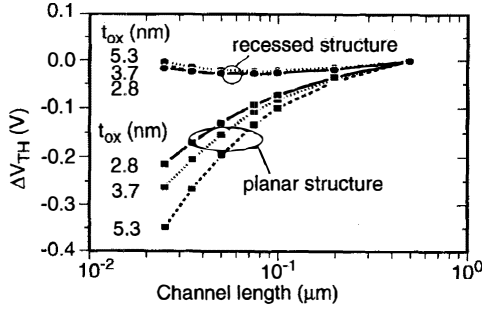


Fig. 2. Threshold voltage roll-off at low drain bias.  $V_{DS} = 0.1$  V,  $N_{sub} = 2 \cdot 10^{17}$   $\text{cm}^{-3}$ . Recessed structure:  $x_j = -5$  nm,  $\alpha = 30^\circ$ .

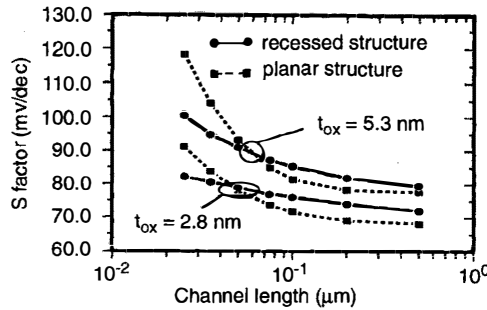


Fig. 3. Evolution of the subthreshold swing with the effective channel length.  $V_{DS} = 0.1$  V,  $N_{sub} = 2 \cdot 10^{17}$   $\text{cm}^{-3}$ . Recessed structure:  $x_j = -5$  nm,  $\alpha = 30^\circ$ .

part of the study is limited to low bias condition, classical drift-diffusion simulations are used. Different device geometries have been simulated, and it has been found that the best recessed structure has a very small junction depth and a moderate interface slope [12]. Then, the simulations have been carried out with  $\alpha = 30^\circ$  and a junction depth close to zero:  $x_j = 0$  nm or  $x_j = -5$  nm. As reported in Fig. 2, threshold voltage roll-off is clearly present for the planar device, due to the influence of the drain-bulk junction on the channel region. On the contrary, the recessed structure nearly keeps the same threshold voltage for all simulated channel lengths, for any gate oxide thickness. The threshold voltage even increases as the channel length is reduced. This behavior is attributed to a “coupling” of the potential barriers created at both corners of the gate, which slightly increases the total barrier between source and drain as the  $U$  grooved channel converts into a  $V$  grooved channel [12]. Another parameter affected by the length reduction is the subthreshold swing. In a “long channel” approximation, it is expressed as

$$S \approx \frac{k_B T}{q} \ln(10) \left( 1 + \frac{C_D}{C_{ox}} \right) \quad (1)$$

where  $C_D$  and  $C_{ox}$  are, respectively, depletion and oxide capacitances. For a geometrical reason, the average value of  $C_{ox}$  is inferior in the recessed device than in the planar one. This should give a better (lower)  $S$  factor to the planar structure. Fig. 3 confirms this interpretation for a long planar

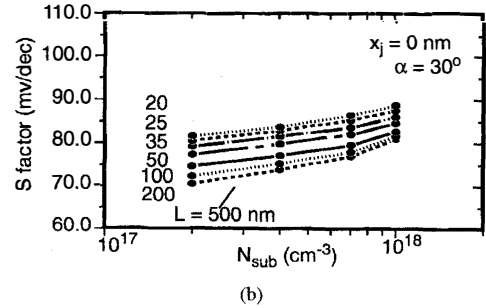
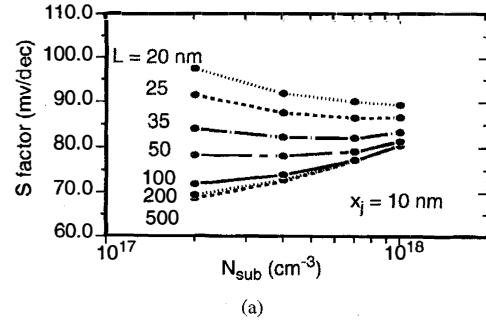


Fig. 4. Evolution of the subthreshold swing with the substrate concentration.  $V_{DS} = 0.1$  V,  $t_{ox} = 12.8$  nm: (a) planar and (b) recessed structure.

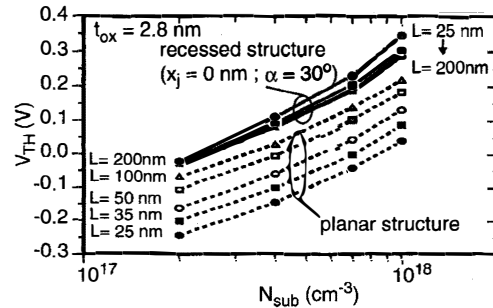


Fig. 5. Threshold voltage as a function of the substrate concentration,  $V_{DS} = 0.1$  V.

device. However for devices shorter than 50 nm, the situation is reversed:  $S$  factor is less degraded in the recessed structure. It is thus possible, with a nonplanar device to obtain both advantages in the limit of very short channels: i.e., nearly no roll-off and a slow increase of the subthreshold swing. Fig. 4 presents the influence of the bulk doping level. Following relation (1), the depletion capacitance  $C_D$  and the  $S$  factor increase with the doping concentration. This behavior is observed for the longest planar structures ( $L > 100$  nm). However, for devices shorter than 50 nm, the subthreshold slope deviates from its long-channel expression:  $S$  decreases as the doping level raises, due to short-channel effects. On the contrary, the recessed MOSFET's always exhibit the same “long channel” behavior. This allows for the preservation of a reasonable subthreshold characteristic with a moderate substrate doping. The doping level has to be determined in relation with the desired threshold voltage, as pointed by Fig. 5. As mentioned above, the threshold voltage does not depend on the channel length for recessed structure, and unlike fully-depleted SOI

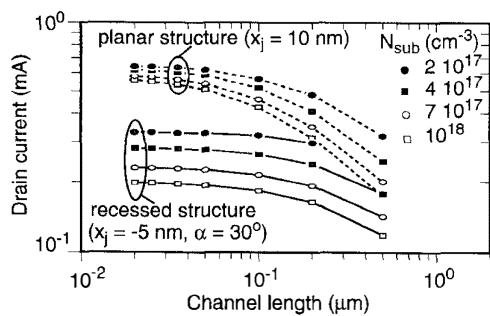


Fig. 6. Saturation current for  $V_{DS} = V_G - V_{TH} = 1.2$  V,  $t_{ox} = 2.8$  nm.

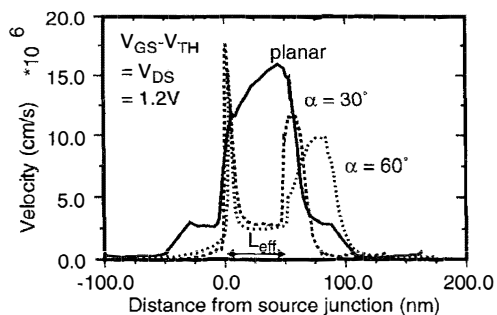


Fig. 7. Mean velocity along the Si/SiO<sub>2</sub> interface,  $N_{sub} = 2 \cdot 10^{17}$  cm<sup>-3</sup>,  $x_j = 10$  nm for planar and  $x_j = 0$  nm for recessed devices.

structures [6],  $V_{TH}$  may still be adjusted according to the bulk doping concentration.

### C. High-Bias Simulations

With the reduction of dimensions, short-channel effects and subthreshold behavior have to be strictly controlled, as mentioned in the previous part. Another aspect of the optimization concerns the high-current performances. The qualitative evolution of the drain current in the saturation region with a constant gate voltage overdrive ( $V_G - V_{TH} = V_{DS} = 1.2$  V) is presented on Fig. 6, from drift-diffusion simulations. Although drift-diffusion model is not accurate for very short devices, it is clearly observed that the maximum saturation current in nonplanar devices is roughly reduced by a factor 2 with respect to its planar counterpart. However, as the threshold voltage is better controlled in recessed structures, this difference may be partially compensated by the use of a lower doping level in the bulk, while keeping equivalent noise margins. Monte Carlo simulations, including nonstationary transport, give more details about the electrical behavior of the different devices and about the main limitation on current. In Fig. 7, mean electron velocity is plotted along the Si/SiO<sub>2</sub> interface of three different structures. For the planar device, nonequilibrium transport occurs in all the channel region and in the drain, as indicated by velocity peaks. On the contrary, nonstationary transport in recessed MOSFET's is only observed near the oxide corners, essentially in the drain region. The magnitude of nonstationary phenomena is small in the channel, and in general, lower than the ones present in the corresponding planar structure. This is a positive point

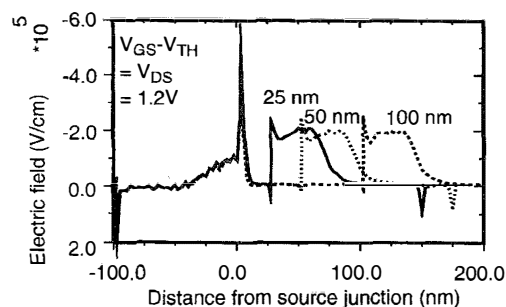


Fig. 8. Electric field parallel to the Si/SiO<sub>2</sub> interface,  $N_{sub} = 2 \cdot 10^{17}$  cm<sup>-3</sup>,  $x_j = 0$  nm,  $\alpha = 30^\circ$ .

concerning hot carrier phenomena and reliability. In order to better understand the mechanism involved in the current limitation, Fig. 8 reports the electric field profiles for different channel lengths of the optimized recessed structure. In the channel region, the lateral field is screened by the corner effect and its magnitude is low. Conversely, a large and narrow peak of electric field is present at the source oxide corner while its magnitude and shape on the drain side remain unchanged, but are simply translated according to the device length. This means that the electric field and, thus, the transport properties are totally controlled by the oxide/channel geometry. For optimization, a compromise has to be found between the tight control of short-channel effects and subthreshold slope allowed by the corner effect and the high-current performances associated with velocity overshoot, that are available in planar structures.

## IV. CONCLUSION

Device simulations using classical drift-diffusion formalism and Monte Carlo method can explain the behavior of grooved MOSFET's. Due to the corner effect, short-channel effects can be suppressed by an appropriate geometry of the interface, while the threshold voltage is still determined by adjusting the bulk doping level. The main drawback of the corner effect for high-speed applications is the reduction of the maximum saturation current. However, this restriction on current can be traded-off with the suppression of short-channel effects for high-density applications (e.g., memories) in which low-power operation is required. Otherwise, for equal noise margins, it is possible to use a lower concentration than in conventional planar devices. Thus, the degradation of the current drive capability is limited. On the other hand, the nonequilibrium transport is mainly located in the drain region. This means that the magnitude of hot carrier phenomena should be reduced compared to planar MOSFET's.

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Since 1989, he has been engaged in ISEN tutorial courses on integrated circuit design. In 1992, he was Visiting Scientist at the IBM T. J. Watson Research Center, Yorktown Heights, NY, working on characterization and simulation of submicron SOI-MOSFET's. In October 1993, he joined CNRS (IEMN/ISEN Laboratories), where he is currently head of a group involved in device physics, device simulation, analog circuit simulation, and exploratory device fabrication using scanning probe microscopy (SPM) techniques.