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# Over-Voltage and Cross-Conduction Hard Switching Stress on Schottky Gate-Type p-GaN HEMT in Half-Bridge Operation Experimental and Physical Approaches

L. Ghizzo<sup>a,b,c\*</sup>, D. Trémouilles<sup>c</sup>, F. Richardeau<sup>b</sup>, S. Vinnac<sup>b</sup>,  
F. Jamin<sup>a</sup>, G. Guibaud<sup>a</sup>

<sup>a</sup> THALES SIX France SAS, Toulouse, France

<sup>b</sup> LAPLACE University of Toulouse, CNRS, INPT, UPS, Toulouse, France

<sup>c</sup> LAAS-CNRS, University of Toulouse, CNRS, Toulouse, France

## Abstract

The GaN HEMT power device emerges as a promising wide-bandgap component for obtaining ultra-compact and very high efficiency power converters. Nevertheless, its long-time switching operation capability in high overload regimes near or just above its maximum ratings remains unknown. The physical degradation mechanisms specific to GaN HEMT as well as the associated electrical signatures must now be established and better understood. In this article a stress protocol is proposed combining or not functional drain-source over-voltage switching and transient low dead-time cross-conduction stresses. A no-loaded Half Bridge (HB) is used. All stress parameters studied have been associated to electric changes such as drain-source, gate-source leakage currents, and threshold voltage drifts of intrinsic values and even some physical degradation by LIT compound analysis. After analysis, it appears that both the electric field and the current are very stressful for the devices and lead to current leakage caused by physical degradation. The aging observed might be generated from the injection of hot electrons and located depending upon the drain voltage value which influences the depletion region and thus the electric field peak.

## 1. Introduction

The HEMT GaN transistor has several advantages over its silicon counterpart in power applications where high efficiency, high power density, and high frequency are important. However, its functional reliability is still a concern for some even though significant results have been obtained in hard switching regimes in [1][2]. To extend the functional reliability of the p-GaN HEMT from a use within its nominal ratings to overload regimes (near or just above its maximum ratings), a no-loaded half-bridge inverter topology is considered in this study. In addition to the  $V_{DS}$  over-voltage stress, the 2DEG switching energy stress applied through  $C_{OSS}$  discharge can be greatly intensified using a small dead-time value and therefore leading to an additional cross-conduction stress. The effect of the over-voltage magnitude (120% of the bus voltage  $V_{dc}$ ) under hard-switching is studied in correlation with the cross conduction stress. Intrinsic values ( $C_{RSS}$ ,  $C_{OSS}$ ,  $C_{ISS}$ ,  $I_{GSS}$ ,  $I_{DSS}$ ,  $V_{th}$ , etc.) are monitored to understand the electrical phenomena responsible for the aging in each case. This paper presents the no-load half-bridge and cross conduction test setup, the drift of device's intrinsic values and gives a possible explanation based on

experimental results and physical mechanisms analysis.

## 2. Experimental details

The device under test (DUT) is a commercial, 100V, 90A, 7m $\Omega$  packaged p-GaN gate AlGaIn/GaN HEMT. 26 devices were installed on 13 half-bridges integrated on dedicated daughter Printed Circuit Boards (PCBs) which were developed and used for the proposed stress as illustrated in Fig.1(a) and (b) and plugged-in on a main power motherboard including its FPGA-based control set as illustrated in Fig.1(c). Results presented in this paper are based on a stress duration of 35 hours (7 hours/day). Characterization measurements are performed with a Keysight™ B1505A power device analyzer/curve tracer.

N.	P.	$V_{DC}$	$T_d$	$(R_{G,ON} ; R_{G,OFF})$	cross cond.
#1, #2, #3		120 V	30 ns	(10 $\Omega$ ; 50 $\Omega$ )	yes ; hard sw
#4, #5		120 V	120 ns	(10 $\Omega$ ; 50 $\Omega$ )	no ; soft sw
#6, #8		67 V	120 ns	(10 $\Omega$ ; 50 $\Omega$ )	no ; soft sw
#9, #10		67 V	20 ns	(10 $\Omega$ ; 50 $\Omega$ )	yes ; hard sw
#7, #11		67 V	120 ns	(10 $\Omega$ ; 2 $\Omega$ )	no ; soft sw
#12, #13		67 V	N/A	N/A	no ; DC stress

Table 1: Table of the stress parameters (P) applied to each couple of transistors of the daughterboard number (#N).

\* Corresponding author. lucien.ghizzo@gmail.com

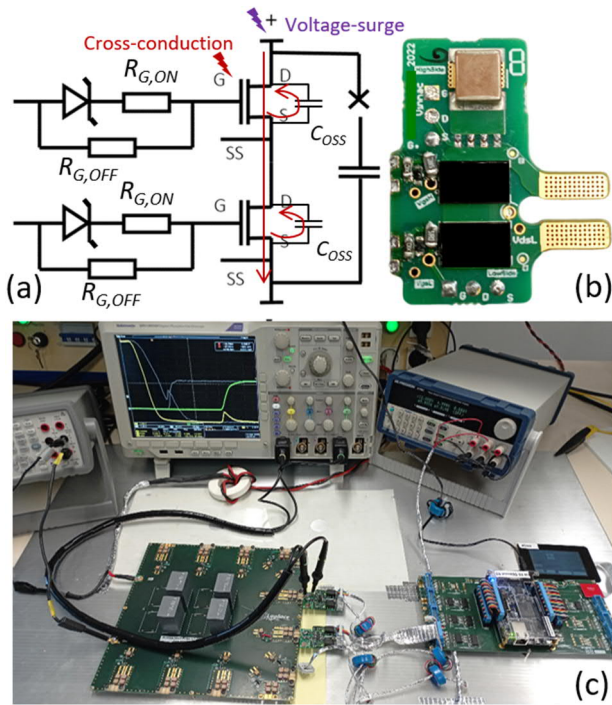


Figure 1: (a) Schematic of the half bridge daughterboard composed of a decoupling ceramic capacitor connected to two HEMTs, one high-side and one low-side, and their gate control circuit with gate resistors  $R_{G,ON}$  and  $R_{G,OFF}$ . The capacitor can be easily disconnected to perform characterization measurements (b) daughterboard. (c) Test bench composed of the main motherboard (12 legs in parallel) and 2 daughterboards. Gate driver boards are connected to feed gate voltages by a FPGA board with a user interface where stress parameters can be selected.

The switching frequency  $F_{sw}$  is set to 2kHz, this very low value allows to avoid heating up the components during the stress to only focus on electrical stress and not consider the thermal stress that could complicate the interpretation. A higher switching frequency will degrade more rapidly the DUTs and can change the degradation mechanisms with the temperature stress added. This stress will be studied with a very precise monitoring of temperature in a future study. The absence of load leads to negligible losses (25mW/transistor at 2kHz) and makes it unnecessary to add a heatsink. With a nominal dead-time of typically 120ns, the 2DEG is only activated by the controlled transistor during the discharge of its  $C_{OSS}$  and to recharge the opposite transistor's  $C_{OSS}$  under  $V_{dc}$  with a high  $dv/dt$  and low losses. Now considering a low dead-time ( $T_d$ ) value, a cross-conduction arises quickly over a few nanoseconds and exhibits a 2DEG through the two transistors with a lower  $dv/dt$  extra losses, as explained hereafter.

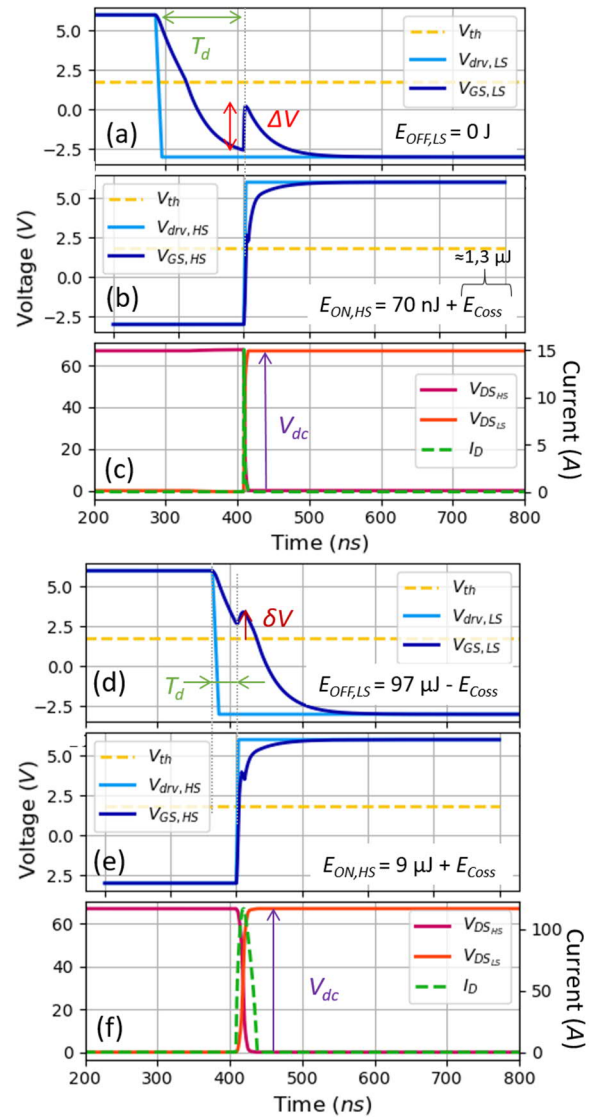


Figure 2: (a) LTspice simulated waveforms of the driver voltage  $V_{drv}$  and gate voltage  $V_{GS}$  at the turn-off of the LS transistor. (b) driver voltage  $V_{drv}$  and gate voltage  $V_{GS}$  at the turn-on of the HS transistor, the threshold voltage  $V_{th}$  is in dashed line. (c) LS and HS transistors'  $V_{DS}$  and drain current. (d)  $V_{drv}$ ,  $V_{GS}$  at the turn-off of the LS transistor with a small  $T_d$  that generates cross-conduction. (e) driver voltage  $V_{drv}$  and gate voltage  $V_{GS}$  at the turn-on of the HS transistor, (e) LS and HS transistors'  $V_{DS}$  and drain current (multiplied by 10) in the case of cross-conduction.

The waveforms of Fig.2 illustrate the main parameters of interest. All stress parameters are matched to their respective daughterboards' numbers in table 1. Two main stress parameters are studied. The switched voltage  $V_{dc}$ , on the transistors of boards #4 and #5 for  $V_{dc}$  chosen voluntarily high (120 % of the rating) and on boards #7 and #11 for a smaller value ( $V_{dc} = 67V$ : 2/3 of the rating). The cross-conduction will be studied (with a small  $T_d$  and high  $R_{G,OFF}$ ) on boards #1,#2,#3 for a high  $V_{dc}$  value and

on #9 and #10 for a smaller value. When the LS transistor is off, the turn-on of the HS transistor through the small  $R_{G,ON}$  produces a strong positive  $dv/dt$  on the LS drain. The negative  $dv/dt$  applied to the  $C_{GD}$  of the LS transistor generates a current peak from the gate to the driver through  $R_{G,OFF}$  that induces the spike  $\Delta V$  in Fig.2(a). A high  $R_{G,OFF}$  value of  $50\Omega$  produces a large  $V_{GS}$  spike and combined with a short  $T_d$  it generates a cross-conduction phenomenon. In fact, if  $T_d \approx 20 - 30ns$ , the spike will appear earlier on the decreasing slope of  $V_{GS}$  at the turn-off, and could exceed the threshold voltage [3]. The active turn-on of one transistor forces the re-triggering on the opposite transistor that is turning off (or that has just turned off), as shown in Fig.2(d)(e)(f). For the duration of the spike ( $\approx 10$  to  $20ns$ ) LS and HS 2DEGs are simultaneously fully activated and a significant current flows through both channels under a smaller  $dv/dt$  than in a long dead-time case ( $26$  kV/ $\mu s$  without cross-conduction and  $11$  kV/ $\mu s$  with cross-conduction). Indeed, as illustrated in Fig. 2(d) the extra 2DEG formed in the LS transistor can be assimilated to a transient load subtracted from the active HS 2DEG and therefore reducing the resulting current injected into  $C_{OSS}$  across LS and HS devices. The energy at turn-on  $E_{turn-on}$  is then increased ( $\times 10$ ) with an additional cross-conduction energy  $E_{cross-cond}$  and more stressful and could be expressed as [4][5]:

$$E_{turn-on} = V_{dc}Q_{C_{oss}} + E_{cross-cond} \quad (1)$$

The turn-on energy with cross-conduction is four times higher than the one in the case of a  $400\mu H$  ( $\approx 40A$ ) Half-Bridge without cross-conduction. Boards #6,#7,#8 and #11 will serve as references for the stress applied on the other boards. A DC voltage of  $67V$  was applied on the transistors of #12 and #13 for 35h at off state ( $V_{GS} = -3V$ ) to compare with dynamic stress as well.

### 3. Drift and degradation after the stresses applied to the transistors.

#### 3.1. Experimental results

The comparison between the characterization measurements at  $t_0$  (before stress) and  $t_{35h}$  (after a stress duration of 35 hours, 7h/day) shows some irreversible degradation and drifts of electrical characteristics as highlighted in Fig.3,4,5,6. Initial curves at  $t_0$  are displayed in cool colors (blue, green, violet) and after stress in warm colors (orange, red and brown). Forward and backward sweeps are performed to take into account a possible hysteresis. The results of the high voltage stress are shown first and the low voltage stress results are shown next. The influence of cross-conduction is shown in each case.

#### High voltage stress, no cross-conduction

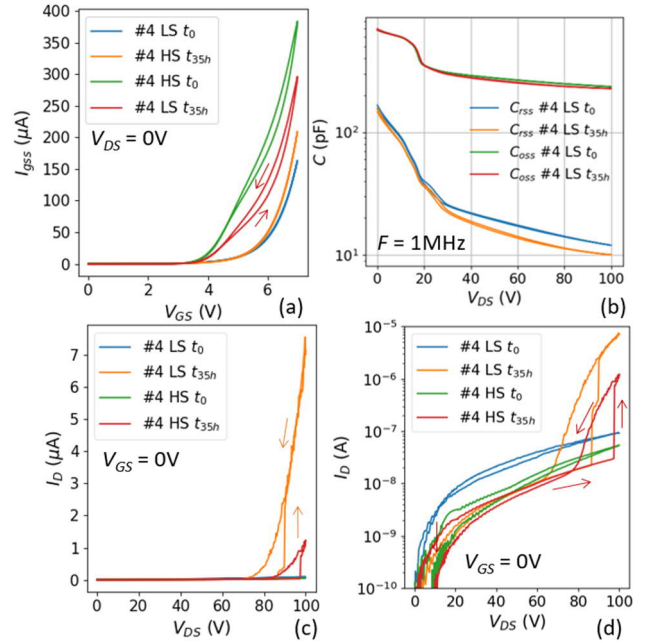


Figure 3: Characterization of the stress board #4 before ( $t_0$ ) and after 35 hours of stress ( $t_{35h}$ ) at 120V with no cross-conduction ( $T_d = 120ns$ ). (a) Gate leakage current  $I_{gss} = f(V_{GS})$  at  $V_{DS} = 0V$ . (b)  $C_{rss}$  and  $C_{oss}$  under  $V_{DS}$  at  $F = 1$  MHz. (c) Drain leakage current  $I_{DSS} = f(V_{DS})$  at  $V_{GS} = 0V$ . (d) Display of (c) with log scale. The main degradation to observe is the high drain source leakage current that appears around  $V_{DS} = 90V$  for LS and  $V_{DS} = 98V$  for HS.

The transistors of boards #4 and #5 were stressed on the drain with a switched voltage of 120% of their rating (i.e.  $V_{dc} = 120V$ ). The irreversible degradation is visible on both transistors of board #4 as shown in Fig.3(c) on the drain leakage  $I_{DSS} = f(V_{DS})$ . This degradation is visible starting at  $V_{DS} = 90V$  for the LS, and around  $V_{DS} = 98V$  for the HS. It is characterized by a steep increase of the drain leakage current. Below this voltage, the leakage current mainly overlaps with the curve at  $t_0$  and the drain leakage is around  $10nA$  at this voltage. When  $V_{DS}$  is reduced again (backward sweep), the leakage current gets back to a normal value as in the forward sweep as shown in Fig.3(d). This leakage current seems to be between drain and source, as the gate current during this measurement is not changed (similar curves to  $I_{DSS}$  of board #2 in Fig.3(a)).



### High voltage stress with cross-conduction

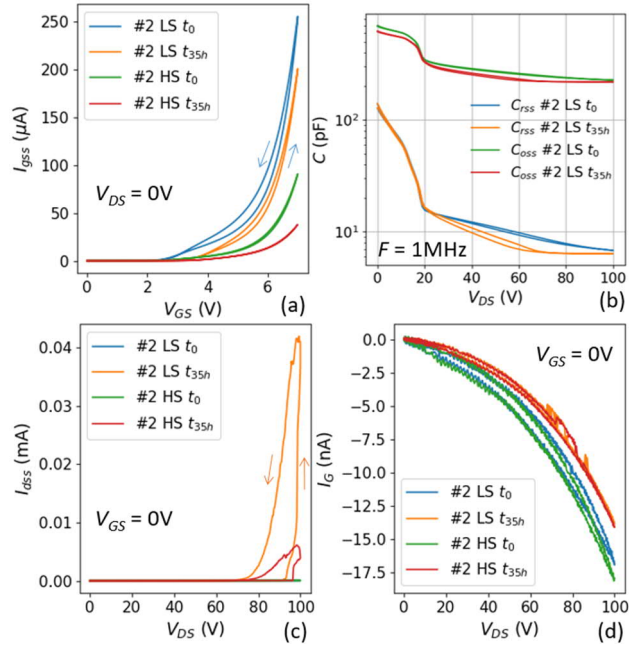


Figure 4: Characterization of board #2 before ( $t_0$ ) and after ( $t_{35h}$ ) stress at 120V with cross-conduction ( $T_d = 30ns$ ). (a) Gate leakage current  $I_{gss} = f(V_{GS})$  (b)  $C_{rss}$  and  $C_{oss}$ . (c) Drain leakage current  $I_{dss} = f(V_{DS})$  at  $V_{GS} = 0V$ . (d) Gate current during the  $I_{dss}$  measurement depicted in (c). The main degradation to observe is the high drain-source leakage current that appears after a threshold voltage for around  $V_{DS} = 95V$  for the LS and  $V_{DS} = 97V$  for the HS.

The devices of boards #2 and #3 were also stressed under  $V_{dc} = 120V$  (like boards #4 and #5) with an additional cross-conduction phenomenon. They also exhibit a change of the drain current leakage above 80V but stronger than in the previous cases. This leakage can reach the mA range. The capacitance  $C_{GD} = C_{rss}$  has significantly changed in this case and becomes constant just before or near the abnormal current leakage.

### Low voltage stress with cross-conduction

To evaluate the impact of cross-conduction alone, a stress under  $V_{DS} = 67V$  (2/3 of the voltage rating) with a short deadtime of 20ns is conducted on boards #9 and #10. The degradation of the HS transistors identified by a high leakage current between gate and drain is depicted in Fig.5(c) and (d). The capacitance  $C_{rss}$  knee's drift to higher voltage (Fig.5(b)) and the gate leakage current  $I_{gss} = f(V_{GS})$  tends to increase especially at low voltage (Fig.5(a)). The LS switches exhibit the same degradation patterns, yet in a less pronounced manner. The devices of board #1 that underwent cross-conduction at higher  $V_{DS}$  share the same degradation patterns on  $I_{gss}$  between  $t_0$  and  $t_{35h}$  in addition to a constant  $C_{rss}$  starting at 60V. The  $I_{dss}$  curve has both

the electrical changes observed before: a gate drain leakage current and a steeper increase of the drain-source leakage current above  $V_{DS} = 90V$ .

### Low voltage stress, no cross-conduction

The transistors of the other boards #7,#11,#6,#8 tested under a  $V_{dc}$  voltage within the ratings and no cross-conduction show a similar change but less significant than the low voltage cross-conduction case (see Fig. 7 for #8). A high gate-drain leakage current also appears and the  $C_{rss}$  knee is shifted to higher  $V_{DS}$  values for all transistors. The stress was done with a smaller  $R_{G,OFF}$  value for #7 and #11 in order to reduce the switching energy but no change has been observed compared to transistors #6 and #8.

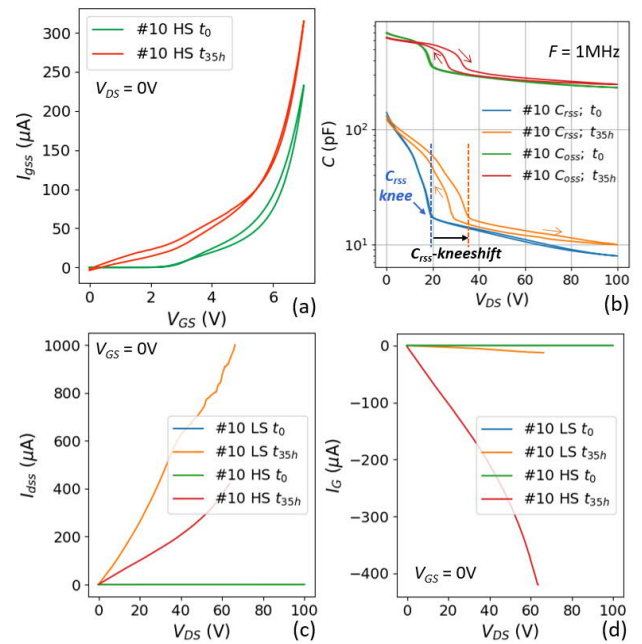


Figure 5: Characterization of the stress board #10 before ( $t_0$ ) and after 35hours of stress ( $t_{35h}$ ) under 67V with cross-conduction ( $T_d = 20ns$ ). (a) Gate leakage current  $I_{gss} = f(V_{GS})$ . (b)  $C_{rss}$  and  $C_{oss}$ . (c) Drain leakage current  $I_{dss} = f(V_{DS})$ . (d) Gate current during the  $I_{dss}$  measurement. The main degradation to observe is the drain-source high leakage current that appears for LS and the gate-drain leakage current for HS.

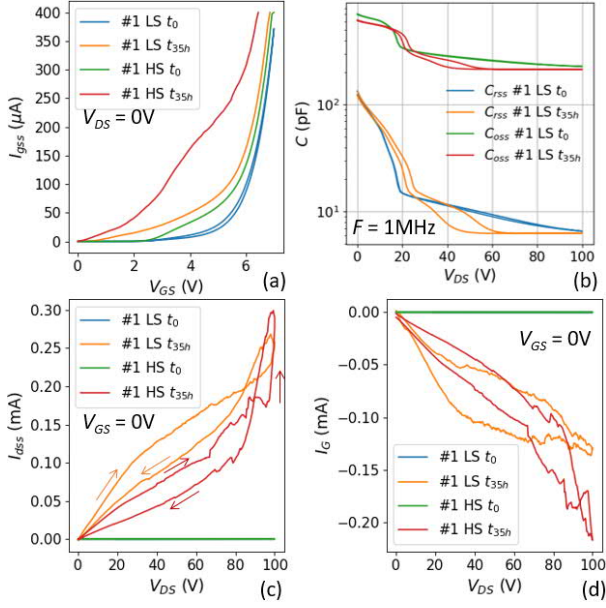


Figure 6: Characterization of the stress board 1 before ( $t_0$ ) and after 35hours of stress ( $t_{35h}$ ) under 120V with cross-conduction ( $T_d = 30ns$ ). (a) Gate leakage current  $I_{gss} = f(V_{GS})$ . (b)  $C_{rss}$  and  $C_{oss}$ . (c) Drain leakage current  $I_{dss} = f(V_{DS})$  at  $V_{GS} = 0V$ . (d) Gate current during the measurement depicted on (c). The main degradation to observe is the gate to drain short on (c) and (d).

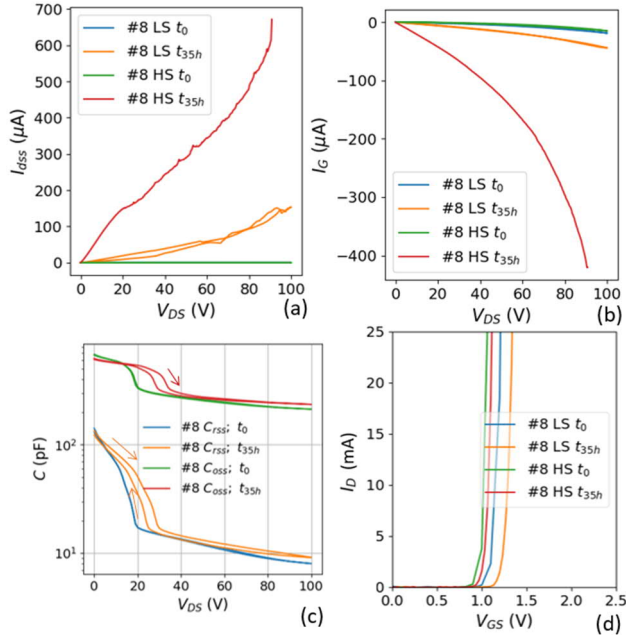


Figure 7: Characterization of the stress board #8 before ( $t_0$ ) and after 35hours of supposedly no stress ( $t_{35h}$ ) under 67V without cross-conduction ( $T_d = 130ns$ ). (a) Drain leakage current  $I_{dss} = f(V_{DS})$ . (b) Gate current leakage during  $I_{dss}$  measurement of (a) showing the gate drain leakage (c)  $C_{rss}$  and  $C_{oss}$ . (d) Preconditioned measurement of  $V_{th}$  (for obtaining a stable value independent from the history of the device), a shift up to 25% can be observed.

Most of the transistors were degraded after 35 hours (leakage current above the ratings) yet all devices are still

working post-stress. Despite being physically degraded after  $t_{35h}$ , the transistors are still functional, they still switch and no visible change ( $dv/dt$ ,  $\delta V_{GS}$ , oscillations...) has been observed, even for the degraded ones. The less degraded transistors have leakage levels within the ratings given in the datasheet despite being physically and electrically “changed”. With the hard switching stress or high  $V_{DS}$  voltage stress, 100% of the devices tested drifted or were degraded. Unexpectedly, for the “non-stressed” transistors ( $V_{DS}$  67V, long deadtime conditions) that were not supposed to drift as well as for the transistors that were under DC voltage at off-state for the same duration, around 30% of these devices were physically degraded (for example board #8 as it can be seen in Fig. 7).

Num.	Stress	Drift observed			
		$I_{gss}$	$I_{dss}$	$C_{rss}$	$V_{th}$
#1	120V, 30ns	LS $D_{pin}$ ; HS $\approx D_{pin}$	short GD	$C_{rss}$ const. at $V_{DS} > 70V$	no
#2	120V, 30ns	LS $\searrow$ ; HS $\searrow$	$\nearrow$ at $V_{DS} > 80V$	$C_{rss}$ const. at $V_{DS} > 70V$	$\searrow$
#3	120V, 30ns	LS $\nearrow$ ; HS $\nearrow$	$\nearrow$ at $V_{DS} > 80V$	$C_{rss}$ const. at $V_{DS} > 70V$	$\searrow$
#4	120V, 120ns	LS $\nearrow$ ; HS $\searrow$	$\nearrow$ at $V_{DS} > 80V$	$C_{rss} \approx$ const. at $V_{DS} > 70V$	$\approx \searrow$
#5	120V, 120ns	LS $\searrow$ ; HS $\nearrow$	$\approx$ at $V_{DS} > 80V$	$C_{rss} \approx$ const. at $V_{DS} > 70V$	no
#9	67V, 20ns	LS $\nearrow$ ; HS $D_{pin}$	HS: $\approx$ short GD	$C_{rss}$ shift	no
#10	67V, 20ns	LS $\times D_{pin}$ ; HS $\nearrow$	short GD	$C_{rss}$ shift	no
#8	67V, 120ns	LS $\nearrow$ ; HS $\nearrow$	short GD	$C_{rss}$ shift	$\nearrow$
#11	67V, 120ns	LS $\nearrow$ ; HS $\nearrow$	short GD	$C_{rss}$ shift	no

Table 2: Summary of the most significant drifts of intrinsic parameters observed on the stressed devices. The arrows stand for increase or decrease, the symbol  $\approx$  stands for “less significant” for the devices that exhibit the same drift but to a lesser degree, “ $\times D_{pin}$ ” means that the  $D_{pin}$  effect is not present anymore due to the degradation.

Table 2 summarizes the most important degradations observed during the stresses. The high voltage stress (120V) seems to change the drain leakage current at high  $V_{DS}$ . The transistors stressed at low voltage shows a gate-drain leakage current and a  $C_{rss}$ -knee shift. The cross-conduction increases the level of leakage and degradation in both cases (Fig. 3 vs Fig. 4). The high voltage stress with cross-conduction can combines the two changes (see Fig.6), a high drain leakage current appears as well as a GD leakage and capacitance knee shift. A physical interpretation of these results is given in the next part.

### 3.2. Hypothesis on degradation

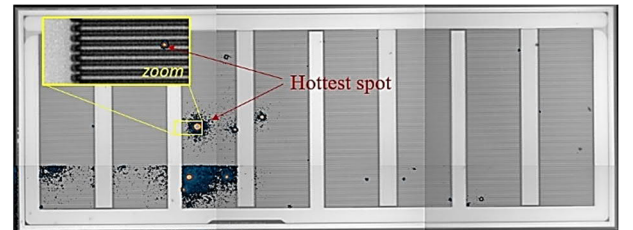


Figure 8: Infrared light LIT of transistor #2 LS (stitching of several images) with a 5x magnification under an electric polarization between 75V and 95V (lock-in frequency 25Hz), applied with probes landed on the electrical vias. The acquisition time is 3 to 5s. The LS transistor of board 2 was cut-off from the

board, all the board layers (PCB and copper layers), leadframe and transistor package were mechanically removed by parallel lapping. The silicon substrate was thinned to a thickness of  $100\mu\text{m}$ . The view of the chip on Fig.8 is an upside-down view of the chip's GaN layers through the silicon substrate. Around 20 hot spots appear on the chip with one hotter than the others (10x magnification zoom in small window).

A localization of physical degradation has been conducted with infrared Lock-In Thermography (LIT) (Fig.8) indicating the location of possible physical degradations in the transistor. Many hotspots were revealed on the whole active surface of the device. As shown in Fig. 9, that uses another type of localization of defect method called Photon Emission Microscopy (PEM), the emission spots (defects zones) are on two different locations on the metal pattern of the transistor represented on Fig.9c. One of them is near the gate, between the gate and the field plate (FP) (Fig.9a) while the other is closer to the drain contact, between the field plate and the drain metal (Fig.9b). The most stressed devices (#1,#2,#3: High voltage and cross-conduction), have numerous spots in both LIT and PEM (more than 20) and are on the two locations that have been described before, but mainly near the drain edge. In general, it has been observed that spots are near the drain for devices that have been stressed at  $V_{\text{DS}}=120\text{V}$  and near the gate for 67V stress. A non-stressed device was also tested and presented no such hot spots.

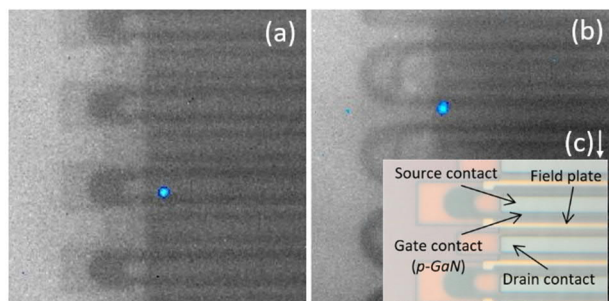


Figure 9: InGaAs camera PEM image of the emission spots. (a) Defect near the gate that might be a GD leakage current through the AlGaN barrier (b) defect near the drain metal that is expected to be a DS leakage current through the GaN layer. (c) optical zoom of the metal structure seen from the backside. The blur in these pictures cannot be avoided as it depends on the camera resolution and the remaining GaN thickness of  $10\mu\text{m}$  we look through with the IR camera.

### Degradation near the gate metal (Low voltage/cross-conduction)

The spots located between gate and field plate could be related to the gate-drain leakage current observed on transistors of boards #1,#8,#9 (HS only), #10 and #11. It could be the failure of the  $D_{\text{pin}}$  diode in the gate stack see Fig.10a or may correspond to a leakage path on the sidewall of the p-GaN layer as illustrated in blue in Fig. 11. This zone is a weak spot in terms of insulation, the

form of the gate metal makes a spike and a cavity below, reducing the insulation distance. During the FIB Slice&View it has been observed that this distance could be much smaller than the one represented in Fig.11. Electrically, it shorts the equivalent  $D_{\text{pin}}$  diode between the p-GaN/AlGaN and AlGaN/GaN interfaces. This leakage current is correlated with the  $C_{\text{rss}}$ -knee shift to higher  $V_{\text{DS}}$  (Fig.7c). The preconditioned threshold voltage (see the full protocol in [6]) is also affected with an increase up to 30% as shown in figure 7. The  $C_{\text{GD}}$ -knee shift to higher  $V_{\text{DS}}$  is an indicator of degradation in the field plate (FP) area.

This degradation is ascribed to charge trapping in defects caused by hot electrons generation. These traps could be located in the oxide layer (injected via tunneling over the AlGaN barrier, the same traps can also be in the GaN layer) and change the polarization around the 2DEG. The new polarization shifts the  $C_{\text{rss}}$  knee to a higher voltage (shift up to 20V) which means it affects the depletion behavior of the 2DEG under  $V_{\text{DS}}$  at off-state as explained in [6]. The 2DEG under the FP is still activated at a higher  $V_{\text{DS}}$  than at  $t_0$ . The presence of the 2DEG in this range of  $V_{\text{DS}}$  voltage acts against the field plate effect. Indeed, the FP purpose is to protect the gate stack from the electric field by moving away the main peak to the edge of the FP with the depletion of the 2DEG. Then during the electrical stress  $V_{\text{DS}}$  generates a high electric field which eventually leads to a local gate-drain breakdown. In another study the negative breakdown voltage (BV) value of the gate was measured around -38V which meets the voltage value of the shifted  $C_{\text{rss}}$ -knee after stress. It indicates that this voltage may have been applied on the gate during the stress. Note that the "drain" in this leakage path is actually the 2DEG connected to the drain metal.

The nature of defect for the accumulated degradation might either be cracks formation through thermomechanical stress, generated by hot electrons scattering the lattice [5] or the hypothesis stated in [7]. The report of [7] explained it might be hot electrons that generate electron-hole pairs with impact ionization, injecting holes in the oxide layer, locally increasing the electric field too and leading to dielectric failure. A metal filament can be formed from the metal gate for instance leading to the GD leakage. A Transmission Electronic Microscope lamella would be necessary to verify the hypothesis made in this paper.

For the transistors that were less stressed (67V, 120 ns and DC stress: #6,7,8,11,12,13) the higher electric field on the gate stack due to the  $C_{\text{rss}}$ -knee shift due to trapping reducing the FP effect is also the cause of failure. However, in these cases the trapping phenomenon is far less significant and might not be related to hot electrons and degradation of layers but is only due to the electric field of  $V_{\text{DS}}$  [8]. The traps accumulated with time increased the shift and the electric field near the gate stack leading, for some of the devices, to failure. The samples lot used in



this work might present a technology that may not have a sufficient quality regarding of the high hysteresis encountered, the low duration before degradations and the significant instability of  $V_{th}$  in [6].

### Degradation near the drain metal (High voltage)

The second spot location is a defect near the drain edge (or field plate drain side edge but less likely). This defect localization is correlated with a change of  $I_{dss}$  and  $C_{GD}$  at high voltage (above  $V_{DS} = 80V$ ). The capacitance after the knee is reduced and for the strongest stresses (#2, #3 for instance) it even becomes constant at a given  $V_{DS}$  value. The depletion of the 2DEG is faster after the field plate ( $V_{ds} > 20V$ ) for a degraded device and the surface of the 2DEG does not even vary (after 65V on Fig.4b for instance) for the devices that show a constant capacitance from a given  $V_{DS}$  value at  $t_{35h}$ . It means that the 2DEG is fully depleted or that the leakage current is entirely vertical through the defect. Indeed, the drain-source leakage current has no influence on the gate current during the  $I_{dss}$  measurement as seen on the characterization results (see Fig 4c and 4d).

This leakage path is expected to be at the edge of the drain metal and to be vertical across the GaN layer as illustrated on Fig. 10(b) and Fig. 11 in yellow. The leakage current then reaches the conductive epitaxial layers (AlGaIn or GaN, the epitaxy is a stack of AlGaIn and GaN layers) below the GaN buffer and connected to the source electrode. This leakage is not across the whole silicon substrate as the thinning of the silicon substrate (10  $\mu m$  to 2 $\mu m$ ) and backside package removal did not make the spot disappear.

A drain-source leakage current between the field plate and the 2DEG across the AlGaIn and oxide layer under the field plate hypothesis can be ruled out thanks to another study we made on this part-number device (study of static  $V_{DS}$  breakdown voltage). This defect location leads to the melting of the FP and to a filament path (around 150V) see Fig 11, the current leakage path is a direct short and not an abnormal current leakage appearing only above 80V like in this case. A Focused Ion Beam (FIB) Slice and View verified this failure mechanism (Fig. 11 in red).

The current and high electric field distribution might alter the GaN layer quality through the emission of hot electrons that transfer energy to the lattice and change its quality as the stress is an aggravated semi-ON/Hard switching stress [2]. The high  $V_{DS}$  chosen in the stress of boards #1-5 eases this location degradation compared to 67V stress. With a same drain bias of 120V, cross-conduction accelerates this alteration as it increases the number of electrons and energy. The layer is then sufficiently degraded to completely deplete the 2DEG from  $V_{DS} = 60V$  during the off-state as shown in Fig.4(b). The completely depleted 2DEG during the stress increases the electric field peak amplitude at the edge of the drain

metal edge. The peak location will locally accentuate the degradation caused by hot electrons. As in the 67V stress scenario the physical defect is suspected to be a crack or a cavity due to thermomechanical energy generated by hot electrons.

This defect is located in a thick layer and does not entirely break the electrical isolation as the leakage appears only at high  $V_{DS}$  (a leakage threshold voltage value). The defect reduced the thickness of insulation, as  $V_{DS}$  increases the electric field peak amplitude also increases especially under the drain edge metal. At a given value (around  $V_{DS} = 90V$ ) the electric field amplitude is sufficient to reach the threshold leakage value and the leakage current  $I_{dss}$  can follow the new vertical leakage path across the GaN layer. This mechanism might be similar to Stress Induced Leakage Current (SILC).

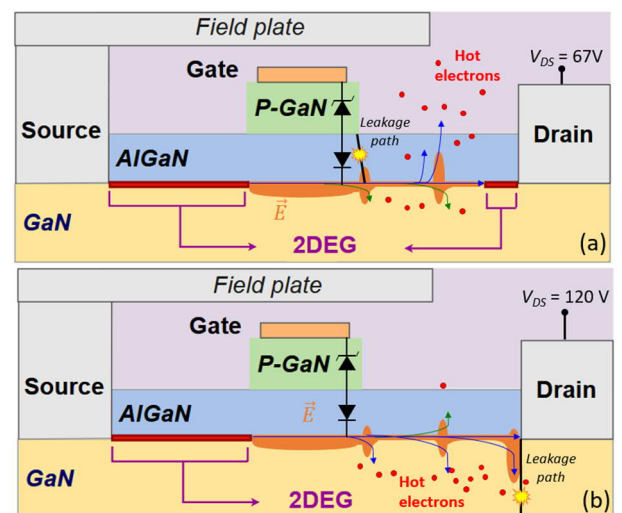


Figure 10: (a) Formation of the gate leakage path through degradation caused by the emission of hot electrons at (a)  $V_{DS} = 67V$  and (b)  $V_{DS} = 120V$ . The yellow “explosions” symbols illustrate the defect heating/light emission captured with LIT and PEM on Fig. 9 through the GaN layer.

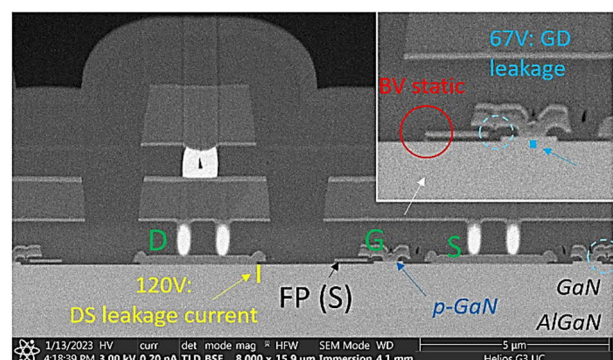


Figure 11: FIB cross-section of the active area showing the location where the defects are expected to be according to our hypothesis. In yellow the drain-source leakage which corresponds to Fig. 4c electrical signature. In blue the gate-drain leakage (Fig. 7ab) which is the failure of  $D_{pin}$  diode shown in Fig.10. Also, the form of the metal contact is not perfect due to fabrication maybe thermal relaxation. It makes a small spike and



a small cavity which reduces the dielectric insulation above (blue circles). This particular zone seems to be a weakness of this structure, in other pictures of the FIB Slice&View, it has been observed that the spike and the cavity could be bigger. In red the leakage path formed between drain and source in the previous study about static breakdown voltage. The AlGaN barrier is not visible in this picture due to its small thickness.

#### 4. Conclusion

This original no-load Half-Bridge test is particularly stressful and degrades the transistor very rapidly compared to its expected lifespan. A high drain leakage current occurs through physical defects that may originate from hot electrons's damages. The degraded areas are around the gate or in the GaN buffer, depending on the electric field distribution, which depends on the 2DEG depletion and thus on the bus voltage. The cross-conduction stress seems to accelerate and amplify the degradations as it increases the quantity of electrons. It has been observed that high voltage stress generates a high drain-source leakage current at high  $V_{DS}$ . This leakage current might come from a degradation in the GaN buffer near the drain metal. A stress at low voltage or a cross-conduction stress creates a  $C_{RSS}$  knee shift and a high gate drain current leakage. This electrical change is supposed to result from a physical degradation near or the gate stack. Further failure analysis will be conducted to verify the degradation mechanisms.

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#### References

- [1] Andrea Minetto, Nicola Modolo, Matteo Meneghini, Enrico Zaroni, Luca Sayadi, Sébastien Sicre, Bernd Deutschmann, Oliver Häberlen, "Hot electron effects in AlGaN/GaN HEMTs during hard-switching events, *Microelectronics Reliability*", Volume 126, 2021, 114208, ISSN 00262714, doi:10.1016/j.microrel.2021.114208.
- [2] I. Rossetto *et al.*, "Evidence of Hot-Electron Effects During Hard Switching of AlGaN/GaN HEMTs," in *IEEE Transactions on Electron Devices*, vol. 64, no. 9, pp. 3734-3739, Sept. 2017, doi:10.1109/TED.2017.2728785.
- [3] N. Perera, A. Jafari, R. Soleimanzadeh, N. Bollier, S. G. Abeyratne and E. Matioli, "Hard-Switching Losses in Power FETs: The Role of Output Capacitance," in *IEEE Transactions on Power Electronics*, vol. 37, no. 7, pp. 7604-7616, July 2022, doi:10.1109/TPEL.2021.3130831.

- [4] U. Jadli, F. Mohd-Yasin, H. A. Moghadam, J. R. Nicholls, P. Pande and S. Dimitrijević, "A Simple Equation for the Energy Stored by Voltage-Dependent Capacitances," in *IEEE Transactions on Power Electronics*, vol. 35, no. 12, pp. 12629-12632, Dec 2020, doi: 10.1109/TPEL.2020.2993639.
- [5] R. R. Chaudhuri, V. Joshi, S. D. Gupta and M. Shrivastava, "On the Channel Hot-Electron's Interaction With C-Doped GaN Buffer and Resultant Gate Degradation in AlGaN/GaN HEMTs," in *IEEE Transactions on Electron Devices*, vol. 68, no. 10, pp. 4869-4876, Oct. 2021, doi: 10.1109/TED.2021.3102469.
- [6] L. Ghizzo, D. Trémouilles, F. Richardeau, S. Vinnac, L. Moreau, N. Mauran, "Preconditioning of p-GaN power HEMT for reproducible  $V_{th}$  measurements", *Microelectronics Reliability*, Volume 144, 2023, 114955, doi:10.1016/j.microrel.2023.114955.
- [7] Alejandro Pozo, Shengke Zhang, Gordon Stecklein, Ricardo Garcia, John Glaser, Zhikai Tang, and Robert Strittmatter, *GaN Reliability and Lifetime Projections Phase 14, Efficient Power Conversion (EPC)*, 2022.
- [8] J. Chen *et al.*, "OFF-State Drain-Voltage-Stress-Induced VTH Instability in Schottky-Type p-GaN Gate HEMTs," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 9, no. 3, pp. 3686-3694, June 2021, doi: 10.1109/JESTPE.2020.3010408.