



HAL
open science

A wideband sub-6GHz continuously tunable gm-boosted CG Low Noise Amplifier in 28 nm FD-SOI CMOS technology

Mohamed Khalil Bouchoucha, Manuel Barragan, Andreia Cathelin, Sylvain Bourdel

► To cite this version:

Mohamed Khalil Bouchoucha, Manuel Barragan, Andreia Cathelin, Sylvain Bourdel. A wideband sub-6GHz continuously tunable gm-boosted CG Low Noise Amplifier in 28 nm FD-SOI CMOS technology. IEEE 49th European Solid State Circuits Conference (ESSCIRC 2023), Sep 2023, Lisbon, Portugal. 10.1109/ESSCIRC59616.2023.10268734 . hal-04241250

HAL Id: hal-04241250

<https://hal.science/hal-04241250v1>

Submitted on 22 Oct 2023

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.



Distributed under a Creative Commons Attribution - NonCommercial 4.0 International License

A wideband sub-6GHz continuously tunable g_m -boosted CG Low Noise Amplifier in 28 nm FD-SOI CMOS technology

M. Khalil Bouchoucha^{1,2}, Manuel J. Barragan², Andreia Cathelin¹, Sylvain Bourdel².

¹STMicroelectronics, 38920 Crolles, France

²Univ. Grenoble Alpes, Grenoble INP, CNRS, TIMA, 38000 Grenoble, France

Abstract— This paper presents the design of a tunable multi-mode inductorless Low Noise Amplifier (LNA) based on an active g_m -boosting Common Gate (CG) architecture. The tunability is achieved through a discrete coarse mode selection followed by a continuous fine-tuning thanks to the back gate of the Fully-Depleted Silicon-On-Insulator (FD-SOI) technology. It demonstrates the capability offered by the body bias to implement finely tunable architectures. The proposed LNA targets the Long-Term Evolution for machines (LTE-M) and Narrowband IoT (NB-IoT) cellular standards. It has been implemented in STMicroelectronics 28 nm FD-SOI Technology with an active area of 0.0059 mm². The measured performance exhibits more than 30 dB voltage Gain with 20 dB of dynamic over the implemented modes. The noise figure (NF) ranges from 1.8 dB to 7 dB while the Input referred third-order Intercept Point (IIP_3) ranges from -24.5 dBm to -6.5 dBm depending on the selected mode. The maximal power consumption is 1.86 mW from a 0.9 V supply. The LNA performances are fine-tuned across the modes achieving a large coverage of the design space.

Keywords—IoT, LTE-M, NB-IoT, LNA, Low power, FD-SOI, multimode, adaptive, body-bias control.

I. INTRODUCTION

The new generation of Internet-of-Things (IoT) devices including smart cities, connected greenhouses and medical assistance, brings in new challenges on classical technologies related to coverage in inaccessible areas, battery lifetime and cost. In this context, two cellular technologies have been introduced with the 3GPP releases 13 to 16, the LTE-M and the NB-IoT [1]. These applications impose strict challenges on RF transceivers to target good performances at a reduced power budget. From the receiver (RX) point of view, it should operate in a wideband frequency range from 460 MHz up to 2.2 GHz. To satisfy the high coverage and penetration requirements from both standards with best-in-class performance, a challenging sensitivity of -116 dBm is needed which implies a very low noise figure (NF). Since the Low Noise Amplifier (LNA) is the main noise contributor as the first block in the RX chain, across the power input range it must comply with a minimal NF of 2 dB at the maximum gain while 10 dB is sufficient at the maximal input level ($P_{in} = -25$ dBm). Besides, due to the large input power dynamic range (from -116 dBm for the NB-IoT and -110 dBm for the LTE-M cases to -25 dBm) a multi-mode solution is required.

Moreover, the selectivity and resilience towards RX blockers translates into requirements on the LNA linearity performance. This concerns mainly the low-sensitivity mode since it targets higher input signals. Thus, due to high blocker levels, a compression point of -15 dBm and an IIP_3 of -10 dBm are required.

In addition to these requirements, an aggressive power consumption below 2 mW is targeted and a compact inductorless single-ended solution is preferable for IoT SoC integration.

In this paper we propose a multimode LNA that addresses the described design challenges. The proposed solution makes use of the high intrinsic performance of the FD-SOI technology, together with its tunability capabilities thanks to the body-bias control. This allows an additional tuning knob to adjust the transistor main metrics and reduce power consumption for the target performance.

The rest of the paper is organized as follows. In Section II, the architecture selection with respect to the state-of-the-art is detailed. Section III describes the proposed LNA circuit and derives analytical expressions for its main performances. Then, section IV details the implementation in a 28 nm FD-SOI technology and presents measurement results. Finally, section V summarizes our main contributions.

II. ARCHITECTURE SELECTION AND STATE-OF-THE-ART ANALYSIS

The circuit's topology is selected based on a theoretical analysis and the wideband LNA state-of-the-art review [2] to target the specifications. A high value and flat gain, low noise figure and good impedance matching are needed across a wide RF frequency band. Besides, reduced area and low power consumption are key characteristics of the target design. Inductive degenerated circuits have good noise and power consumption performances [3]. However, they do not comply with low-cost compact radios for IoT applications due to the area overhead of the on-chip inductors.

The common gate (CG)-based topologies are wideband and show attractive power efficiency numbers. Although the design methodology for matching and gain settings is simple, the CG suffers inherently from a NF higher than 2-3 dB [4] which does not meet our specifications. Nevertheless, the main advantage of this topology over the CS-based ones, is the availability of the gate terminal to feed an extra RF signal. In fact, with appropriate DC biasing and filtering, an RF signal applied to the gate of a CG topology could be an opportunity to improve its performance without affecting the amplifier behavior. For instance, unbalanced signals applied to both source and gate terminals will improve the gate-to-source voltage swing, V_{GS} , and then improve the effective transconductance of the device. Thus, the g_m -boost CG topologies have a great potential to reduce the CG noise at low power. The generic configuration of this topology is shown in Fig.1. The principle is based on introducing an auxiliary amplifier with a gain of $(-A)$ between the source and the gate terminals. Hence, the transconductance of the classic CG is increased by $-(A+1)$ factor. Passive implementations rely mainly on the cross-coupled capacitor (CCC) pair technique [5] to set $A = 2$. Introducing multiple gain loops allows to increase A . However, some of these solutions need external transformers or inductors [4], [6]. Although inductorless solutions based on several feedback

loops [7] achieve better NF , gain and power consumption trade-offs, they are restricted to fully differential topologies. An auxiliary CS amplifier can serve as active g_m -boosting for single ended architectures. Besides, the noise canceling (NC) architecture reduces further the CG noise [8]. The LNA in [9] features these techniques to achieve a NF of 2.1 dB for 4.5 mW power consumption. However, an external inductor is needed for biasing. The complementary current reuse CS stage with NC in [10] suppresses the inductor and reduces the power to 3.4 mW for higher NF . Nevertheless, these single-gain-mode solutions are not suitable for our LNA requirements. A multi-mode active g_m -boost CG in [11] features 3 discrete gain steps through a transistor switching technique. Despite a power budget limited to 2 mW, the minimum NF is higher than 3 dB and multiple control signals are needed for mode switching.

In this paper, we propose a compact wideband single-ended LNA based on continuously tunable multimode g_m -boost CG architecture. It has a significantly reduced NF in the high-sensitivity mode (sub-2dB) for a power consumption below 2 mW while satisfying the linearity requirements for the low-sensitivity mode.

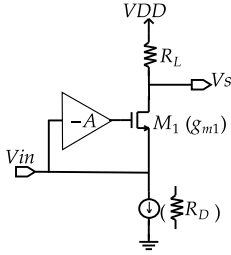


Fig. 1. Generic circuit of the g_m -boost CG LNA

III. PROPOSED ACTIVE GM-BOOST LNA

A. Circuit Description

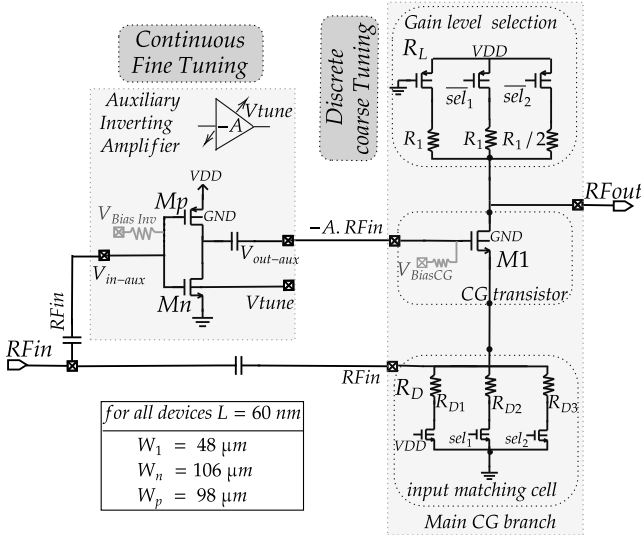


Fig. 2. Simplified schematic of the proposed multi-mode LNA.

The schematic of the proposed LNA is shown in Fig. 2. It is based on the active g_m -boost CG architecture. The CG branch comprises also a switched load resistor R_L and a switched degeneration resistor R_D at the source of the CG transistor M_1 imposing the input matching. The active boosting is implemented with an auxiliary inverting amplifier composed of the NMOS M_n and PMOS M_p transistors to feed the amplified input signal to the gate of M_1 .

The LNA main performance equations are derived from the small signal equivalent circuit depicted in Fig.3. For the inverting amplifier, the equivalent components are expressed through the NMOS and PMOS relative characteristics in parallel expressed as $G_M = g_{mn} + g_{mp}$, $R_{DS} = \frac{1}{g_{dsn} + g_{dsp}}$, $C_{GS(D)} = C_{gs(d)n} + C_{gs(d)p}$ and $C_{DS} = C_{dsn} + C_{dsp}$. C_{L1} is the equivalent load capacitor at the output V_{out_aux} and C_L is the load capacitor of the LNA. The transfer function of the inverting amplifier is expressed as,

$$A(j\omega) = \frac{V_{out_aux}(j\omega)}{V_{in_aux}(j\omega)} = -G_M R_{DS} \frac{1 - j\omega \frac{C_{GD}}{G_M}}{1 + j\omega (C_{GD} + C_{DS} + C_{L1}) R_{DS}} \quad (1)$$

The LNA input resistance can be expressed as,

$$R_{in}(j\omega) = \frac{1}{g_{m1}(1 + A(j\omega)) \left(1 - \frac{1}{g_{m1} R_D}\right)} \quad (2)$$

where g_{m1} is the M_1 transistor transconductance.

The static voltage gain expression can be simplified as,

$$G_o = \frac{V_{out}}{V_{in}} = g_{m1} R_L (1 + A) \quad (3)$$

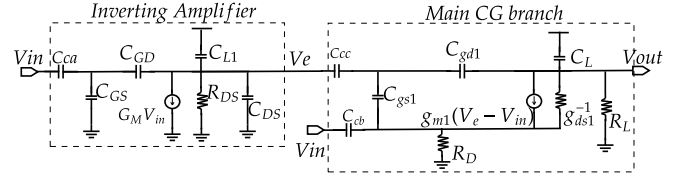


Fig. 3. Equivalent small-signal model of the proposed multi-mode LNA.

The noise factor of the LNA considering M_1, M_n, M_p, R_L, R_D and the source resistance $R_S = 50 \Omega$ is,

$$F = 1 + \frac{\gamma \left(\frac{A^2}{G_M} + \frac{1}{g_{m1}} \right)}{(1 + g_{m1}(1 + A)R')^2 (1 + A)^2 R_S} + \frac{\frac{R_S}{R_D}}{(1 + R_S(1 + A)g_{m1})^2} + \frac{1}{R_L R_S (g_{m1}(1 + A))^2} \quad (4)$$

with $R' = R_D // R_S$ and γ is the excess noise factor that we consider the same for the three transistors for simplification.

For a LNA, the IIP_3 is preferred to express the linearity performance. The equivalent V_{IIP_3} voltage can be derived as,

$$V_{IIP_3} = \sqrt{\frac{1}{\frac{(1 + A)^2}{IIP_{3cg}} + \frac{A}{(1 + A)IIP_{3aux}^2} + \frac{3}{2} \frac{A}{IIP_{2cg} IIP_{2aux}}}} \quad (5)$$

where, IIP_{2cg} and IIP_{3cg} are the input referred second and third intercept points of the CG branch and IIP_{2aux} and IIP_{3aux} are the second and third intercept point of the inverting amplifier.

B. Multimode Operation

The multimode operation of the proposed LNA combines coarse and fine tuning to allow a large coverage of the design space and the continuity of the performance variation along a large dynamic. Discrete gain steps of 6 dB are obtained by selecting different resistances forming R_L , through the switches commanded by the signals sel_1 and sel_2 . Since the voltage gain is proportional to R_L as indicated in (3),

controlling its value determines the operation mode as shown in Table I.

TABLE I. MODE DESCRIPTION FOR EACH CONFIGURATION

Mode	High sensit.	Medium sensit.	Low sensit.
P_{in} [dBm]	-116 to -60	-60 to -40	-40 to -25
R_L	R_1	$R_1/2$	$R_1/4$
sel_1	$sel_1 = sel_2$	$sel_1 = 0$	$sel_1 = sel_2 = 0$
sel_2	$= V_{DD}$	$sel_2 = V_{DD}$	
Voltage Gain	G_0	$G_0 - 6dB$	$G_0 - 12 dB$

Within each mode, the inverting amplifier boosting factor ($-A$) is finely tuned via a continuous control offered by the body-bias variation of M_n ensuring the continuity between adjacent modes. As shown in section III.A, the ($-A$) variation allows to sweep the LNA main performances. The body-bias voltage V_{tune} adds in variations of the inverting amplifier characteristics atop the coarse control setting. Besides, it allows to compensate corner variations. The input matching condition is maintained while varying ($-A$) by setting R_{in} within values that assure a return loss $S_{11} < -10$ dB. Hence, this condition is satisfied through the choice of g_{m1} and the degeneration resistance R_D for each mode.

IV. MEASUREMENT RESULTS

Fig. 4 presents the microphotograph of the fabricated chip in 28nm FD-SOI CMOS 8ML technology. The active area of the LNA is 0.0059 mm². The implemented circuit includes an output buffer based on a source follower for measurement purposes. The buffer contribution is de-embedded from the reported results using a stand-alone on-chip test path.

To demonstrate the feasibility and the performance of the proposed LNA, measurement results along with LNA post layout simulations (PLS) are presented for the 3 operation modes showing performances tunability within each mode.

Fig. 5 presents the small-signal measured performances of the three modes. Thanks to the CG branch, a 4 GHz wideband matching ($S_{11} < -10$ dB) is achieved over all the gain values. The high-sensitivity mode measured performances are shown in Fig. 5a. The LNA achieves a sub-2dB NF in line with the target specifications. Over the fine-tuning range, the minimum noise figure ranges from 3 dB to only 1.84 dB. The NF is then degraded at very low and higher frequencies because of the flicker noise and respectively the LNA bandwidth limitation. A 500 mV V_{tune} tuning range allows to get 7 dB of gain variation without impacting the 3-dB bandwidth that remains at 2.2 GHz as required. The LNA exhibits a maximum gain ranging from 23.5 dB up to 30.5 dB

with a power budget between 1 mW and 1.86 mW. Also, the S_{21} and NF shapes are similar for different V_{tune} values.

Fig. 5b shows the main results of the medium-sensitivity mode. The LNA achieves an S_{21} between 19 dB and 26 dB with a 3 dB bandwidth of 3.1 GHz. The measured NF is quite flat with the frequency, achieving a minimum from 2.5 dB to 4.3 dB as a function of V_{tune} .

The low-sensitivity mode allows to complete the 20 dB dynamic of gain tuning, with an S_{21} varying from 19 dB to 9.3 dB as depicted in Fig. 5c. For all V_{tune} values, it achieves the highest 3-dB bandwidth at 5 GHz. Furthermore, the NF can be tuned from 3 dB to 7 dB for a power consumption between 1.68 mW and 0.81 mW, respectively.

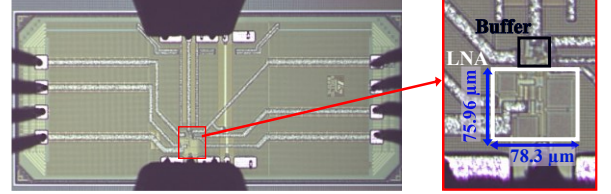


Fig. 4. Chip micrograph

Upon the 3 coarse operation modes, good agreement between PLS and measurements is observed. Also, the continuous tunability performance allows covering a large design space including corners variation which complies with the standard requirements.

To evaluate the linearity performance, the input compression point P_{1dB} at 1 GHz is measured for the three modes over 1 V tuning range of V_{tune} . The obtained results are presented in Fig. 6. Since the NF and gain requirements in the low-sensitivity mode are relaxed, it achieves the best performance in terms of linearity with a $P_{1dB} = -15$ dBm for the lowest gain in line with the specifications.

For the IIP_3 measurements, a two-tone test at frequencies from 0.5 GHz up to 6 GHz is applied at the LNA input for the three configurations. The IIP_3 variation with respect to the frequency and V_{tune} is shown in Fig. 6. The IIP_3 remains constant with respect to the input frequency in the 3 operation modes, verifying the wideband operation of the LNA. The IIP_3 decreases with V_{tune} (i.e., with gain) according to (5). For the low-sensitivity mode, the lowest gain exhibits an IIP_3 as high as -6.4 dBm which is in line with the selectivity requirements. The worst-case scenario corresponds to the highest gain point within the high-sensitivity mode. Fig. 7 illustrates the IIP_3 curves with the fundamental and third-

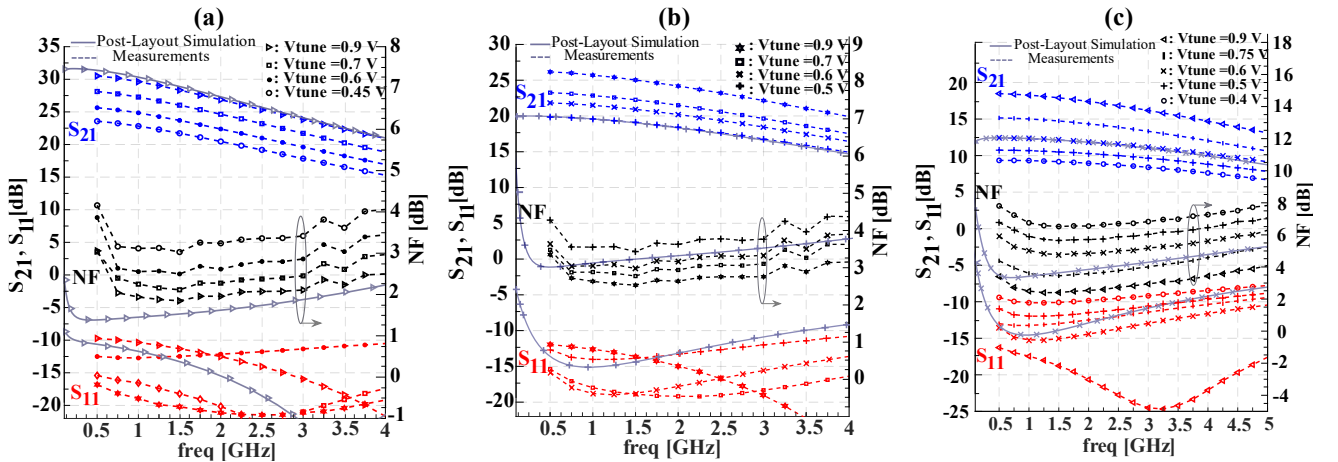


Fig. 5. LNA main performances: S_{21} , S_{11} and NF for (a). High-sensitivity mode, (b). Medium-sensitivity mode and (c). Low-sensitivity mode

order output powers. The obtained $IIP_3 = -25$ dBm is higher than the input power amplitudes for which this mode is active. Hence, the LNA respects the linearity requirements for all the modes.

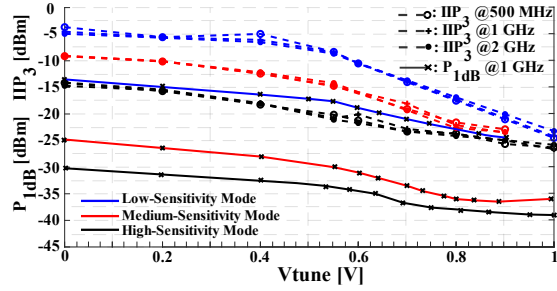


Fig. 6. IIP_3 and P_{1dB} variation with V_{tune} and tone-frequency across the modes

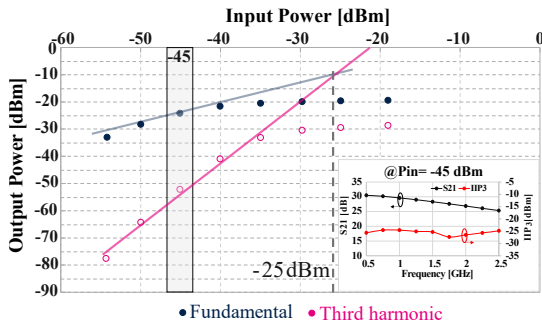


Fig. 7. IIP_3 @1 GHz for the highest gain point of the LNA

TABLE II. COMPARISON WITH STATE-OF-THE-ART WIDEBAND LNAs

Reference	This work			Access'21 [11]			ISSCC'22 [10]	JSSC'21 [9]	TMTT'11 [7]
	Model1	Mode2	Mode3	Mode1	Mode2	Mode3			
Architecture	Active gm - boost CG			Active gm - boost CG			Positive feedback CGCS with CM and active feedforward	CGCS with current reuse	CCC CG with multiple feedback
Multimode	Yes/Continuously tunable			Yes/Discrete Modes			No	No	No
Freq. Band [GHz]	0.5 ~ 2.2	0.5 ~ 3.1	0.5 ~ 5.2	0~4.5	0.5~3	0~4.5	0.2~3	0~4.5	0.1~1.7
S11 [dB]	<-10	<-10	<-10	<-7	<-7	<-7	<-12	<-10	<-10
Gain [dB]	23.5 ~ 30.5	19 ~ 26.1	9.3 ~ 19	22.9	19.4	16.8	18.6	15.2	23
NF [dB]	3 ~ 1.84	4.3 ~ 2.5	7 ~ 3	3.6	5.4	6.6	2.7	2.09	1.85
IIP_3 [dBm]	-16 ~ -24.5	-13.2 ~ -23.4	-6.5 ~ -20.5	-17.2	-16.8	-16.4	-8.5	-4.6	-2.85
Power [mW]	1 ~ 1.86	1 ~ 1.8	0.81 ~ 1.68	2	0.9	0.35	3.4	4.5	2.8
VDD [V]	0.9			1.2	0.9	0.6	1	1	2
Techno. [nm]	28 FD-SOI			28 FD-SOI			28 CMOS	28 CMOS	90 CMOS
Silicon Area [mm ²]	0.0059			0.0015			0.0078	0.03	0.03
Biasing condition	Current source and body bias			Current source and transistor switching			Current source	Offchip inductor	—
Type/Nb. Inductors	S-E/0			S-E/0			S-E/0	S-E/1	Diff/0
FoM1	37 ~ 29.5	33 ~ 24	29 ~ 12.3	27.7	26.8	28	18.2	19.4	23.6
FoM2	81.7 ~ 74	78 ~ 69	73 ~ 56.9	84.2	83.2	84.4	60.36	49.8	54

S-E: Single-ended topology, Diff: Differential topology

$$FoM1 = 20 \log_{10} \left(\frac{Gain[abs]BW [GHz]}{P_{DC}[mW](F_{min} - 1)} \right) \quad FoM2 = 20 \log_{10} \left(\frac{Gain[abs]BW [GHz]}{P_{DC}[mW](F_{min} - 1)A[mm^2]} \right)$$

To verify the stability of the fabricated LNA, Fig. 8 shows the K -factor (K_f) derived from the measured S-parameters (LNA plus buffer) for the highest gain. The circuit is unconditionally stable as $K_f > 1$.

The LNA performance is summarized and compared with relevant wideband LNAs state-of-the-art in Table II. This work copes at the same time with the NF and power

consumption constraints while ensuring the relevant linearity specifications. The presented LNA achieves the same NF of 1.84 dB as best-in-class work [7] while consuming 33% less power. The proposed inductorless solution is at par with the lowest area solution [11], while improving noise and power consumption features. The linearity performance is at par with the state-of-the-art especially in the low-sensitivity mode. The proposed active g_m -boost CG LNA reaches up to 30.5 dB of voltage gain with the already mentioned low power consumption. To the best of authors' knowledge, this is the first time a wideband sub-6 GHz *continuously tunable* LNA is presented with a gain dynamic range of 20 dB and sub-2dB NF .

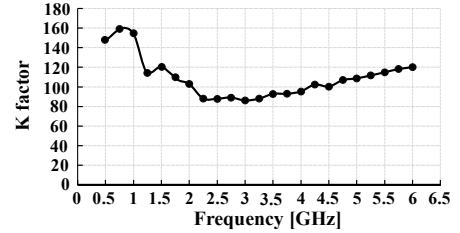


Fig. 8. Stability factor for the highest gain point of the LNA

V. CONCLUSION

The design and implementation of an inductorless wideband continuously tunable LNA is presented and measurements are positively compared with the state-of-the-art. This design takes advantage of the body bias terminal in the FD-SOI technology to fine-tune the LNA performance over a wide operation range. The proposed LNA is suited for the NB-IoT and LTE-M 5G cellular standards.

ACKNOWLEDGMENT

The authors would like to thank Mathieu COUSTANS and Frederic PAILLARDET from ST for fruitful design discussions as well as, Cybelle Goncalves from ST and Loic VINCENT from CIME Nanotech Grenoble for on-wafer measurements.

REFERENCES

- [1] <https://www.3gpp.org/specifications-technologies/releases/>
- [2] M. K. Bouchoucha *et al.*, "Performance benchmark of State-of-the-art Sub-6- GHz wideband LNAs Based on an Extensive Survey," Accepted for IEEE ISCAS May.2023
- [3] H. J. Lee *et al.*, "A 3 to 5 GHz CMOS UWB LNA with input matching using miller effect," IEEE JSSC Feb. 2006.
- [4] L. Zhang *et al.*, "A 3.2 mW 2.2-13.2 GHz CMOS Differential Common-Gate LNA for Ultra-Wideband Receivers," IEEE IMS, June 2022.
- [5] T. Cho *et al.*, "A Single-Chip CMOS Direct-Conversion Transceiver for 900MHz Spread-Spectrum Digital Cordless Phones", IEEE ISSCC, Feb. 1999
- [6] H. G. Han *et al.*, "A 2.88 mW +9.06 dBm IIP_3 Common-Gate LNA With Dual Cross-Coupled Capacitive Feedback," IEEE TMTT, March 2015.
- [7] E. A. Sobhy *et al.*, "A 2.8-mW Sub-2-dB Noise-Figure Inductorless Wideband CMOS LNA Employing Multiple Feedback," IEEE TMTT, Dec. 2011
- [8] S. C. Blaakmeer *et al.*, "Wideband Balun-LNA With Simultaneous Output Balancing, Noise-Canceling and Distortion-Canceling," IEEE JSSC, June, 2008
- [9] A. Bozorg *et al.*, "A 0.02–4.5-GHz LN(T)A in 28-nm CMOS for 5G Exploiting Noise Reduction and Current Reuse," IEEE JSSC, Feb 2021
- [10] Z. Liu *et al.*, "A 0.0078mm² 3.4mW Wideband Positive-Feedback-Based Noise-Cancelling LNA in 28nm CMOS Exploiting Gm Boosting", IEEE ISSCC 2022
- [11] T. Taris *et al.*, "Inductorless Multi-Mode RF-CMOS Low Noise Amplifier Dedicated to Ultra Low Power Applications," IEEE Access 2021.