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▶ To cite this version:

Hassan Hamad, Dominique Tournier, Jean-Michel Reynes, Olivier Perrotin, Régis Meuret, et al.. First Results on 1.2 kV SiC MOSFET Body Diode Robustness Tests. 34th European Symposium on Reliability of Electron Devices, Failure Physics and Analysis, Oct 2023, Toulouse, France. hal-04240602

HAL Id: hal-04240602 https://hal.science/hal-04240602

Submitted on 13 Oct 2023

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First Results on 1.2 kV SiC MOSFET Body Diode Robustness Tests

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Abstract

The paper propose a methodology study to analyze the body diode robustness of SiC MOSFETs. Different manufacturers, are used to validate the analysis. Two types of stresses have been applied: a continuous conduction test, (BDCT) or a pulsed conduction test, the classical half-sine surge current test applied to body diodes, BDSCT. BDCT applied current must be limited to avoid destruction related to the packaging but BDSCT enable to analyze both assembly degradation and bipolar degradation.

1. Context

SiC MOSFETs are widely used in new application design because of their strong loss reduction, as well as their capability of operating with high switching frequencies and high operating temperatures. Reliability issues related to the gate oxide are well addressed and numerous studies have been published on the topic of threshold voltage instabilities [1; 2]. It is also a classical way in power electronics to use the body diode to avoid an external Schottky diode [3; 4]. In the present study, 1.2 kV SiC MOSFET body diodes were stressed and studied to identify any aging or degradation issues in case of use.

Observing the diode conduction is not a standard test and little described in the associated datasheet. In this study the Body Diode Conduction Test, BDCT, [5] described in Fig. 1 enables to stress several body diodes during a long time, by applying a common and constant series current. Another classical stress is the surge current stress for diodes [6] that could be named Body Diode Surge Current Test, BDSCT for body diodes [7]. The circuit is described in Fig. 1.

The expected degradation phenomena are: the metallization degradation and associated metal reconstruction [8] and the bipolar degradation [9].

1 BDCT

1.1 BDCT setup

Picture of the test bench is shown in Fig. 2,

devices are placed on a heat plate in order to make tests under high temperature and air cooling system is used to help thermal dissipation. The test was performed on similar devices with $V_{\rm BR}$ of 1200 V and $R_{\rm DS-ON}$ of 75 m Ω , produced by two different manufacturers.



Fig. 1: Schematic of the experimental setup showing 4 DUTs put on the heat plate, and the thermocouple fixed on the surface of DUT1.

For both manufacturers, devices have shown overheat when studying 4 devices in the same time; in fact, for a DC current of 18 A, the average power to dissipate was about 75 W per device. Devices from manufacturer A and B were then both tested for 1000 hours, the stress was stopped each 100 hours to perform static characterization for the DUTs.

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Fig. 2: Experimental test bench of the BDCT setup.

1.2 BDCT results

In a first run, DUTs have been stressed at high current, near the nominal current specified in the



Fig. 3: Evolution of VTH during the BDCT stress datasheet. However, in this first test, all the DUTs were quickly destroyed (\sim 20 h), probably because of



Fig. 4: Evolution of the on-resistance measured at 20 A, during the BDCT stress

a temperature inhomogeneity and an overheating. So in a second step, devices for both manufacturers

were tested at a current of 18 A (which is approximately 0.5 $I_{\rm n}$) and for a negative $V_{\rm GS}$ equal to the recommended value given by the datasheet of each device.

For both manufacturers, no significant degradation has been seen along the stress. Fig. 3-5 show the stress results for both manufacturer devices. V_{TH} measurements were based on a bipolar preconditioning protocol (JEP184).



Fig. 5: Evolution of the diode on-voltage drop during the BDCT stress

The first 20 stress hours show a slight drift of characteristics (threshold voltage V_{TH} and the resistance R_{DS-ON} increase by 1% for both manufacturers. DUT B shows slight drift on its transfer and body diode characteristics); then the devices for both manufacturers do not show any parameter change for higher stress time.

2 Surge Current Test (BDSCT)

2.1 BDSCT setup

BDSCT test is interesting to determine the power limits that the device is able to support, however it is not possible to use this test with higher current, so the solution is to apply current pulses.



Fig. 6: Schematic of the experimental setup of the BDSCT.

Fig. 6 and Fig. 7 show the surge current test setup. The DUT and the power MOSFETs are places on an aluminum plate to force the heat dissipation. 4

capacitors (100 mF each) are added in parallel with the voltage source to insure the current demand and to avoid reaching the compliance of the voltage source.



Fig. 7: Surge current test setup

The highlighted part shows the control circuit and drivers are placed inside the white box. Fig. 8 and Fig. 9 show the current, voltage and power pulse waveforms. To avoid the self-heating of the DUT, and to recharge properly the capacitors, pulses are repeated with a period of 4 s.

For a pulse duration of 10 ms, the DUT shows significative degradation for a surge current of 2 I_n (Fig. 10). R_{DS-ON} increases by 10% (Fig. 12).



Fig. 8: DUT voltage and current pulse shapes (If & Vf)

This parameter change is probably due to local overheating on the contact level leading to critical degradation of the DUT.



Fig. 9: Main switch voltage (V_{DS}) and the power across them during the surge pulse.

It was then decided to reduce the pulse duration to 2 ms: decreasing the pulse duration will lead to the decrease of energy per pulse so, surge current could reach higher values allowing to trigger another degradation mechanism.



Fig. 10: Evolution of R_{DS-ON} after BDSCT up to 2 In for long pulse duration (10 ms).

Fig. 11 shows that for pulse duration of 2 ms and a surge current up to 4 I_n , the DUT does not receive critical degradation. R_{DS-ON} , transfer and body diode characteristics do not drift significantly.



Fig. 11: Evolution of DUT parameters after BDSCT up to $4 I_n$ for short pulse duration (2 ms).

For higher surge current (at 4.5 and 5 I_n), degradation is seen on the device characteristics. At



Fig. 12: Evolution of DUT B2 (stressed at 4.5 In) and DUT B3 (stressed at 5 In) R_{DS-ON} after BDSCT, for short pulse duration (2 ms).

this stage, $R_{\rm DS-ON}$ increases systematically 3.1 $m\Omega/1000$ cycles (at 4.5 I_n) and 4.9 $m\Omega/1000$ cycles (at 5 I_n).



Fig. 13: Evolution of DUT B2 (stressed at 4.5 In) and DUT B3 (stressed at 5 In) V_F after BDSCT, for short pulse duration (2 ms).

Body diode and transfer characteristics drift significantly to the right. Results are in agreement with the ones obtained by Palanisamy [9], for high body diode current, stack defaults are triggered and could be seen at high current measurements. The BDSCT does not affect the threshold voltage of the body diode and leakage currents which stay constant along the stress.

3 Conclusion

BDCT has a limited current level because of a temperature inhomogeneity (our assumption) that could be observed on an inconsistent Von measurement, with respect to the calibration process. However, for a reduced current level (~ In/2) no clear degradation was observed.

One option is to apply a pulsed current stress instead of a continuous current stress, but it will be further difficult to implement, particularly for several components connected in series.

Surge current stresses or BDSCTs yield an easier way to stress the body diodes. For great time duration, i.e. 10 ms, a weak metallization degradation is observed at nominal current.

For shorted pulse duration, the bipolar degradation could be observed at a high current level, about five times the nominal current.

The final paper will include further results on both BDCT and BDSCT measures, and some details about the temperature inhomogeneity will be presented.

Acknowledgements

This work was carried out in the framework of the IRT Saint Exupery project SiCRET (SiC Reliability Evaluation for Transport). We acknowledge the financial support from the SICRET industrial, and academic members and the financial support from the French National Research Agency (ANR).

SiCRET Industrial members: Alstom, Alter Technology, Emotors, Liebherr, Nucletudes, Safran, SuperGrid Institute, Thales, Vitesco Technologies. SiCRET academic members: Ampère, LAAS, IES.

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