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An Advanced Integrated Cooling Solution for High Voltage and Power Density Modules

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Abstract—This study investigated the thermal performance of a packaging solution designed to manage the electrical isolation and cooling of high voltage (> 3300 V) SiC power semiconductor devices. The proposed packaging merges the ceramic substrate and the heat exchanger into a single component, streamlining the overall design. Specifically, a novel heat exchanger is developed for a multi-chip module (20 kV), utilizing a combination of jet impingement and channel-flow cooling techniques. Computational fluid dynamics (CFD) simulations and experimental validation are conducted on a multi-chip module to assess the thermal resistance of this new cooling solution. The results demonstrate a low thermal resistivity of $0.118 \text{ cm}^2\text{K/W}$, indicating the potential for improved cooling performance in high voltage and power density semiconductor applications.

Index Terms—High voltage, insulation, packaging, computational fluid dynamics (CFD), Cooling, power electronics, high power density

I. INTRODUCTION

Power electronics packaging and cooling are crucial for high voltage power electronics modules (> 20 kV), especially as the demand for high power and energy efficiency continues to rise. Effective packaging and cooling solutions are essential to ensure reliable and safe operation. The advent of silicon carbide (SiC) technology has enabled the development of higher voltage power devices, which might be used in applications such as renewable energy systems [1]. However, these devices generate a substantial amount of heat during operation, which can lead to performance degradation, component failure, and safety concerns if not properly managed. Consequently, it is vital to design and implement effective packaging and cooling solutions to ensure the longevity and optimal performance of high voltage power electronics systems.

While the majority of research studies focus on the high voltage semiconductor devices themselves, it is important to also address the challenges associated with their packaging, particularly in terms of electrical insulation and thermal management. In traditional high voltage packages, a thick

solid layer, typically made of aluminium oxid (Al_2O_3) or aluminium nitride (AlN) ceramic, is required for electrical insulation, which limits the cooling performance. Additionally, high voltage SiC devices demonstrate exceptional electrical performance but are highly sensitive to elevated temperature. For instance, SiC MOSFETs experience a significant increase in on-state resistance, ranging from two to three times, when their temperature rises from 25°C to 150°C [2]. Several studies have indicated that operating high voltage SiC devices below 100°C junction temperature is preferable in order to fully leverage their performance advantages [3], [4]. Therefore, the target junction temperature of the power semiconductors in this work is specified to be below 100°C .

The ultimate aim of this study is to design a module rated at 20 kV. This work builds on a novel packaging concept that was previously presented for single-chip modules [5]. The proposed structure integrates the liquid cold-plate directly in the ceramic layer. This results in a dramatic reduction in complexity of the thermal path, which leads to a better cooling performance. With the adoption of the novel package, the thermal resistance for a single-die cooler at a water flow rate of 3 L min^{-1} is significantly reduced from 0.32 K/W in the traditional packaging to 0.26 K/W ($0.21 \text{ cm}^2\text{K/W}$). The previous work [5] is extended here for a 20 kV module with six 3.3 kV SiC MOSFETs and their six associated snubbers, making the structure and the cooling system more complex, but also more representative of a real application. The electrical structure of the module is described by Vienne et al. [6]. To simplify the cooling system, the power module is designed with two identical sub-modules, each containing three dies and three RC snubber circuits.

II. INTEGRATED COOLING DESIGN

A sub-module consists of three SiC MOSFETs and three snubbers attached to an AlN cooler. The SiC dies are placed on the upper part of the copper sheets and the snubbers on

TABLE I: Thermal requirements

Die size [mm ²]	power density q_{loss} [W/cm ²]	th. resistance R_{th} [K/W]	th. resistivity r_{th} [cm ² K/W]	inlet T T_{in} [°C]
8.9 × 3.676	367	< 0.5	< 0.16	40

the lower part. The top view of the system with the design parameters is shown in Fig. 1.

Both MOSFET and snubber circuits generate heat in operation and require cooling. The SiC dies (G2R50MT33-CAL) have a size of 8.9 mm × 3.676 mm. Each SiC die dissipates 120 W in nominal conditions. This corresponds to 367 W/cm² heat density. The target specification for the thermal resistance is 0.5 K/W or 0.16 cm²K/W when fluid’s inlet temperature is considered to be 40 °C. Table I summarizes the thermal requirements of the module.

The RC snubber has four resistors for static balancing (3.2 mm × 2.5 mm and 1.5 MΩ each, in series), a capacitor (680 pF) and twenty four resistors for dynamic balancing (3.1 mm × 1.6 mm and 75 Ω each, with four groups of six resistors in parallel, the four groups being connected together in series). Each snubber generates a total heat of 54 W, which is distributed among the resistors. The 75 MΩ resistors dissipate 2.22 W (44.76 W/cm²) each, while the 1.5 MΩ resistors dissipate 0.17 W (2.13 W/cm²) each. The datasheet [7] specifies a maximum operating temperature of 155 °C for the snubber components. This means that compared to the SiC MOSFETs, the snubbers have relatively low heat dissipation and can operate at higher temperatures, so this study will primarily focus on the cooling of the SiC dies.

The AlN cooler has a size of 100 mm × 50 mm × 12.5 mm. A thickness of 3.3 mm top AlN is chosen for insulation purpose between the spreaders and the cooling fluid. Four copper sheets are brazed on the AlN cooler. The copper sheets have a constant width of 40 mm. The length of the first copper sheet is 32 mm. This copper plate is larger than other plates because that is where the DC+ connector is placed. The middle two copper sheets have a length of 22 mm. The width of the copper sheets is the same as the snubbers (22 mm × 25 mm) to keep the size of the cooler as small as possible. The fourth copper sheet is required for later placement of the DC- terminal. A separation distance of 2 mm is selected between the copper sheets to effectively insulate the 3.3 kV from each other.

A cross section showing the material layers of the cooler is shown in Fig. 2. The SiC dies are sintered on copper spreaders brazed directly on the AlN heat sink. The snubber circuits are placed on AlN DBC substrates. The ground potential of the module is placed directly on the bottom. A creepage distance of about 17.5 mm is required for the electrical insulation (> 20 kV) between the top and bottom side. This is a combination of the height of the AlN cooler (12.5 mm) and 5 mm distance between copper sheets and the AlN edges. The channel (pins) has a height of 6 mm. Conical pins are used due to their better cooling performance [5]. The pins under the SiC dies have a top diameter of 2.7 mm and a bottom diameter of 1.8 mm.

A. Cooler design

The cooling system has been optimized, taking into account the constraints and limitations of the manufacturing process. It incorporates both inline and staggered pin configurations, allowing for optimal heat dissipation. A preliminary CFD analysis (not presented here) shows that inline pins provide a better cooling performance for jet impingement cooling, while staggered pins provide better performance for channel-flow cooling. However, channel-flow cooling produces high pressure drop in the system and uneven thermal resistances for the dies. To solve this problem, the cooler combines jet-impingement and channel-flow. The distance between the axes of the pins is kept as small as possible, limited to 3 mm by the manufacturer for inline pins. Staggered pins allow for larger pin density while keeping the same minimum distance between pins as for inline pins.

In Fig. 3, a cross-section of the channel at its midpoint is depicted showing the distribution of the pins in the channel. To increase the fluid velocity within the channel, a central 2 mm wide and 75 mm long wall is implemented, effectively dividing the flow between the snubbers and MOSFETs. Unlike the SiC dies, the temperature requirements for the snubbers are not as critical, which is why larger pins are positioned beneath them for easier manufacturing. The middle die (D2) benefits from jet-impingement cooling, while the other two dies are cooled through channel-flow. The arrangement of pins ensures that the staggered pins, being denser than the inline pins, compensate for the lower flow rate experienced by the top (D1) and top (D3) chips, resulting in balanced cooling across all three dies. The liquid is directed towards the snubbers through openings located at the channel’s sides, specifically targeting the area where the snubbers are located. Consequently, the snubbers benefit from the cooling method of channel-flow with staggered pins. The outlet is situated at the midsection of the snubber channel.

III. CFD CALCULATIONS

Ansys CFD is used for the simulations presented here. For all simulations, the boundary conditions are set as follows: 120 W power dissipation for each SiC die; constant water volumetric flow (0.5 to 3 L min⁻¹) at the inlet at 40 °C; zero-pressure condition at the outlet; conservative flow condition for all interface regions; adiabatic condition for all the external walls. For the snubbers, there is a heat dissipation of 2.22 W for each small resistor and 0.167 W for each large resistor (corresponding to 54 W per snubber).

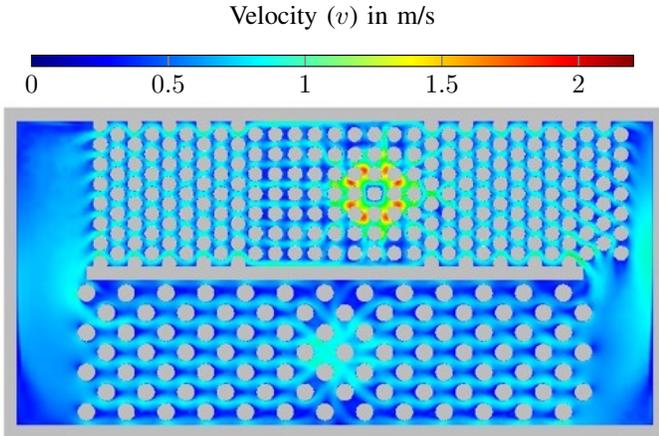
The properties (thermal conductivity and thickness) of the materials used for the simulations are presented in Tab. II. The layer names refers to Fig. 2

A. CFD results

The velocity distribution in the cooling channel is the key factor to achieve good cooling and similar temperatures of the three dies. The velocity distribution at the middle of the channel is shown in Fig. 4. Higher velocities are achieved under the middle die (D2) due to the jet impingement. Lower velocities

TABLE II: Materials properties

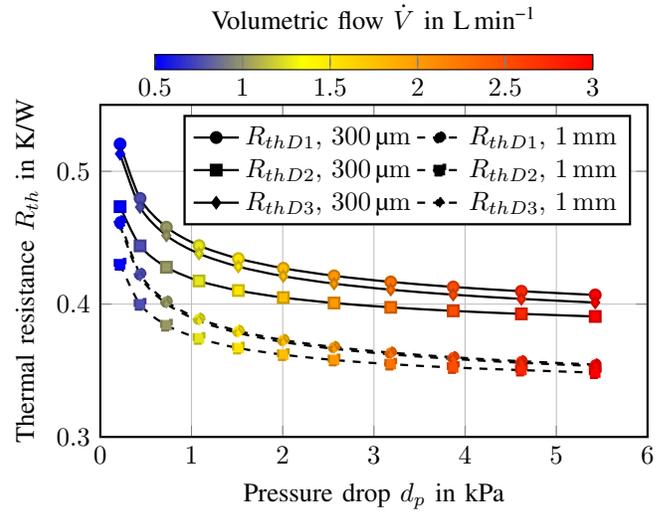
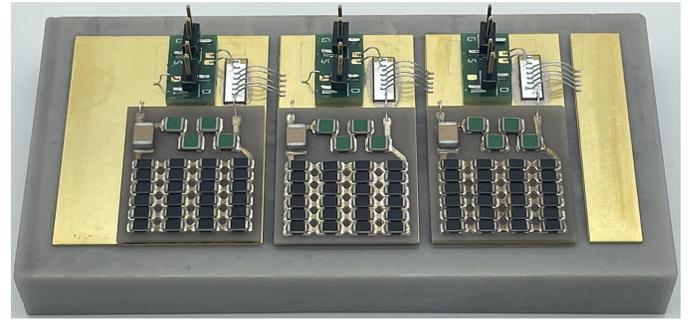
Material	Thermal conductivity λ [W/(mK)]	Thickness b [μm]
Chip (4H-SiC)	370	390
Die Attach (Ag)	100	50
spreader (Cu)	394	300 to 1000
Metal braze (AgCuTi10)	361	10
Resistors (Al_2O_3)	13	650
Cu1	394	300
AlN1	170	650
Cu2	394	150
Glue (epoxy adhesive)	11	50


 Fig. 4: Velocity distribution in the middle of the channel at 3 L min^{-1}

are observed under the two other MOSFETs. However, the staggered pins there produce more turbulences, enhancing the heat transfer process. The pins at wall (three-quarter pins) are important because they enhance the flow in the middle of the channel instead at the space between the wall and pins. Therewith, higher velocities are achieved in the channel under the dies leading to better cooling performance.

In Fig. 5, the computed thermal resistances of the three dies are depicted as a function of pressure drop for a cooler with copper spreader thicknesses of $300 \mu\text{m}$ or 1 mm . The colorbar at the top of the graph is scaled according to the flow rates, ranging from 0.5 L min^{-1} to 3 L min^{-1} . As the flow rates increase, the disparities in thermal resistances among the dies diminish. Particularly, a slight discrepancy in thermal resistances is noticeable with the $300 \mu\text{m}$ copper spreader, but this distinction is reduced at higher flow rates and with the adoption of thicker spreader (1 mm).

The use of thicker copper proves advantageous due to its improved heat spreading effects, resulting in better cooling performance under the same pressure drop conditions. At a flow rate of 3 L min^{-1} , a total pressure drop of approximately 5.5 kPa is calculated, corresponding to a total pumping power of about 0.27 W . The cooler with $300 \mu\text{m}$ copper achieves a maximum thermal resistance of about 0.41 K/W . This value is reduced to approximately 0.36 K/W with the 1 mm copper


 Fig. 5: Calculated thermal resistances of the three dies as a function of pressure drop; $300 \mu\text{m}$ and $300 \mu\text{m}$ refer to two thicknesses for the spreader layer; the location of the dies (D1, D2, D3) is shown in Fig.1

 Fig. 6: A prototype vehicle with 1 mm copper metallization

cooler. These findings highlight the significance of copper thickness in influencing the cooling performance of the system, and the impact of flow rates on the distribution of thermal resistance of the dies.

IV. EXPERIMENTAL STUDY

Three metallised ceramic (AlN) coolers are fabricated by CeramTec GmbH, Germany with identical internal layouts but with different copper spreader thicknesses ($300 \mu\text{m}$, $500 \mu\text{m}$, $1000 \mu\text{m}$). Three 3.3 kV SiC MOSFETs are sintered on the copper sheets. Three PCBs are placed beside the dies for the connection of the gate signal. The snubbers and PCBs are glued onto the metal pads. $300 \mu\text{m}$ aluminium wires are used for bonding the chips pads (gate, source and drain) to the PCBs. Two copper connectors are soldered onto the left and right copper sheets forming the the power terminals (DC- and DC+). Finally, two brass fittings (forming the inlet and outlet) are glued to the heatsinks. Fig. 6 shows the populated test vehicles. The test vehicles are connected to a test setup that consists of a fluid loop and a thermal analyzer (Phase 12B,

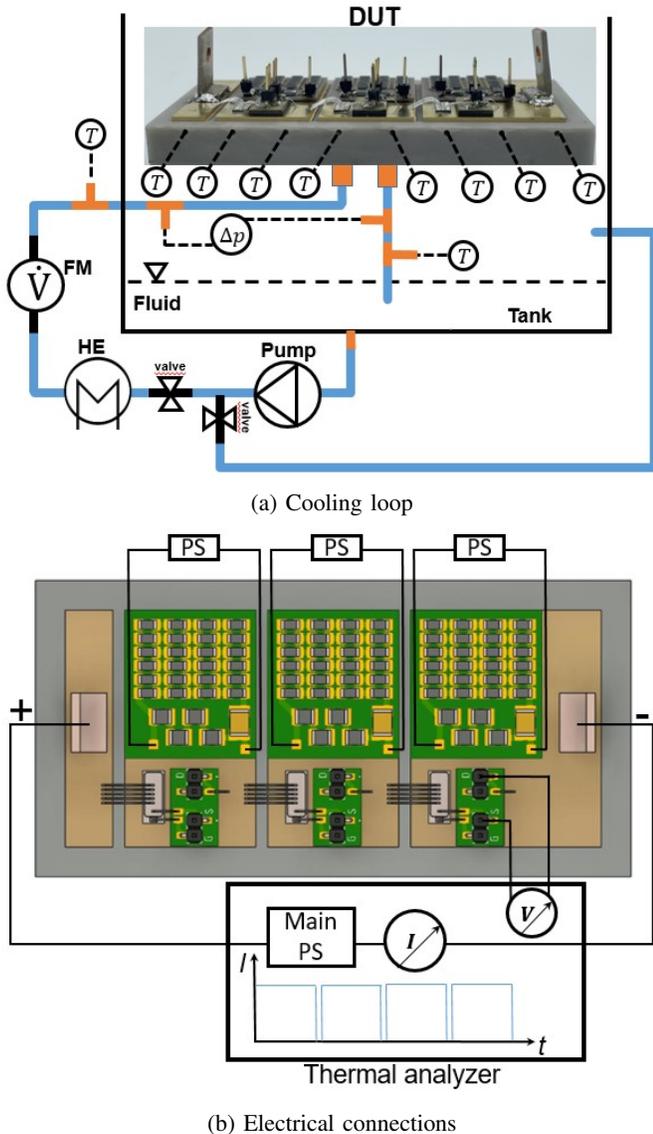


Fig. 7: schematic test setup of the cooling loop and electrical connections

Analysis Tech) for precise measurement of R_{th} . A schematic illustrating the electrical and hydraulic connections can be found in Fig. 7. Regarding the liquid circuit, water is pumped into the DUT, with valves allowing for flow-rate adjustments, and a flow meter (FM) measures the flow rate. To maintain the circuit's temperature at 40°C , a heat exchanger (HE) is incorporated. The pressure drop (Δp) is measured between the inlet and outlet to assess hydraulic performance. During the testing process, a power of 120 W is applied to each SiC die. To supply power to the snubbers, a power supply is connected to each of them, ensuring consistent operation throughout the experiment.

A. R_{th} characterisation

The thermal resistance (R_{th}) of semiconductor devices is measured with a temperature-sensitive parameter, the forward

voltage drop of the body diodes of the MOSFETs [8]. Three power supplies (not presented in Fig. 7b) are used to apply -5 V bias between gate and source of each MOSFET and ensure they are fully blocked. Before initiating thermal measurements, the semiconductor devices are calibrated in a lab oven. The oven allows precise control of the temperature of the devices. The calibration process involves recording the voltage drop between the source and drain at various temperature settings. To limit self-heating effects, the corresponding V_{DS} value is monitored by the thermal analyzer at a low reading current (5 mA). A calibration curve is generated, establishing the relationship between the voltage drop V_{DS} and the corresponding junction temperature (T_j). During the actual thermal test, the thermal analyzer utilizes this calibration curve to determine the junction temperature by measuring the voltage drop V_{DS} . The measurement is performed during the device operation with the voltage drop recorded at a known power dissipation level. After determination of the junction temperature, the thermal resistance can be calculated by dividing the temperature difference between the junction and coolant's inlet temperature by the power dissipation. Additionally, the thermal impedance of the device can also be measured, representing its transient thermal response.

B. Test results

Fig. 8 presents a comparison between the maximum measured and simulated thermal resistances for various copper spreader thicknesses as a function of pumping power. The green area in the graph refers to the target area ($R_{th} < 0.5\text{ K/W}$). The results obtained from CFD show a remarkable agreement with the experimental data. Thicker copper exhibits enhanced cooling performance due to its superior heat dissipation capability. Specifically, the thermal resistance decreases from 0.41 K/W with $300\text{ }\mu\text{m}$ copper thickness to 0.36 K/W with 1 mm copper thickness at a water flow rate of 3 L min^{-1} . This corresponds to $0.1177\text{ cm}^2\text{K/W}$ thermal resistivity. Consequently, a junction to fluid temperature difference of 43.2°C is observed at 120 W power dissipation (366.8 W/cm^2 for each die). Assuming that the thermal resistance remains constant, the cooler would be capable of dissipating about 510 W/cm^2 (166.7 W per die) at a temperature difference of 60°C .

Fig. 9 illustrates the measured thermal impedance for the three dies at water flow rates of 1 L min^{-1} and 3 L min^{-1} for the cooler with 1 mm copper thickness. All curves demonstrate nearly identical behavior, differing only at the steady-state value (thermal resistance). At low flow rates, slight differences in thermal resistances between chips can be observed. However, these differences are reduced at higher flow rates (3 L min^{-1}), where all curves coincide.

V. CONCLUSION AND OUTLOOK

This work presented an integrated cooling system tailored for high voltage ($> 20\text{ kV}$) and power density semiconductors. The cooling design specifically focused on a module consisting of six 3.3 kV SiC MOSFETs ($3.676 \times 8.9\text{ mm}^2$) and six snubbers. To streamline the manufacturing process, thermal

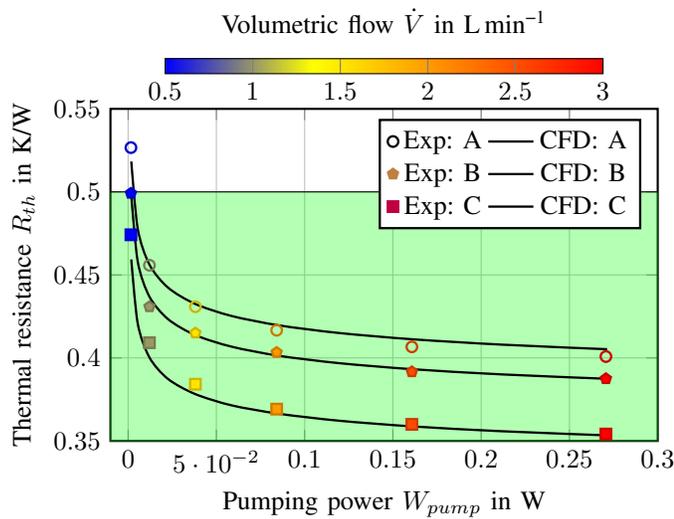


Fig. 8: The measured and calculated maximum thermal resistance as a function of pumping power for different spreader thicknesses; A: 300 μm , B: 500 μm , C: 1000 μm copper

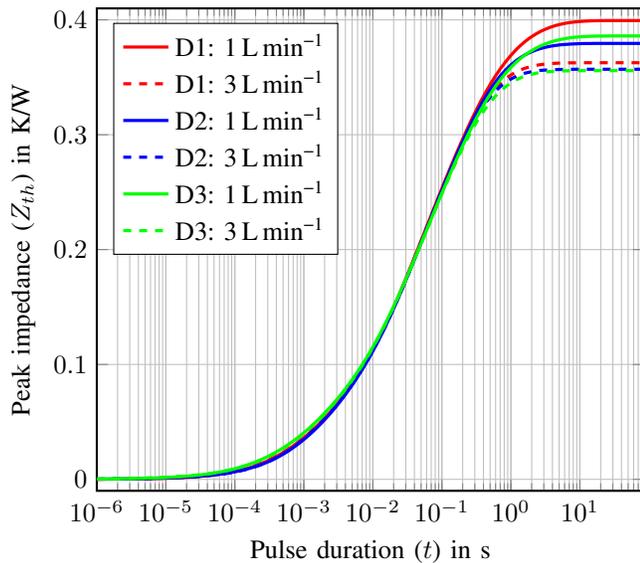


Fig. 9: Measured thermal impedance (Z_{th}) for the three dies of the cooler with 1 mm copper at 1 L min^{-1} and 3 L min^{-1} water flow rates

test and reduce costs, the module incorporates two identical AlN cooler configurations (submodules), enabling efficient thermal testing. The investigation involves three coolers, each comprising three SiC dies and three snubbers, with different copper spreader thicknesses. Numerical and experimental analysis are conducted to evaluate their performance. The cooling design combines inline and staggered pin structures, along with jet impingement and channel-flow cooling concepts, to enhance cooling efficiency. The results of simulations and experiments demonstrate a remarkable agreement, indicating that low and uniform thermal resistances for the three dies are

achieved. The thermal resistivity obtained is 0.118 $\text{cm}^2\text{K/W}$, enabling effective cooling of devices with power losses of up to 510 W/cm^2 at a junction to coolant temperature difference of 60 $^\circ\text{C}$. The results also demonstrate that despite the use of high thermal conductivity ceramic (AlN) material, there is a clear benefit in using a thick copper heat spreader between the dies and the heatsink: the thermal resistance of the cooler is reduced by approximately 12% for a 1 mm spreader with respect to the 300 μm thick spreader.

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