3-Phase 7-Level Multiplexed Converter for Medium-Voltage AC Applications

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Space Vector Modulation Strategy for a Three-Phase 7-Level Multiplexed Converter

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***Abstract*–This paper presents a novel Space Vector Modulation (SVM) strategy for the three-phase 7-level Multiplexed Converter (3Φ7L M_LM_XC) in high-power AC applications. The main idea of the proposed SVM is to use the dq-coordinate to rapidly find the switching triangle enclosing the reference vector in the 7-L space vector diagram. Then all available switching sequences and vector duty cycles are pre-allocated on look-up tables to speed up the algorithm in embedded digital platforms. All steps of the proposed SVM are implemented in half one sector that can be implemented with a minimum computational burden. The proposed algorithm can improve the quality of the waveforms and avoid the intrinsic forbidden states, preventing the catastrophic failure of the power conversion system. The algorithm has been implemented in a field-programmable gate array (FPGA) and tested using the Hardware-In-the-Loop (HIL). This paper presents results under different operating conditions to verify the proposed SVM strategy.**

I. Introduction

In the last few years, the requirements of high voltage and high-power power conversion systems have been intensively addressed because of the persistent increase of installed Renewable Energy Sources (RES) generation capacities, predominantly photovoltaic and wind turbines. With these applications' constantly increasing power ratings, voltage increasing, and current reduction allow for the use of smaller conductors, leading to considerably reduced cost, size, and weight of the system. Thus, multilevel topologies are the most promising solution for the mentioned applications [1]. Several multilevel topologies and their control strategies have been proposed in literature [2], [3]. However, the complexity of multilevel modulation strategies and control algorithms have been a significant problem for their use in industrial applications, especially when the number of converter levels increases [4]. The main modulation strategies for the multilevel converter are the carrier-based sinusoidal pulse width modulation (SPWM) techniques and the space vector modulation [5], [6]. In the SPWM, each phase of the multilevel converter is controlled separately, and three-phase sinusoidal signals are compared with the triangular carrier waveform arranged in different ways. Depending on the arrangement of the carriers, different techniques have been proposed over time, such as Phase Disposition (PD), Phase Opposition Displacement (POD), and Alternative Phase Opposition Displacement (APOD) [7]. As shown in [7], for a given multilevel topology, the phase disposition (PD) method gives rise to the lowest harmonic distortion. On the other hand, the SVM technique identifies the switching states of a multilevel converter as a point in complex space. The three closest switching states are then selected with duty cycles calculated to achieve the same volt-second average as the sampled reference phasor [8]. The SVM modulation technique presents advantages compared to classical carrier based PWM modulations [5]. During the years, more SVM techniques for multilevel converters have been proposed to fill some problems of the topologies, such as capacitor voltage balancing, common-mode voltage elimination, and modulation index extension [9]. The SVM algorithm can be categorized in 2-D and 3-D versions [10]. The 2 -dimensional SVM algorithm for modular multilevel converters is presented in [10]. However, this method uses multiple overlapped two-level and three-level hexagons instead of a single multilevel hexagon. The overlapping effect gives similar switch patterns, allowing voltage balance across the full bridges. A 2-dimensional SVM implementation scheme has been proposed in [11] to facilitate direct determination of the space vector location without the need to identify the sub-triangle number. In this case, the switching pulses can be generated without using the lookup table. The switching pulses are generated for any n-level converter by eliminating the lookup table. In [12], the simplified SVM algorithm based on a new coordinate system and the mapping table method has been applied to the modular multilevel converter. In this case, the SVM has been implemented in 2 dimensions, called H-D coordinates, independent of level numbers. Moreover, the authors assert that the SVM can operate well with various modulation ratios and level numbers. The three-dimensional space vector modulation for a four-leg multilevel diode clamped converter has been proposed in [13]. In the cited paper, the SVM has been realized in *ABC* coordinates instead of using $\alpha\beta\gamma$ coordinates. In [14], the SVM algorithm in the αβγ coordinate has been presented to be applied to the NPC four-leg converter. The $\alpha\beta\gamma$ representation offers exciting information about the zero-sequence component of both currents and voltages (proportional to the γ coordinate). However, the change of reference frame has to be carried out, which implies complex calculations. Additionally, the three-dimensional (3-D) representation of the switching vectors in αβγ is challenging to understand. The SVM algorithm has been presented in [15] to solve the voltage unbalance problem across the flying

capacitors in a Nested-NPC converter. Here, the SVM has been implemented in αβ coordinates and uses the specific combinations of existing space vectors to produce virtual vectors with zero average currents flowing through flying capacitors so that the voltage ripples are reduced. A hybrid modulation strategy for a medium-voltage hybrid seven-level Active-NPC converter is presented in [16]. The hybrid modulation consists of two paralleled processes, the low-frequency modulation applied to the Active-NPC converter and a high-frequency SVM in αβ coordinates applied to the H-bridge converters connected at the output of each NPC phase.

This paper aims to create the SVM modulation technique for a new three-phase 7-level Multiplexed Converter (3Φ7L M_LM_XC). The proposed SVM has the following features.

1. Self-identification for the adjacent switching states of the reference voltage vector in *dq* coordinates.
2. Implementation of the algorithm in half one sector in order to reduce the computational burden.
3. Generalizing switching sequences using the look-up tables implemented on the FPGA to speed up the algorithm.
4. Improve the quality of the three-phase currents at different modulation index.

The remaining part of the paper proceeds as follows. In Section II, the multilevel topology is presented. In section III, the SWM algorithm is deeply discussed. In Section IV, the effectiveness of the proposed SVM is verified and validated through HIL results. Section V concludes the paper.

II. Topology Analysis of the 3Φ7L M_LM_XC

The 3Φ7L M_LM_XC topology is illustrated in Figure 1, in which two Flying Capacitors (FCs) are cascaded with a three-phase Neutral Point Clamped (NPC) converter.

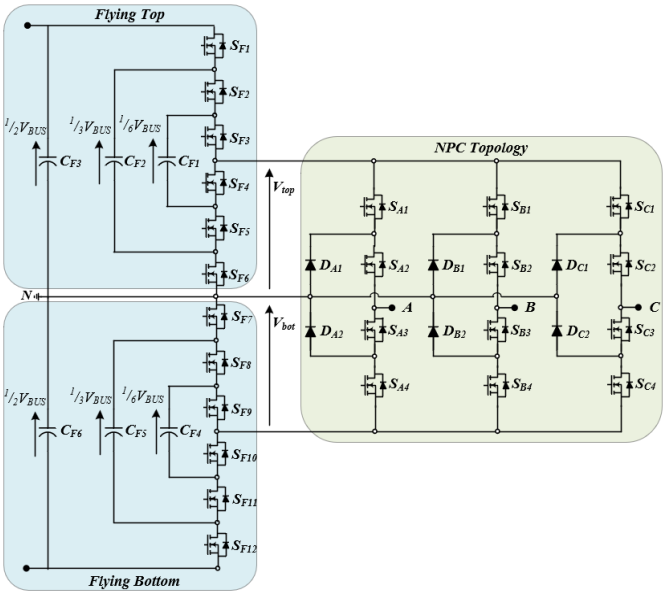

Figure 1: Three-phase 7-level Multiplexed Converter (3Φ7L M_LM_XC) topology.

The term multiplexed arises precisely from combining the two multilevel topologies without coupling them with passive elements. The voltage across the top and bottom FCs is $^1/_2V_{BUS}$, while the voltage across the flying capacitors C_{F1} (C_{F4}), C_{F2} (C_{F5}), C_{F3} (C_{F6}), is $^1/_6V_{BUS}$, $^1/_3V_{BUS}$ and $^1/_2V_{BUS}$. The top FC controls the positive DC-bus, while the bottom FC manages the lower part of the DC-bus. In each converter phase, the phase-to-neutral output voltage can provide seven voltage levels, 0, $\pm^1/_2V_{BUS}$, $\pm^1/_3V_{BUS}$, $\pm^1/_6V_{BUS}$. The benefit of the proposed topology is the low voltage stress across the power semiconductors, which enables low-cost silicon components or SiC devices can be used to improve efficiency and power density. In fact, the maximum blocking voltage $V_{BL(max)}$ across the power semiconductors located in the FC1 and FC2 (S_{F1},…S_{F12}) is $^1/_6V_{BUS}$, while the maximum blocking voltage of the power semiconductors placed in the three-phase NPC converter (S_{x1}, S_{x2}, S_{x3}, S_{x4}, D_{x1}, D_{x2} with $x \in \{1, 2, 3\}$) is $^1/_2V_{BUS}$. The state variables related to the phase to neutral voltages V_A, V_B, V_C are indicated with s_1, s_2, s_3, respectively. The variable s_i, with $i \in \{1, 2, 3\}$ can assume seven integer values -3, -2, -1, 0, 1, 2, 3. Thus, as listed in Table I, each state variable s_i is associated with the output phase-to-neutral switching voltages V_x,.

Table I. State variable s_i as a function of phase-to-neutral voltage V_x.

State variable s_i	Phase-to-neutral voltage V_x
-3	$-^1/_2V_{BUS}$
-2	$-^1/_3V_{BUS}$
-1	$-^1/_6V_{BUS}$
0	0
1	$^1/_6V_{BUS}$
2	$^1/_3V_{BUS}$
3	$^1/_2V_{BUS}$

For example, the space vector state (s_1 s_2 s_3)=(1 0 -2) is related to the three-phase output voltage equal to $^1/_6V_{BUS}$, 0, $-^1/_3V_{BUS}$, respectively. Figure 2 shows the space vector diagram of the 3Φ7L M_LM_XC in *ABC* coordinates.

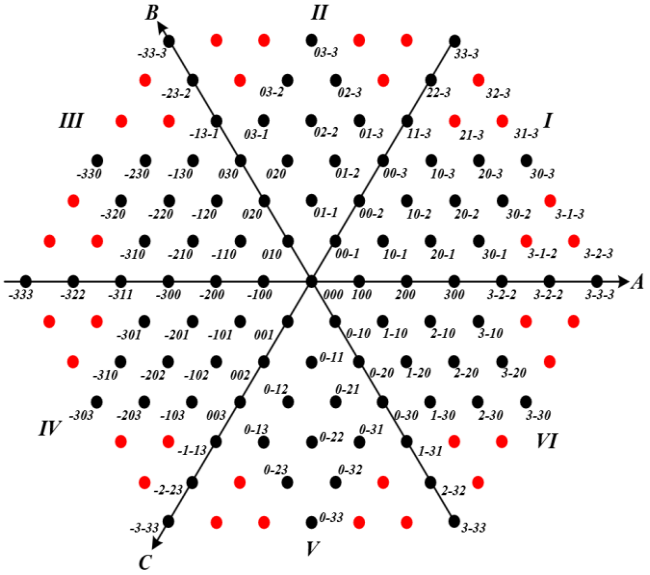

Figure 2. Space vector states for 3Φ7L M_LM_XC in *ABC* coordinates.

The hexagon can be divided into six sectors, where each sector is an equilateral triangle. Theoretically, the number of converter states is 2^{24}, of which 127 states are non-redundant. These 127 states are combined to synthesize the rotor reference vector v_{ref} in *ABC* coordinates (and subsequently in the *dq* plane). However, only 91 states are permitted, and the remainder are forbidden. The forbidden states are highlighted in red Figure 2. For instance, the state vector (3 -1 -2), highlighted in red in sector I, implies that phase A is at $^1/_2V_{BUS}$, phase B is at $-^1/_6V_{BUS}$,

and phase C is at $-^1/_3V_{BUS}$. This switching state is not allowed since phases B and C of the NPC inverter cannot have $-^1/_6V_{BUS}$ and $-^1/_3V_{BUS}$ simultaneously, given that the negative DC-bus is shared through the phases, as illustrated in Figure 3. Thus, the 3Φ7L M_LM_XC configuration has states that cannot be used to synthesize the reference vector. Additionally, the reference vector is synthesized using only three state vectors, indicated with V_1, V_2, V_3, in each switching period T_{sw}.

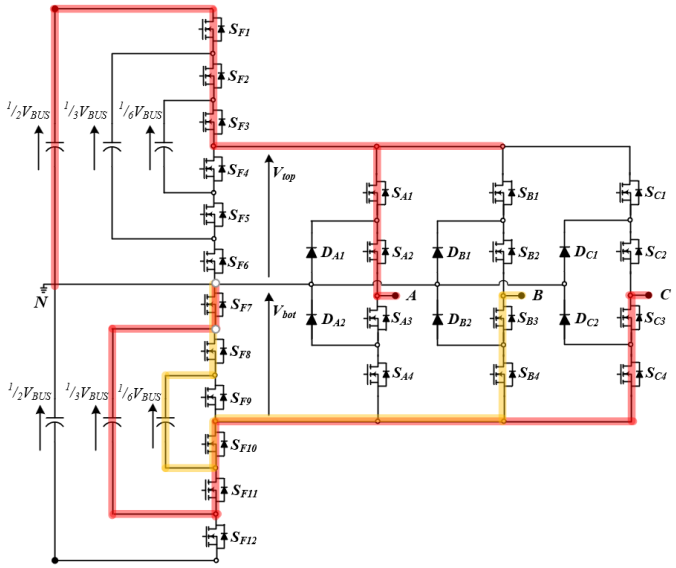

Figure 3. Forbidden space state vector (3 -1- 2) for 3Φ7L M_LM_XC in *ABC* coordinates.

III. Proposed SVM Algorithm for 3Φ7L M_LM_XC

The flowchart of the proposed SVM algorithm is shown in Figure 4. The first step of the algorithm performs the transformation of the reference vector in the *dq* coordinate. The first sector of the hexagon is split into different sub-areas, which have different shapes. In each sub-area, three state vectors are identified. Once the area has been recognized, the corresponding coordinate of the vertices in the *dq* axis is determined (V_{1d}, V_{2d}, V_{3d}), (V_{1q}, V_{2q}, V_{3q}).

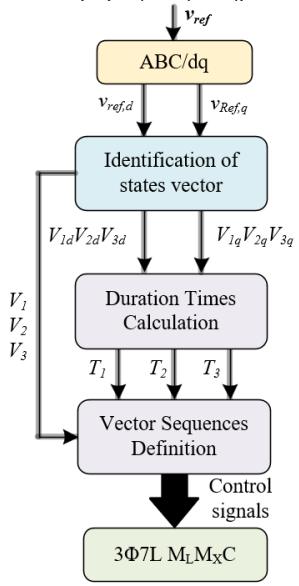

Figure 4. Flowchart of the space vector modulation algorithm for 3Φ7L M_LM_XC.

In the next step, the duration times T_1, T_2, T_3 of each state vector is computed. Finally, the state vectors at the corresponding time are applied to the converter. For each state vector, 24 gate signals are sent to command the power switches of the converter.

A. *ABC to dq coordinates*

To achieve the state vectors and the corresponding time of application is helpful to change coordinates from an *ABC* reference to a *dq* stationary cartesian reference. Figure 5 shows the projection of sector I in the *dq* plane considering the Clarke transformation given in (1), where the forbidden states are highlighted in red. It can be seen that sector I of the *dq* plane is divided into two different zones: green and yellow.

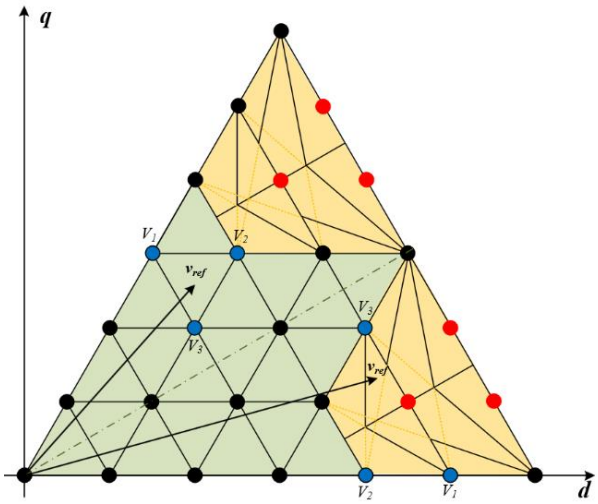

Figure 5. Sector I in *dq* coordinate of space vector states.

$$\begin{bmatrix} V_{i,d} \\ V_{i,q} \\ V_{i,0} \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix}\begin{bmatrix} s_{i,1} \\ s_{i,2} \\ s_{i,3} \end{bmatrix} \quad (1)$$

The linear zone is emphasized in the green zone, while the non-linear area is highlighted in yellow. The linear and non-linear zones, in which the reference vector $\boldsymbol{v_{ref}}$ moves, can be divided into many sub-areas. When $\boldsymbol{v_{ref}}$ is located in one of the sub-areas, the nearest three state vectors V_1, V_2, V_3 are selected to synthesize the reference vector by forming the switching sequence over one switching period T_{sw}. For instance, looking at Figure 5, two reference vectors $\boldsymbol{v_{ref}}$ are considered: one in the linear zone and the other in the non-linear zone. The corresponding state vector is highlighted in blue for each vector $\boldsymbol{v_{ref}}$.

B. *Identification of states vector*

To identify the right triangle, which contains the head of the reference voltage vector, it is possible to consider only half of the sector I due to the symmetry. By decreasing the sub-areas necessary for the modulation, the computational burden of the algorithm is strongly reduced. As a result, Figure 5 can be simplified in Figure 6.

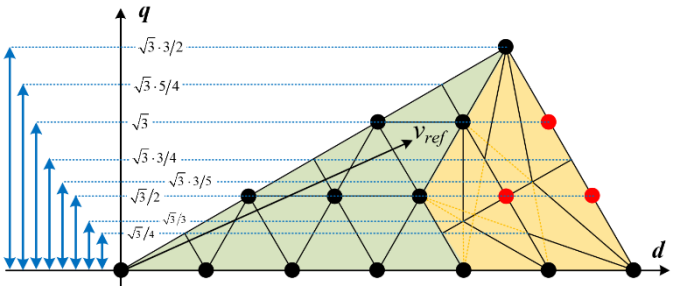

Figure 6. Reduced sector I. Space vector states between 0° and 30°.

In order to understand the space vectors, it is necessary to know the sub-area in which the reference vector falls. To do that, two comparisons are necessary along the *q*- and *d*- axis. The *q* coordinate of the reference vector $v_{ref,q}$ is compared to the quotation highlighted in blue in Figure 6. The quotations have been obtained by performing the geometrical analysis of the triangles. After that, an analogous comparison has been made for $v_{ref,d}$. If the reference vector falls in the triangle where the vertices are highlighted in blue in Figure 7, along d-axes are derived several boundary points painted in violet, drawn like squares, of d-coordinates, named $d_1 \ldots d_N$. Comparing $v_{ref,d}$ with $d_1 \ldots d_N$ values, the triangle is identified.

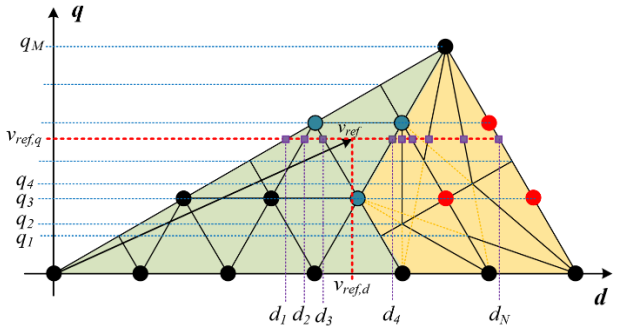

Figure 7. Example of identification of space vector state.

All the sub-areas are equilateral triangles when the reference vector v_{ref} is in the linear zone. The vertices of the tringles identify the vector state necessary for the modulations, as highlighted by the blue dot in Figure 7. The reference vector v_{ref} is always synthesized in the non-linear zone using three state vectors. The corresponding vectors depend in which sub-area the reference vector v_{ref} falls.

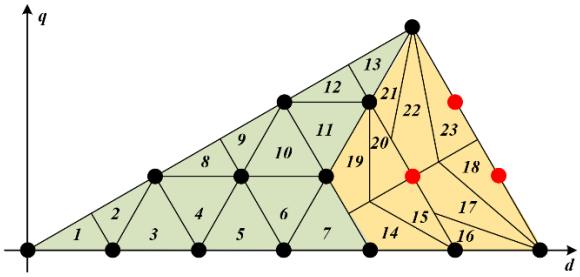

Figure 8. Numbers of sub-areas of half sector I.

Each sub-area has been identified with a number, as illustrated in Figure 8. The vector states V_1, V_2, V_3 for each sub-area are listed in Table II.

Table II. Number of sub-area and corresponding state vectors

Number of sub-area	State vectors V_1, V_2, V_3
1	V_1=(0, 0, -1), V_2=(0, 0, 0), V_3=(1, 0, 0)
2	V_1=(0, 0, -1), V_2=(1, 0, -1), V_3=(1, 0, 0)
3	V_1=(1, 0, -1), V_2=(1, 0, 0), V_3=(2, 0, 0)
4	V_1=(1, 0, -1), V_2=(2, 0, -1), V_3=(2, 0, 0)
5	V_1=(2, 0, -1), V_2=(2, 0, 0), V_3=(2, 0, 0)
6	V_1=(2, 0, -1), V_2=(3, 0, -1), V_3=(3, 0, 0)
7	V_1=(3, 0, -1), V_2=(3, 0, 0), V_3=(3, -1, -1)
8	V_1=(1, 0, -2), V_2=(1, 0, -1), V_3=(2, 0, 0)
9	V_1=(1, 0, -2), V_2=(2, 0, -2), V_3=(2, 0, -1)
10	V_1=(2, 0, -2), V_2=(2, 0, -1), V_3=(3, 0, -1)
11	V_1=(2, 0, -2), V_2=(3, 0, -2), V_3=(3, 0, -1)
12	V_1=(2, 0, -3), V_2=(2, 0, -3), V_3=(3, 0, -2)
13	V_1=(2, 0, -3), V_2=(3, 0, -3), V_3=(3, 0, -2)
14	V_1=(3, -2, -2), V_2=(3, -1, -1), V_3=(3, 0, -1)
15	V_1=(3, 0, -2), V_2=(3, 0, -1), V_3=(3, -2, -2)
16	V_1=(3, -3, -3), V_2=(3, -2, -2), V_3=(3, 0, -1)
17	V_1=(3, -3, -3), V_2=(3, -2, -2), V_3=(3, 0, -2)
18	V_1=(3, 0, -3), V_2=(3, 0, -2), V_3=(3, -3, -3)
19	V_1=(3, 0, -2), V_2=(3, 0, -1), V_3=(3, 0, -1)
20	V_1=(3, -2, -2), V_2=(3, -1, -1), V_3=(3, 0, -2)
21	V_1=(3, 0, -3), V_2=(3, 0, -2), V_3=(3, -1, -1)
22	V_1=(3, -2, -2), V_2=(3, -1, -1), V_3=(3, 0, -3)
23	V_1=(3, -3, -3), V_2=(3, -2, -2), V_3=(3, 0, -3)

C. *Duration Times Calculation*

Afterward the space vector states are obtained, the reference voltage vector $\boldsymbol{v_{ref}}$, which is synthesized by the three adjacent voltage space vectors, can be described as in (2), where $T_{sw}={}^1/_{fsw}$ is the switching period, V_{1d}, V_{2d}, V_{3d} and V_{1q}, V_{2q}, V_{3q} are the adjacent basic voltage space vectors and T_1, T_2, and T_3 are the corresponding action times.

$$\begin{bmatrix} V_{1d} & V_{2d} & V_{3d} \\ V_{1q} & V_{2q} & V_{3q} \\ 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} T_1 \\ T_2 \\ T_3 \end{bmatrix} = \begin{bmatrix} v_{ref,d} T_{sw} \\ v_{ref,q} T_{sw} \\ T_{sw} \end{bmatrix} \quad (2)$$

Since the vector state and the corresponding time are commutated in each switching time, the smaller the switching period, the better waveforms will be.

D. *Vector Sequences Definition*

The switching sequences for all types of triangles, where the sequence V_1, V_2, V_1, V_1, V_3, V_1 is performed two times. The time duration of each point of the triangle, V_1, V_2, V_3, are listed in Table III.

Table III. Space vectors as a function of application time.

Sequence	**Vectors**	**Application time**
1	V_A	${}^1/_8 \cdot T_1$
	V_B	${}^1/_2 \cdot T_2$
	V_A	${}^1/_8 \cdot T_1$
	V_A	${}^1/_8 \cdot T_1$
	V_C	${}^1/_2 \cdot T_3$
	V_A	${}^1/_8 \cdot T_1$
2	V_A	${}^1/_8 \cdot T_1$
	V_B	${}^1/_2 \cdot T_2$
	V_A	${}^1/_8 \cdot T_1$
	V_A	${}^1/_8 \cdot T_1$
	V_C	${}^1/_2 \cdot T_3$
	V_A	${}^1/_8 \cdot T_1$

This sequence has been selected to improve the quality of the waveforms. The vector states are associated with the corresponding application time using the carrier signal, as illustrated in Figure 9. As seen, sequence 1 is applied in half switching period.

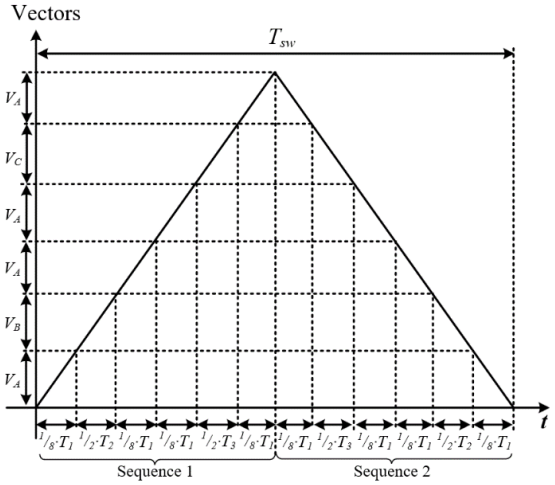

Figure 9. Vector sequences and application time in one switching period.

IV. Experimental Verification

The proposed SVM algorithm has been evaluated considering the DC side of the converter connected at six constant sources, where the total DC-bus is equal to 3000V. The converter's output is connected to a three-phase load R_L through the filter inductance L_f, where L_f=500µH and R_L=5Ω, as illustrated in Figure 10. The switching frequency f_{sw} is equal to 5kHz, the dead-time DT is set at 1µs, and the fundamental frequency f_0 is equal to 50Hz. The relative amplitude of the output voltage is often referred to as the modulation index m. Even in the proposed SVM, the modulation index m is between 0 and $2/\sqrt{3} \approx 1.15$. The 3Φ7L M_LM_XC converter has been real-time emulated by the eHS64 FPGA solver from OPAL-RT, as illustrated in Figure 11.

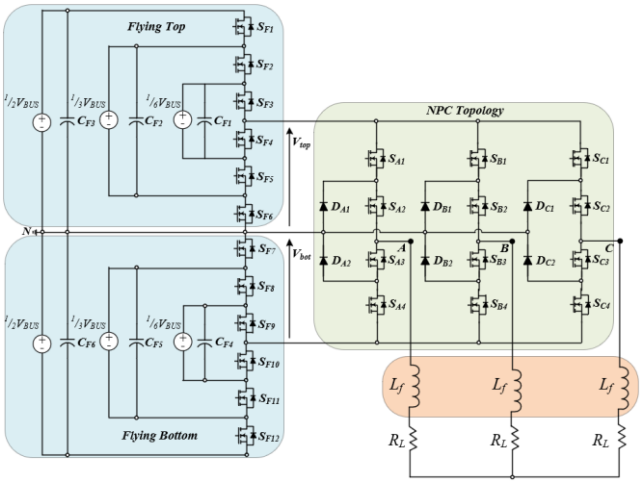

Figure 10. 3Φ7L M_LM_XC connected to the inductor filter and loads.

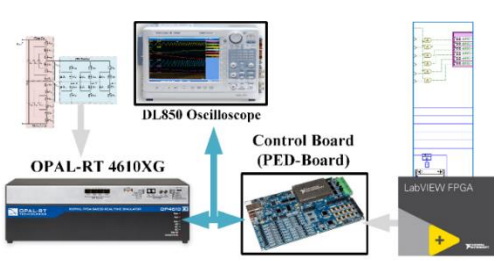

Figure 11. Real-Time setup for testing the 3Φ7L M_LM_XC SVM algorithm.

The SVM algorithm has been implemented on the PED-Board® controller directly on the FPGA, taking advantage of the LabVIEW graphical environment, as illustrated in Figure 12. As can be seen, the most demanding tasks, such as the SVM algorithm, protection, and measurement, runs on the FPGA target. The real-time target executes the Graphical User Interface (GUI) and sets the controllers like the reference vector, switching frequency, and fundamental frequency. The non-deterministic tasks, such as handling the GUI, runs on the host target. The Ethernet link physically realizes communication between the host and RT target.

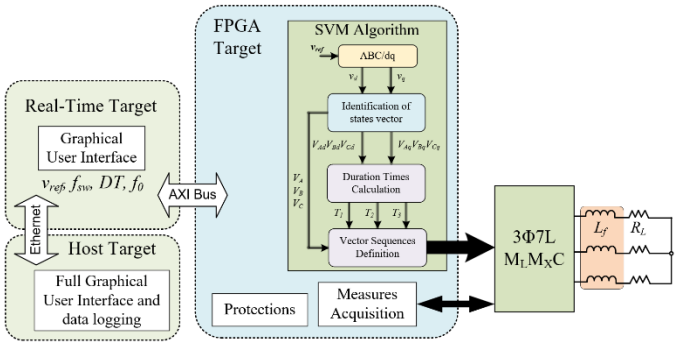

Figure 12. Implemented block scheme of the SVM algorithm in LabVIEW.

Figure 13 shows the voltage and current waveforms at a steady state when the modulation index m equals 0.5. When the modulation index m=0.5, the reference space vector falls in the linear area. As can be seen from Figure 13a, the phase-to-neutral switching voltages show seven voltage levels. Each phase provides zero voltage for approximately 60° since the same positive and negative DC-bus is shared between three-phase of the NPC. Moreover, the peak of the three-phase voltages across the resistive load is equal to 700V, as illustrated in Figure 13b. Figure 13c and Figure 13d illustrate the line-to-line voltages before and after filters. As can be seen, the switching line-to-line voltages show seven voltage levels, while the peak of the line-to-line voltages is close to 1300V. Furthermore, it is possible to recognize four voltages provided by the top and bottom FCs, as illustrated in Figure 13e. Finally, Figure 13f illustrates the three-phase current flowing into resistive loads.

The total harmonic distortion of the phase-to-neutral voltage (THD_V), line-to-line voltages (THD_{VLL}) and phase current (THD_I) are 2%, 1%, 1.5%, respectively.

The converter works in the non-linear zone when the modulation index m crosses the 2/3 value. The voltage and current waveforms at a steady state, when the modulation index m is equal to 1.15, are shown in Figure 14. In this case, as illustrated in Figure 14a and Figure 14c, the number of levels of the switching phase-to-neutral and line-to-line voltages is different from seven since the forbidden state must be avoided. However, the phase-to-neutral voltage, line-to-line voltages and phase current on the resistive load are perfectly sinusoidal waveforms, as illustrated in Figure 14b, Figure 14d, and Figure 14f. Additionally, the voltage provided by the top and bottom FCs shows two voltage levels, as illustrated in Figure 14e.

The total harmonic distortion of the phase-to-neutral voltage (THD_V), line-to-line voltages (THD_{VLL}) and phase current (THD_I) are 2%, 1%, 1.5%, respectively.

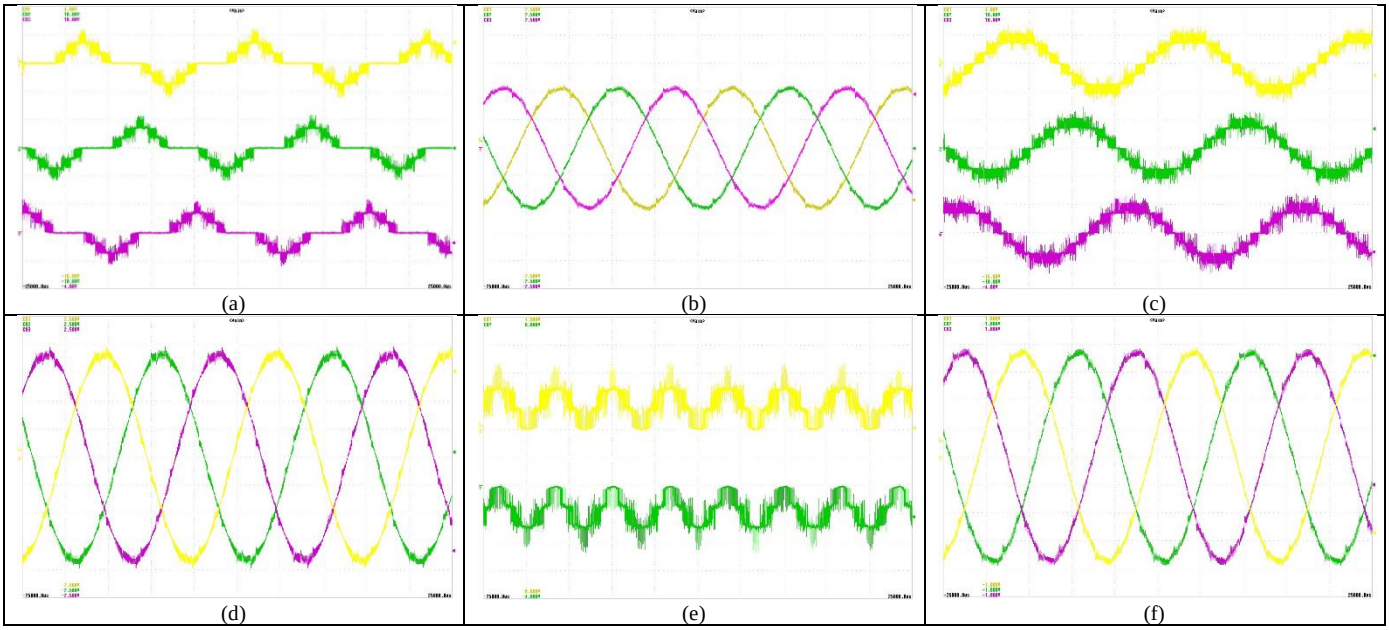

Figure 13. Waveforms at steady state at m=0.55: (a) three-phase switching voltages $V_{A(sw)}$ (yellow line) , $V_{B(sw)}$ (green line), $V_{C(sw)}$ (violet line), 1400V/div; (b) three-phase voltages V_A (yellow line) , V_B (green line), V_C (violet line), 350V/div; (c) three-phase line-to-line switching voltages $V_{AB(sw)}$ (cyan line) , $V_{BC(sw)}$, $V_{CA(sw)}$, 1400V/div; (d) three-phase line-to-line voltages V_{AB} (cyan line), 350V/div, V_{BC}, V_{CA}; (e) top DC-bus voltage $V_{top(sw)}$ (yellow line) and bottom DC-bus voltage $V_{bot(sw)}$ (violet line), 700V/div; (f) three-phase currents i_a, i_b, i_c, 20A/div. 5ms/div.

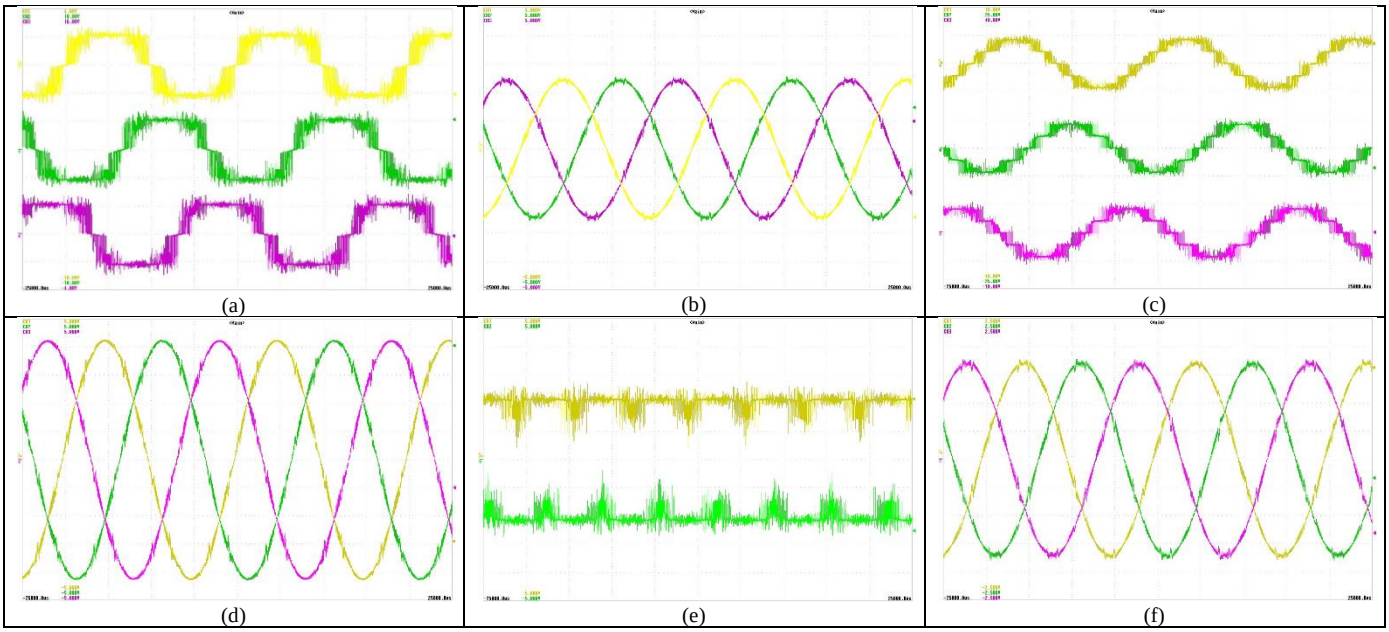

Figure 14. Waveforms at steady state at m=1.15: (a) three-phase switching voltages $V_{A(sw)}$ (yellow line) , $V_{B(sw)}$ (green line), $V_{C(sw)}$ (violet line), 1400V/div; (b) three-phase voltages V_A (yellow line) , V_B (green line), V_C (violet line), 700V/div; (c) three-phase line-to-line switching voltages $V_{AB(sw)}$ (cyan line) , $V_{BC(sw)}$, $V_{CA(sw)}$, 1400V/div; (d) three-phase line-to-line voltages V_{AB} (cyan line), 700V/div, V_{BC}, V_{CA}; (e) top DC-bus voltage $V_{top(sw)}$ (yellow line) and bottom DC-bus voltage $V_{bot(sw)}$ (violet line), 700V/div; (f) three-phase currents i_a, i_b, i_c, 50A/div. 5ms/div.

V. Conclusions

This paper proposes a new SVM algorithm to control the 3Φ7L M_LM_XC for medium-voltage applications. The proposed algorithm works in the *dq*-axis to control the multilevel converter. The proposed SVM algorithm identifies the state vector using only half sector. The identification of a triangle is based on the comparison between the reference vector and the dq-axis. The time calculation and the switching sequences are provided straightforwardly. The SVM algorithm has been implemented on the FPGA and tested using the HIL system. The results show the excellent quality of the converter's output waveforms, verifying the feasibility and validity of the proposed SVM algorithm.

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