Design and efficiency measurement of a sub-unit for a 20kW DC-DC multiphase power converter

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***Abstract*—This paper explores various design strategies for low-voltage, high current DC-DC converters, in order to optimize efficiency, volume and mass, while keeping the project as simple and cost efficient as possible by using only on-the-shelf components, including inductor and heatsinks. The impact of topologies on both efficiency and compactness is studied for a specific aeronautical application. A 2kW 3-level FCML module has been developed for a 100V to 28V DC step-down. It relies on pairs of paralleled EPC2022 GaN transistors to significantly rise converter power density. Two routing strategies to reduce parasitic switching loops are compared using computer simulations, with experimental verification. First experimental results on a prototype show an efficiency up to 98.4% for a specific power of $12.5\mathrm{kW/L}$.**

***Index Terms*—multilevel power converter, flying capacitor, GaN HEMT, paralleled transistor, efficiency, PCB layout**

I. Introduction

With the rapid increase in commercial flights in the last decades, aircraft now represent a significant impact on climate change. Their fuel consumption produces a mix of CO_2 and other greenhouse gas such as water vapor or NO_x. This mix is estimated to have 2 to 4 times the instantaneous warming impact of CO_2 [1]. Commercial flights represented 0.8% of fossil fuel emissions impact on global warming in 2000 and, following the current trends, their impact is expected to reach 5.2% by 2100 [2].

Aircraft electrification is considered a major solution to reduce the contribution of commercial flights to global warming. However, challenging the fuel-based technologies that have been optimized over the past decades with electrical solutions is still an open question, with mass reduction being one of the main issues. The present work is part of the PIPAA projet, which aims to replace a fuel-based auxiliary power unit by fuel cells to power the electrical network of a business aircraft [3]–[5].

This paper explores various design options for optimizing the DC-DC converter connecting fuel cell to the onboard electrical network in Section II. One of the main objectives is to reach high efficiency and high power density, often difficult for low voltage / high current power converters. Multilevel Flying Capacitors converters are compared based on their component count, and on their performances in terms of size (such as in [6]), weight, complexity, and losses. Section III details the development of a prototype once a topology and its components have been selected, with a main focus on hardware and routing considerations. Preliminary experimental results on a prototype are presented and discussed in IV. Section V summarizes the paper and offers prospects for future works.

II. Converter topologies & components comparison

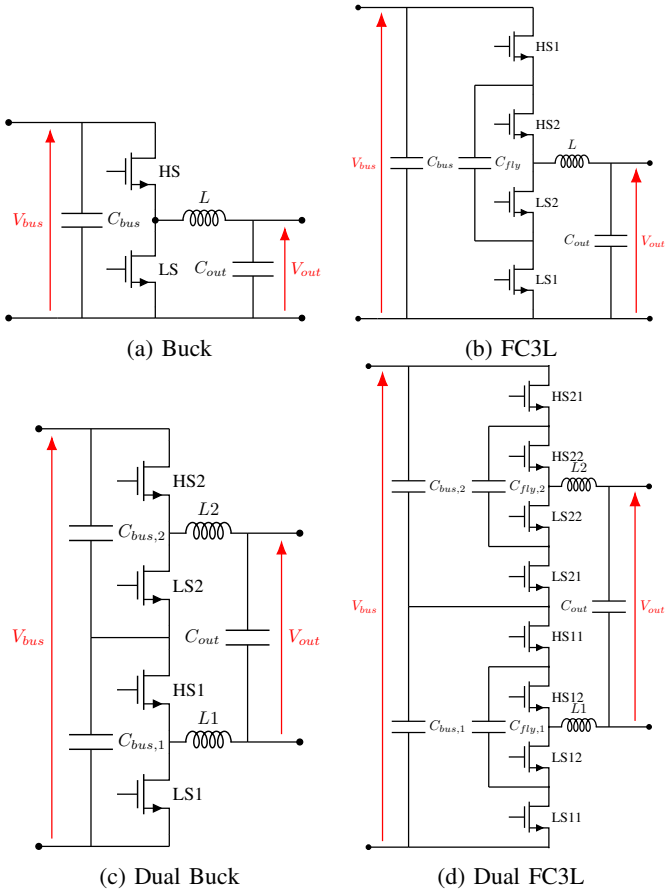
Converter output voltage is maintained at a constant $V_{out} = 28V$ by an auxiliary battery and supercapacitors that are not part of the study. Average load power consumption P_{load} is $15kW$ with a maximum at $20kW$, corresponding to a maximum output current at $715A$. Input voltage from the fuel cell V_{bus} varies between $50V$ and $110V$ depending on fuel cells power supply and cell aging. Power efficiency must be higher than 97%, while converter volume must be less than $15L$ and minimized, and weight density better than $4kW/kg$. As an additional constraint, only *on-the-shelf* components must be used, including heatsinks and inductors.

A preliminary study of topologies and available components was realized in order to determine which design principles may lead to better efficiency, and specific power. Given the very high currents (up to $715A$), paralleling obviously needs to be considered, but the number of parallel paths and the type of paralleling are degrees of freedom that still allow many options.

A. Topologies

In order to show the impact of topologies on efficiency and volume optimization, four converter topologies are have been studied (Fig.1). The classic *Buck* (Fig.1a) converter was studied as a starting point of comparison for more complex chopper topologies. A common trend is that the smaller the

breakdown voltage BV_{ds}, the more efficient the transistor is. A very common topology allowing us to reduce BV_{ds} requirement is the Flying Capacitor Multilevel (FCML) topology, first described in [7]. It was studied in its simplest form, the *3-Level Flying Capacitor* converter (FC3L) (Fig.1b). The required BV_{ds} is divided by 2, and the chopped voltage has its amplitude at $V_{bus}/2$ and its frequency doubled. *Dual Buck* converter [8] (Fig.1c) and *Dual 3-Level Flying Capacitor* converter (Fig.1d) use the previously mentioned topologies in pairs to divide the bus voltage by 2. A positive current in the output load flows through L_2 to L_1.



(a) Buck (b) FC3L

(c) Dual Buck (d) Dual FC3L

Fig. 1: Compared converter topologies in design phase

Inductors are often the largest and heaviest component in low voltage high current converters and, as such, are one of the first criteria to select a topology. For *Buck* converters, the required inductance value for a given design is given by Eq.1 :

$$L = \frac{V_{bus} \cdot D(1-D)}{f_{sw} \cdot I_{out} \cdot \Delta i_{out}} \tag{1}$$

Where V_{bus} is the voltage at the converter input, D is the duty cycle for PWM signals, I_{out} is the mean output current value, and Δi_{out} is the current ripple ratio (no unit).

Eq.1 is generalized for Dual and FCML converters in Eq.2. It will take into account the converter level N, and the region of operation $i \in \mathbb{N}^*$ of the converter, which depends on D and N such as $\frac{i-1}{N-1} < D \leq \frac{i}{N-1}$.

$$L = \frac{V_{bus} \cdot (D - \frac{i-1}{N-1})(\frac{i}{N-1} - D)}{f_{sw} \cdot I_{out} \cdot \Delta i_{out}} \tag{2}$$

It is shown that L is inversely proportional to the switching frequency f_{sw}. Having $f_{sw} \geq 100kHz$ would allow us to select some of the smallest inductors available on the market for such currents. Some silicon transistors can reach these frequencies, but the most adapted transistor technologies are *GaN-based* [9], [10]. *GaN* transistors from *EPC* are considered in Section II-D, transistors from *GaNSystems* were also studied but are not presented for the sake of brevity.

Eq.2 also shows that higher converter levels need lower output inductance value to get the same current ripple than a basic *Buck*. However it doesn't necessarily result in lower inductance mass and volume with available components. With $V_{bus} = 115V$, $I_{out} = 35A$, and switching frequency set at $f_{sw} = 200kHz$, an output current ripple Δi_{out} at 20% implies $4\mu H \leq L \leq 16\mu H$ depending on the topology. Only a few on-the-shelf components can match these specifications, the most interesting ones are the *IHLP-8787MZ-51* at $4.7\mu H$, $3.3\mu H$ and $2.2\mu H$ by *Vishay*. All three of them have the same volume ($22\times22\times13mm^3$) and mass. Having multiple of these inductors in series still results in better efficiency and volume than using another component series.

B. Losses

IHLP-8787MZ-51 AC and DC losses were estimated using *Vishay*'s online simulator. Transistor losses were estimated based on *LTSpice* models and the manufacturer's online loss simulator. Switching losses E_{sw}, Reverse Recovery losses E_{rr} and Conduction losses E_{cond} were separately determined as functions of drain to source voltage V_{ds} and output current I_{out}. A summary of the studied transistors typical characteristics extracted from their datasheet is presented in TableI.

A simple 2D thermal model was used to estimate component temperature elevation. Temperature modifies ON resistance R_{dsON} and creates more losses to dissipate. This feedback loop is solved numerically.

TABLE I: Typical characteristics for studied transistors, at $T_j = 25°C$

	EPC2034C	**EPC2022**	**EPC2024**
$\mathbf{BV_{ds}}$	$200V$	$100V$	$40V$
$\mathbf{I_{ds,max}}$	$48A$	$90A$	$90A$
$\mathbf{R_{dsON}}$	$6m\Omega$	$2.4m\Omega$	$1.2m\Omega$
$\mathbf{C_{oss}}$	$641pF$	$840pF$	$1620pF$
$\mathbf{R_{\theta j,c}}$	$0.3°C/W$	$0.4°C/W$	$0.4°C/W$
$\mathbf{R_{\theta j,b}}$	$4°C/W$	$1.1°C/W$	$1.1°C/W$

C. Thermal Dissipation

Since high temperatures on these transistors degrade their performance ($R_{ds,ON}$) and their longevity, transistors junction temperatures T_j must be kept under control. The studied converter topologies are not viable without any active cooling.

The proposed thermal model for transistors cooling relies on a $6m/s$ airflow produced by a fan and a heatsink. Fan system was not considered in the current study yet, and so has

TABLE II: Performance comparison between topologies for $f_{sw} = 200kHz$, $V_{in} = 80V$ and $P_{in} = 1kW$

	Buck EPC2034C	**FC3L EPC2022**	**Dual Buck EPC2022**	**Dual FC3L EPC2024**
Transistor losses (W)	11.9	9.215	9.215	8.76
Inductor losses (W)	13.2	3.8	4.1	2.4
$\mathbf{T_{j,max}}$	$73.8°C$	$64.1°C$	$63.6°C$	$51.2°C$
efficiency	97.5%	98.7%	98.5%	98.8%
Specific Power (kW/L)	10.6	18.7	18.3	16.9

not been included in compactness and efficiency calculations for this paper. The $31 \times 31 \times 12mm^3$ *Wakefield-Vette Push Pin* heatsink has an approximate thermal resistance vs airflow of $R_{\theta hs,amb}(6m/s) = 2.25°C/W$ (datasheet). It is used in conjunction with a gap filler to drain the thermal flux from the 4 transistors it can cover. Two heatsinks are required to cover the 8 transistors required by some of the studied solutions. To enhance thermal conductivity, the whole volume covered by the heatsink is filled, allowing heat to flow from the PCB as well as transistor case.

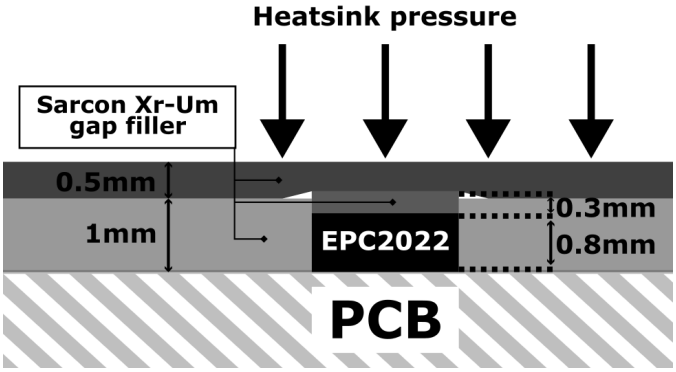


Fig. 2: Thermal interface assembly

A solid thermal pad, *Sarcon XR-Um* series by Fujipoly, serves as thermal interface material. It presents an excellent thermal conductivity of $17W{\cdot}m^{-1}{\cdot}K^{-1}$. This pad is sold in multiple widths, and special care must be taken to ensure good contact between transistor case to heatsink, as well as PCB to heatsink.

The assembly giving best results is presented in Fig.2. The additional $0.5mm$ layer will add unwanted thermal resistance to the system, but evens out width discrepancies and ensures good contact of both transistor and PCB with the heatsink. For a converter topology using 8 transistors, if thermal losses are assumed to be evenly distributed on all transistors, the equivalent junction to heatsink resistance is $R_{\theta j,hs(eq)} = 0.15°C/W$. The total equivalent resistance between idealized thermal losses and air is $R_{\theta j,amb(eq)} = 1.28°C/W$.

Using thermal pads assemblies instead of liquid gap fillers allows for a better control of the quality of the fill. Solid thermal pads don't require additional pieces to wedge the heatsink during drying, and still allow to remove cleanly the heatsink for inspection. They also benefit from their superior thermal conductivity, compared to liquid gap fillers that typically are at around $4W{\cdot}m^{-1}{\cdot}K^{-1}$. But the gains are dependent on how well PCB geometry matches with available pad widths. If *EPC* transistors were $0.1mm$ thinner, the $0.5mm$ pad layer would not have been necessary, giving $R_{\theta j,hs(eq)} = 0.11°C/W$. Another issue is the process of assembling requires care and precision to cut holes or single pads matching transistor size, and to place it without damaging any component (EPC transistors being very fragile). Thermal pads may however be very well fitted for PCB embedded transistors (such as [11], [12]) that present a completely flat surface bellow heatsink.

D. Design comparison

Losses, efficiency and specific power for each tested topology are presented in Table II for one operating point. It appears that $FC3L$ topology has a much better efficiency than $BUCK$, because it allows to use $EPC2022$, which presents better performance than $EPC2034C$ but has a lower BV_{ds}. The main improvement factor comes from better fitting between the required inductance value and the available on-the-shelf components. Indeed, BUCK topology require to use 4 *IHLP (4.7µH)* in series to maintain $\Delta i_{out} \leq 20\%$, which multiplies by 4 the inductance losses. The only serious alternative for this component would be *Standex PQ3218-6R0-50-T (6µH)*. Placing 3 of them in series would give a slightly better efficiency but would drastically decrease Specific Power because of its larger size of $32.5 \times 22.5 \times 18mm^3$. Resulting specific power would be $6.5kW/L$, 40% less than with *IHLP*.

Anticipated volume and specific power of the final converter is a key parameter in topology selection. Estimations were done using the dimensions of the required components and how they would affect PCB routing to get the area for a single phase, then multiply it by the required space between phases (biggest component height plus a margin) times the number of phases to get the $20kW$ converter final height. The inductance has a very big impact both on PCB area and converter height, which limits drastically our choice. Another issue is the heatsink size. *Wakefield-Vette Push Pin Heatsink* covers an area of $31 \times 31mm^2$, enough space to place 4 transistors under it, for a height of $15mm$. More transistors require more heatsinks and driver circuits, which results in lower specific power of Dual FC3L.

Despite *Dual FC3L* slightly better efficiency, its lower specific power and higher complexity makes the *FC3L* converter a better choice. By paralleling 2 transistors per switch and 2x$4.7\mu H$ inductors, we are able to multiply by 2 the flowing power per phase. It results in a bigger PCB (2 heatsinks and 2 inductors instead of 1) but reduces the number of phases required from 20 to 10, to reach $20kW$. It is shown in Table III that efficiency remains the same, while specific power significantly rises (+34%), making the final converter much more compact.

TABLE III: Efficiency, Temperature & Specific Power comparison between single and paralleled transistors for *FC3L*

	FC3L EPC2022	FC3L 2xEPC2022
Input Power (W)	1000	2000
Transistor losses (W)	9.215	18.24
Inductor losses (W)	3.8	7.5
T_{max}	$64.1°C$	$61.0°C$
efficiency	98.7%	98.7%
Specific Power (kW/L)	18.7	25.1

III. Development of a prototype

According to the preliminary study from Section II, a $2kW$ prototype based on the *FC3L* topology was developed. The final result is shown in Figure 3, with a final volume of $72 \times 147 \times 15mm^3$. Its specific power is $12.5kW/L$. It is half the expected specific power from estimates, the main reason being capacitors area and spacing between components for routing reasons were not estimated. This practical result is still a major achievement since paralleling 10 phases to reach the $20kW$ goal will result in a $1.6L$ converter (without including fan volume), 90% less than the maximum $15L$ volume fixed by the specifications. Choosing components and topology is only the first part of designing a converter. This section details hardware integration (such as in [**?**]), PCB parasitics, and same side paralleled transistors implementation.

A. Switching loop stray inductance

$EPC2022$ transistors have very high switching speeds. Measured rise time from $0V$ to $V_{ds} = 37.5V$ is typically $15ns$, which means that high di_{ds}/dt are generated and that special care must be taken when routing the PCB in order to limit ringing and voltage overshoot (such as in [13]). The best practice against stray inductance is to place the capacitor on the same side as transistors and use adjacent copper layers to reduce loop area [14]. Another approach for Flying Capacitor topologies is to intertwine capacitors from both sides of the switching cell [15].

Capacitors cannot be placed under transistor heatsinks, they must be moved next to it or on opposing side. Intertwining requires dedicated copper traces which reduces available copper layers for power flow. Placing intertwined capacitors on bottom layer has the less impact on power flow. Two competing PCB routing strategies were evaluated in order to determine the best approach. Same side capacitors (Fig.3 & 4a), and intertwined capacitors (Fig.4b).

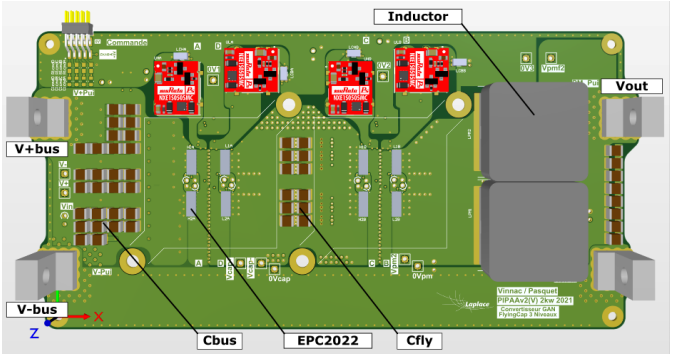
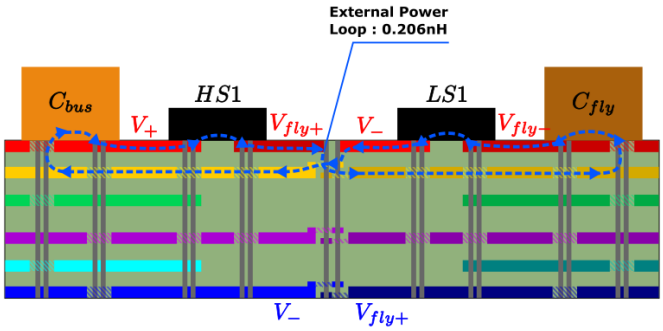
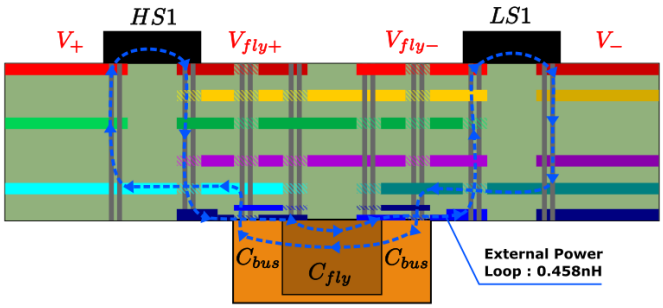


Fig. 3: Top view of the $2kW$ prototype



(a) Same side capacitors



(b) Intertwined capacitors

Fig. 4: Side view of cell 1 switching loop

Stray inductance L_{loop} was simulated for $100MHz$ on a switching cell for both PCBs, using *Ansys Q3D* software. It does not include *EPC2022* package inductance $L_{EPC2022}$, estimated at $0.1nH$ through its LTspice model. Total stray inductance is $L_{total} = L_{loop} + 2 \times \frac{L_{EPC2022}}{2}$. Stray capacitance between power planes C_{planes} were estimated using PCB dimensions, while the *EPC2022* parasitic capacitance from the datasheet is $C_{oss}(40V) = 840pF$ and $C_{oss}(0V) = 2500pF$. The total capacitance is :

$$C_{total} = \frac{1}{\frac{1}{2*C_{oss}(40V)} + \frac{1}{2*C_{oss}(0V)}} + C_{planes} \quad (3)$$

Natural frequency for this LC circuit is :

$$F_{HF} = \frac{1}{2\pi\sqrt{L_{loop}C_{loop}}} \quad (4)$$

By using Eq.4, ringing frequency was estimated by hand, and compared with LTspice results that use more precise, manufacturer provided transistor models. Parasitic values and frequencies are presented in Table IV. They show that while stray capacitance are relatively similar, *Same-side* model has 55% less stray inductance than *Intertwined* model, making the former more promising. A prototype was then produced to verify all of the above predictions through measurements.

The first experimental results on the prototype show a ringing frequency of $156MHz$ (Figure 5) on cell 1 low side transistor drain to source voltage, which matches well with Spice simulations. V_{ds} voltage overshoot is at $50.5V$,

or 35% overshoot, far below *EPC2022* breakdown voltage $BV_{ds} = 100V$.

TABLE IV: Switching Loop Parasitics comparison between routing strategies

Model	*Same-side*	*Intertwined*
$\mathbf{L_{loop}}$ *(Ansys Q3D)*	$0.206nH$	$0.458nH$
$\mathbf{C_{planes}}$ *(estimated)*	$2.55nF$	$3.02nF$
$\mathbf{C_{total}}$	$3.80nF$	$4.27nF$
$\mathbf{F_{HF}}$ *estimated*	$147MHz$	$103MHz$
$\mathbf{F_{HF}}$ *LTspice*	$160MHz$	$102MHz$
$\mathbf{F_{HF}}$ *measured*	$156MHz$	$--$

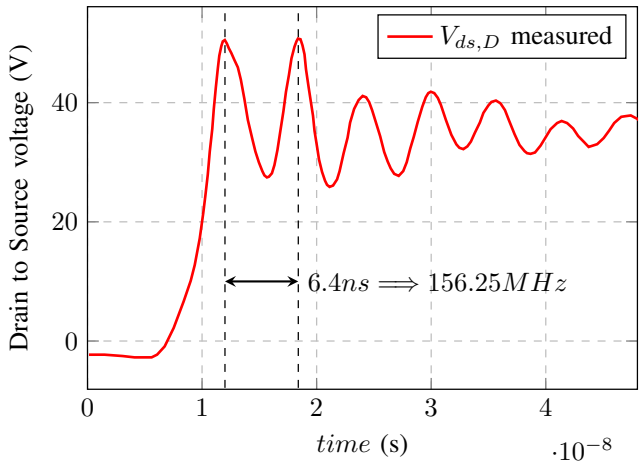
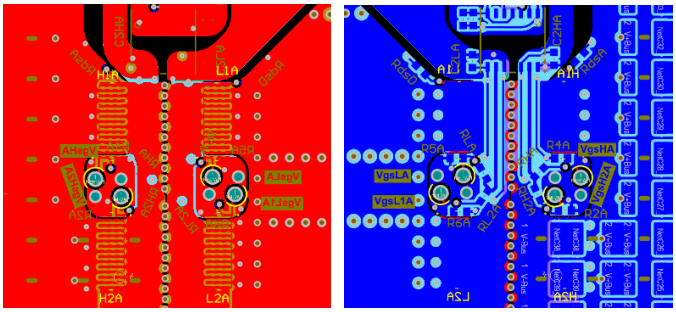


Fig. 5: Cell 1 low side transistor V_{ds} measured ringing during switching for $V_{bus} = 75V$, $I_{out} = 70A$, $deadtime = 35ns$

B. Paralleling transistors

In order to double the load current passing through a single phase, 2 transistors are placed in parallel per switch. Special care must be taken to ensure that paralleled transistors behave synchronously. Oscillations between paired transistors can be produced by asymmetrical layouts at their drains, sources or grids [16], [17]. Required gate current to turn on and off a switch is doubled. Paralleling 2 gate drivers to divide the required driver output current will inevitably lead to asynchronous switching for paired transistors because of command signal propagation delay variation. Having a single driver provide the grid current for paired transistors, however, puts a higher constraint on driver selection. Drivers must allow higher grid currents, and have the lowest internal pull-down resistance possible (or a Miller clamp) to limit the increased risk of Miller turn-on [16].

Infineon driver *2EDF7275K* was selected for its 4A/8A source/sink maximum output current, high switching speed, low internal resistances and dual channels. It allows to control both high side and low side transistors of a switching cell with a single component. The layout of a switching cell is shown in Fig.6. To ensure maximum symmetry between paralleled transistors, transistor grids are put face to face on a *driving islet* at source voltage located between power planes. Driver to grid path has to pass under power planes and only splits between transistors when it reaches the *driving islet*. PWM signals on



(a) Top layer (b) Bottom layer

Fig. 6: PCB layout of a switching cell in v2V prototype

bottom layer are shielded from power flowing above by a source plane on the adjacent layer. A common practice to cage a signal is to place vias at regular interval, as in [15] where a similar shielding issue was encountered. However, since vias would reduce the tight power path on power planes and increase asymmetry between paired transistors, it was decided instead to surround bottom grid path with 2 source paths. Blind vias were not considered for cost reasons. Experimental results show perfect synchronicity of paired transistors V_{gs} and no significant ringing or EMI issue.

IV. Experimental Losses Measurements

The next step in Evaluating *v2V* prototype performance is to measure its efficiency depending on the input voltage V_{bus} and output power P_{load}, output voltage V_{load} being fixed at $28V$ as defined by design requirements. Measurements are done by Opposition method [18], [19], as it allows great precision for high efficiency converters that are reversible in current.

Two copies of the same converter have their output terminals connected to each other, and their input terminals connected in parallel with a single voltage source. One converter has its output voltage V_{opp} regulated, while the other acts as an active load for the former, by regulating the opposition current I_{opp} flowing from one output terminal to the other. Power flows in a loop between both converters. Input voltage V_{bus} is maintained by the voltage source, while a charging current I_{bus} flows from the source to the converter loop. When I_{opp} is established, I_{bus} only serves to compensate for the total loss of the system, which means that total system losses can be directly measured with a power analyser between the voltage source and the converters, while "output power" P_{out} is measured at the output terminals of the converters. If we suppose that our converter has the same characteristics in direct and reverse mode, P_{loss} is a simple division by 2 of measured system losses. The relative error for loss measurements $\frac{\Delta P_{loss}}{P_{loss}}$ is the power analyser's precision.

An experimental setup was realized to evaluate the prototype's efficiency. First measurements were done for a fixed $V_{bus} = 75V$, which is an average voltage for the Hydrogen Fuel Cell at the converter's input, and input power $P_{in} = P_{out} + P_{loss}$ has been swept from $100W$ to $2000W$. P_{loss} was measured, and a total driver power consumption of $1.55W$ was added to it before calculating efficiency. The results are

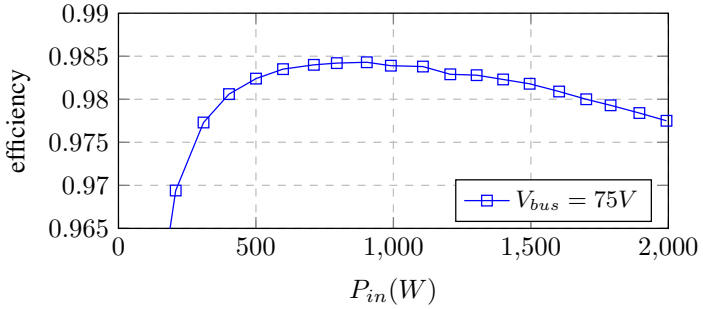


Fig. 7: Prototype's measured efficiency (driver power included) for $deadtime = 35ns$, $f_{sw} = 200kHz$

presented in Fig.7. It is shown that the converter works at up to 98.4% efficiency for $P_{in} = 1100W$, and above 98% for P_{in} between $400W$ and $1700W$.

Further testing is required for other voltages. Fan power consumption and volume still need to be evaluated, once proper optimization will be done. With the current unoptimized fan used in this setup, which has a power consumption of $4.8W$ to cool down 2 converters, efficiency would still reach up to 98.1% efficiency at $P_{in} = 1300W$.

V. Conclusion

The current paper presents design and prototyping of low voltage high current $20kW$ converters with high efficiency and compactness. The high potential of GaN multilevel converters is shown especially when efficiency and volume are key performances. Routing strategies to prevent parasitic switching oscillations are compared by finite element simulations as well as measurement. Thermal cooling has also been studied and tested. Sarcon Thermal paste allowed for improved thermal conduction compared to standard liquid pastes currently used in the industry, but is more expensive and requires proper care to be used efficiently. An experimental setup was built and the first efficiency measurements are very promising. A 20kW converter based on 10 paralleled copies of the studied prototype would occupy a volume of 1.6L, excluding fan volume, but with a $15L$ maximum specified volume, it leaves enough space for fans, casing, auxiliary supplies, etc.

Future work includes thorough efficiency measurement campaign on the Fuel Cell voltage-power range, operation of current-regulated phases in parallel to reach the 20kW target, studying coupled inductors to increase compactness and lower the total mass, developing control for output voltage regulation and phase shedding.

Acknowledgment

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