Thermo-Mechanical and Metallurgical Preliminary Analysis of SiC MOSFET Gate-Damage Mode under Short-Circuit based on a Complete Transient Multiphysics 2D FEM [Best Paper Award]

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1st Prize Winner - Best Paper Awards ESREF'23

Thermo-Mechanical and Metallurgical Preliminary Analysis of SiC MOSFET Gate-Damage Mode under Short-Circuit based on a Complete Transient Multiphysics 2D FEM

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Abstract - For the first time, a complete 2D transient multiphysics electro-thermo-mechanical and metallurgical model of a 1.2kV-80mΩ gate-planar SiC MOSFET power chip has been developed in a single FEM software. This model is used to quantify the short-circuit critical time and energy density with respect to the local SiO_2 interlayer strength at high temperatures and the Al source-metal solidus-liquidus phase transition temperature. Repetitive experimental short-circuits were conducted to confirm the gate-aging existence in coherence with the critical values extracted from the proposed model.

1. Introduction

Understanding the limited use of SiC power MOSFET in extremely abnormal operations such as short-circuit (SC) is necessary for certifying critical applications such as aeronautics. The experimental approach is the main way; however, it is surely expensive to conduct with partial results because it does not allow direct physical links between external macro stresses applied (typically SC fault time, injected energy, drain-source voltage bias) and the chip-level internal stresses (gate oxide mechanical strain-stress, electrode melting temperature, thermal runaway, and latch-up through the p-well parasite bipolar transistor) which lead to damage initiation or failure. For the first time, a complete and alternative approach is proposed in this article by developing and using a complete 2D transient strong coupling multiphysics model fully embedded in Comsol™ software. Previously, in [1], J. Liu *et al.*, using Atlas™ - Comsol™, introduced a weak-coupling model between an imposed transient 2D thermal map and the gate region strain-stress distribution. However, the electro-thermal SiC MOSFET cell-part model is not detailed, and the transient temperature map is unclearly defined around the channel and the source region below the source-metal. Furthermore, Al's latent heat and the temperature dependency on its coefficient of thermal expansion and Young modulus are not included. In [2, 3], K. Yaho *et al.* presented a more detailed 2D and 3D semiconductor planar and trench gate-part model using Sentaurus™, but the thermal-stress process through Sentaurus Interconnect™ exhibits the same limitation as in [1]. In [4], T. Shoji *et al.* considered the latent heat at Al's melting temperature with more accurate mechanical laws using Abaqus™ software. However, the authors used a large-scale chip geometry, including a 2D uniformly imposed Joule heating. Additionally, the transient electro-thermal model part is not considered, and the 2D transient power density is not accurately calculated. In this paper, a new complete multiphysics modeling methodology will be depicted and applied as follows: in sections 2.1 and 2.2, the static and transient wide-range SiC MOSFET cell-level electro-thermal model is depicted, and the two-step fitting procedure is presented focusing on the SC operation. In section 3, the latent heat at the melting temperature of the Al source-electrode is introduced and analyzed; in section 4.1, a preliminary thermo-mechanical analysis of the gate region based on all previous sections' model parts is presented, and the critical pulse time and energy absorption associated with the Al melting temperature and the fracture initiation of the oxide are quantified; in section 4.2 the wide-range temperature dependency of CTE, strain-stress gate-region layers' materials are also investigated; it will result in an interesting physical causality analysis of the possible gate damage scenario in SC operation, including experimental results. Finally, in section 5, a conclusion is suggested.

2. Electro-thermal 2D FEM of a basic SiC MOSFET half-cell

2.1. Step one: static electrical modeling

Thanks to the 2D symmetrical device (Fig. 1a), geometry layers and doping levels of a generation 2 gate-planar 1.2kV-80mΩ-10.8mm² 4H-SiC N-MOSFET half-cell were physically and fully

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parametrized through Comsol Semiconductor Toolbox™ and using previous works from G. Romano *et al.* [5]. The body and source terminals were physically separated but connected at the same ideal electrical node. The considered cross-sectional view is fully parametrized, as described in Table 1. In Fig. 1a), the 4H-SiC part is divided into an intrinsic zone called thick bulk, of thickness t_{drain}, and a zone of heavily doped epitaxy, of thickness t_{drift}, enabling the depletion and spreading of the electric field at the drain-source voltage bias. The upper 4H-SiC chip is covered with a 50 nm deposited SiO_2 gate-oxide layer and the poly-Si gate finger. A SiO_2 protective layer called ILD (Internal Layer Dielectric) covers this gate itself. A thin Titanium layer (Ti) protects the ILD. ILD offers insulation and mechanical protection between the gate contact and the source contact made of aluminum (Al). Electrical isolation boundary conditions were set on the vertical boundaries, and the electrical potentials were imposed on the drain, source, and gate electrodes. Thermal insulation conditions were fixed at all the borders, with a temperature of 300K imposed at the drain electrode to represent the cooling state. At this step (only for semiconductor calculus in the SiC), the thin oxide-poly-gate region was simplified via an equivalent analytic electrostatic model offered by Comsol™. The Gaussian-type doping (or deep junction) profiles were compared and verified with a basic vertical SiC MOSFET available in Sentaurus™ library [6]. Particular attention was paid to the mesh pitch in the channel region, especially near the SiC channel-oxide interface, to well take into account current density gradients. Indeed, 80% of the channel current flows in a less than 2nm thickness. Bulk/channel regions electron/hole mobility thermal dependency laws were defined by D. Kim *et al.* [7], which are based on the well-known Arora's doping dependency based-model. Finally, positive-like fixed oxide-charge density and negative-like trapping profile interface-charge density were firstly defined from [5] and afterward slightly adjusted in combination with channel doping and mobility to pre-fit the average V_{GSTH} value over $25°C < T_j < 175°C$ in the device datasheet [6]. Fig. 1b) gives out $I_{DS}(V_{GS})$ and $I_{DS}(V_{DS})$ static behaviors at this first step. In this section, authors have not tried to fit the static thermal dependency characteristics precisely, as can be seen in Fig. 1b), in order to focus more on the transient channel-current global fitting using the channel's mobility parameter as depicted in §2.2, which will be the basis of the metallurgical and thermal-stress modeling.

TABLE I: GEOMETRIC PARAMETERS [5, 6]

t_{drift}	14µm	t_{ox}	50nm	t_{poly}	185nm
t_{ild}	416n	t_{ti}	45nm	t_{al}	4µm
w_{drift}	8.7µm	w_{ox}	2µm	w_{poly}	1.77µm
w_{ild}	2.33µ	w_{al}	8.7µm		

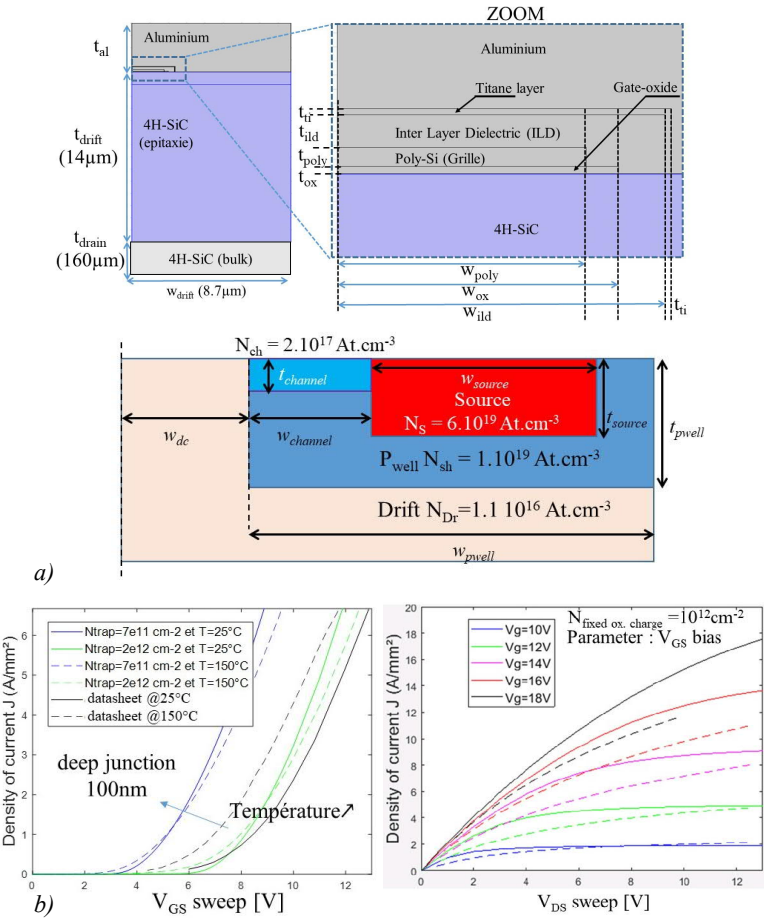

Fig. 1 a) Parametric basis of 1.2kV-80mΩ half-cell gate-planar 4H-SiC MOSFET 2D model and b) static results.

Simulation results seem physically logical but have not sought static mode with higher accuracy because this model will have to be re-adjusted in §2.2 using the channel's mobility parameter at a high transient temperature which is the target of the complete metallurgical and the gate-region thermal-stress study.

2.2. Step two: transient modeling under SC

4H-SiC intrinsic carrier density $n_i(T)$, heat capacity, and thermal conductivity temperature dependency laws were defined in accordance with [7]. Indeed, it is not easy to extend them over a very high-temperature range as in SC operations. This also applies to mobility and charge-trapping/de-trapping laws used

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in §2.1. To address this problem, authors have compensated for all these complex variations with an additional mobility adjustment law thermal dependency $\mu_{adj}(Tj)$ as introduced in (2) from the reference basic Arora's law (1) [5]. In Fig. 2, such a coefficient is efficiently used to completely fit the $I_{DS}(t)$ channel saturation wave on the experimental response from previous authors' work ([8], in Fig. 4a). Note that such a model today does not include Shockley-Read-Hall generation-type leakage current at high temperature and V_{DS} bias. Then, the drain-source leakage current is not modeled in this paper, but this point does not penalize our study, which focuses on the thermal stress around the gate region.

$$\frac{1}{\mu_{channel}} = \frac{1}{\mu_{Arora}(T, N_D, N_A)} + \frac{1}{\mu_{adj}} \quad (1)$$

$$\mu_{adj} = \mu_{0,pl}\left(\frac{T}{T_{ref}}\right)^{\alpha_{PLM}} \quad (2)$$

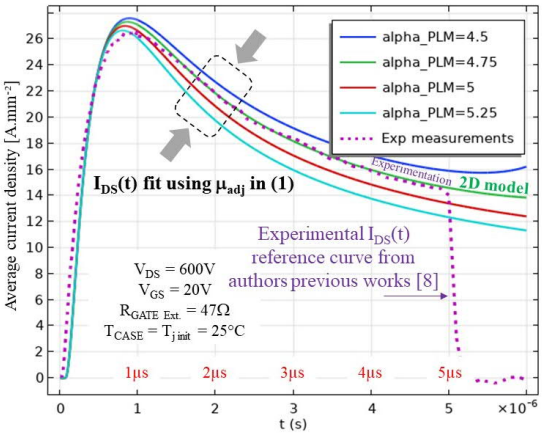

Fig. 2 SC transient $I_{DS}(t)$ (normalized on the active area 6mm²) fitted using an additional μ_{adj} coefficient (1, 2) in Arora's basic mobility law [5] for V_{DS} = 600V, V_{GS} = 20V and $T_{CASE} = T_{jinit}$ = 25°C for different values of α_{PLM} with $\mu_{0,PL}$ = 4000 cm².V⁻².s⁻¹.

3. Transient thermal response and analysis of the Al gate-source electrode, including the solid-liquid phase transition

Due to the relatively low melting temperature of Al (933K) compared to SiC channel temperatures involved in SC (>1200K), a source-electrode melting model is required. In addition, due to the relatively high metal thickness, this one will act as a high-energy heat sink and thus slow down the temperature rise time around the gate region and its strain-stress behavior. The proposed melting model relies on introducing the metal's specific latent heat (L_f = 397 kg/K) over a solidus to liquidus temperature range ($933K \pm \Delta\theta_f$) through an analytic Gaussian transition law as recently implemented for the first time in 2D by authors in [9]. The phase change transition interval is set to be 30 K, as shown in Fig. 3. Such a solidus to liquidus phase change modeling will be applied to the previous 2D transient electro-thermal modeling described in §2.2. Solidus to liquidus thermal conductivity and heat capacitance non-linear laws of Al are also introduced, as well as Ti, SiO_2, poly-Si, and SiC materials based on the parameters in Table II.

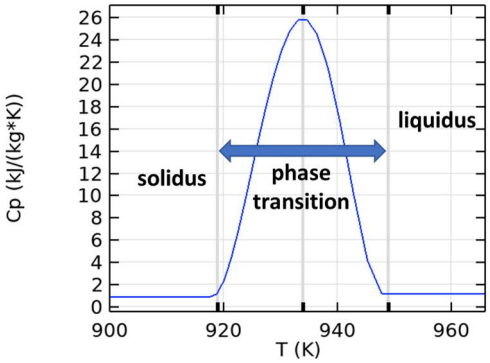

Fig. 3 Al's heat capacity vs. temperature curve.

Table II: A SUMMARY OF THE MATERIAL PROPERTIES FOR §3

Property	Al (solid)	Al (liquid)	Ti	SiO_2	Poly-Si	4H-SiC
ρ (Kg/m³)	2700	2370	4506	2200	2320	2329
$k_{thermal}$ (W/m.K)	237	100	21.9	1.4	34	131
C_p (J/Kg.K)	900	1175	522	730	678	700

Fig. 4a) shows an example of 2D transient thermal maps. The hot spot quickly starts in the JFET inter-cell region, then diffuses to the gate region and afterward to the source region at the channel-source side. The thermal analysis within the channel is graphically difficult to image because of the very strong gradient inside and very small dimensions. In Fig. 4b), as soon as the SiC - Al source interface reaches the solidus–liquidus transition band at t = 2.2µs, a spectacular dynamic "wave-like melting-front spreading" across all the source electrode thickness is visible. The melting front then straightens towards the axis of the gate, which is also a hot region, to finally reach the top of the source electrode at t = 4.2µs. An inset photo also shows a practical top view that proves the metal swelling resulting from a full source melting in the same operating condition.

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Finally, in Fig. 4c), the correlation between this transient thermal analysis and the semiconductor electrical model from §2.2 and the authors' experimentation [8] allows extracting the critical energy density at t = 2.2µs, which is equal to 230mJ/6mm^{-2} = 3.83J.cm^{-2}, leading to a junction temperature T_j = 1420K @2.2µs. Beyond this critical time and energy density absorption, the metal will undergo local melting cycles with each SC stress, severely degrading the electrode-source with a possible diffusion through the ILD-SiO_2 cracks formation or even vaporizing, over-compressing the oxide-poly-gate, as will it be examined in the following §4.

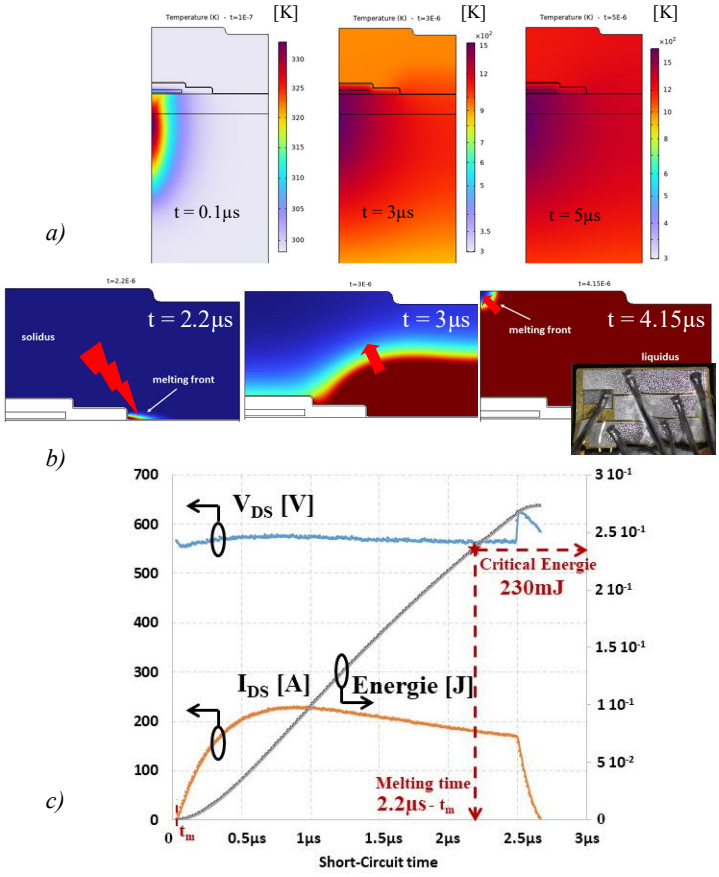

Fig. 4 V_{DS} = 600V, V_{GS} = 20V, T_{CASE} = 25°C a) 2D thermal transient simulation including solidus- liquidus melting model ($\Delta\theta_f$ = 30K, $L_{f\,Al}$ = 397kJ.kg^{-1}) of the Al layer (thickness = 4µm), b) dynamic melting front across the Al layer, c) melting time and energy absorption extracted from electrical modeling and authors experimentation [8].

4. Preliminary thermo-mechanical response and analysis of the Al-Ti-ILD/SiO_2 gate region stress under SC operation

This last part aims to take advantage of the previous full modeling to preliminary analyze the thermo-mechanical behavior and properties of the gate region in short circuit operation in correlation with previous experimental results obtained on the same DUT by the authors. Specifically, the critical time and the critical energy of the ILD-Ti layer's mechanical strength will be extracted in addition to the melting time - energy in §3. All these data seem salient to highlight aging boundaries and to impose a maximum protection time for the gate-driver enabling repetitive short avoiding SiC MOSFET degradations over a wide cycle number.

4.1. Using constant thermal and mechanical properties of gate-region materials (first global simplified modeling)

As a first simple approach, all SiC MOSFET thermal and mechanical parameters have constant values, as described in Table II and Table III. Regarding all these limitations, very promising results were obtained using a dedicated re-meshing of the gate region with a re-interpolation of the transient thermal map between the electro-thermal mesh used in §3 and the new thermo-mechanical mesh used in this section in weak-coupling mode simulation. As electrical and mechanical gradients are very different in intensity and distribution, distinctive mesh sizes are preferable to be implemented. In particular, the JFET and channel regions impose sub-nanometric electric mesh sizes to accurately describe the current density in the channel, whereas a nanometric mechanical mesh size is necessary to consider the stress gradient in the thin Ti layer. The main results are depicted in Fig.5 a) for the same three times used for the thermal maps in §3. It is consistent to note that the maximum mechanical stress regions are localized near the hottest SiC-Ti-Al source electrode zone (see pt "A" and "2" in Fig. 5a)) and around geometric singularities of the ILD-Ti zone (see pts "A", "B", "2" and "4" in Fig. 5a)). Specifically in pt "B", the strong differential CTE at the Al – Ti interface leads to strong mechanical stress in the thin protective Ti barrier layers imposed by the thick Al bulk source electrode and caused by the strong Ti Young modulus value. Such a property is also found partially just below pt "B" at the Ti-ILD/SiO_2 interface but with a slightly lower mechanical stress because ILD/SIO_2 material exhibits a lower Young modulus than Ti and under a lower

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thermal gradient. For critical points “A” and “B” (and partially pt “5”), the simulated mechanical stress exceeds the SiO_2 ultimate strength stress level (1.4GPa [1]), leading to a possible crack initiation and a propagation fracture from the Al bulk – thin Ti barrier to the poly-Si gate finger. In particular, at pt “B”, it is remarkable to visually notice a real “colored maximum stress crest-path” that is completely consistent with ILD-SiO_2 corner cracks observed by authors using FIB-SEM techniques in collaboration with THALES SIX France and CNES laboratories (see inset photo in Fig. 5a)).

Table III: MECHANICAL PROPERTIES OF MATERIALS AT 300 K [1]

Materials	Strength (GPa)	CTE (10^{-6}/K)	Young modulus (GPa)	Poisson ratio
Al	-	23	70	0.33
Ti	-	8.6	115.7	0.321
SiO_2	1.4	0.5	70	0.17
Poly-Si	2	2.6	160	0.22
4H-SiC	21	4.3	500	0.157

In Fig. 5b), the main attention is dedicated to the chronograms of the temporal transient mechanical stresses of the five points of interest. This graph is interesting because it highlights the previously suggested events chronologically. It can be seen that the ultimate strength stress level of 1.4GPa for SiO_2 at point “4” is achieved at 1.9µs before the start of the Al melting at point “2” at 2.2µs. Note that these two critical times represent only 24% and 28% of the device’s failure-mode pulse time (T_{scw} = 8µs [10]). Clearly and physically, the hypothesis that softened or molten Al can penetrate the cracked ILD seems not to be ruled out.

Note that the dynamic melting front modeling seen in §3 is essential to consider because its “heat sink” effect induces a smoother stress rise within the ILD-SiO_2 region. Finally, in Fig. 5c), to confirm the existence of a mechanical rupture threshold of the ILD-SiO_2, authors conducted experimental repetitive SCs on a dedicated test bench [8] considering a short-pulse SC 2.5µs (left side) around the critical time and a long-pulse SC 5µs (right side) greater far than the critical time. In short pulse, the device withstands a set of 1000 SC without showing any apparent gate-source leakage current or drain-source channel transient conduction degradation. In contrast, in long-pulse, the device clearly exhibits a permanent gate-source leakage current from the two-hundredth cycle and drain-source channel transient conduction degradation.

Then these FEM and experimental results could prove that the SC protection delay of the gate driver must operate in a timeless or equal to the critical time to ensure repetitive SC capability to at least 1k cycles.

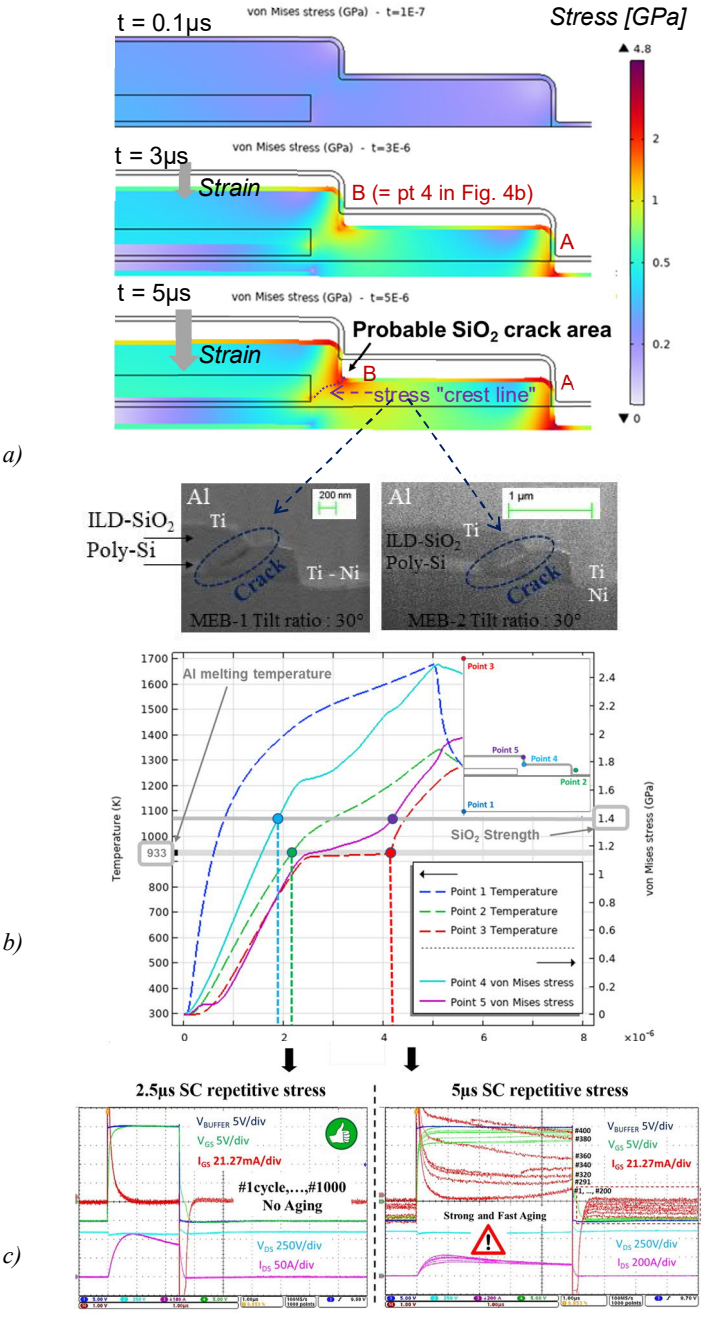

Fig. 5 a) Transient thermo-mechanical strain - stress simulation in SC operation V_{DS} = 600V, V_{GS} = 20V, T_{CASE} = 25°C based on §2.2 semiconductor modeling and including Al phase transition from §3, b) transient thermal and stress trajectories in pts 1, 2, 3 and 4 of the gate, c) correlation with repetitive SC and electrical gate damage–short path from authors’ test bench experiment.

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4.2. Improved modeling: using temperature dependency of thermal and mechanical properties of the gate-region materials

The temperature change can highly influence the properties of SiC substrate and gate-region materials. Because the temperature range in SiC MOSFETs in short-operation is very wide (300 -1500 K), materials would behave differently. The CTE and the Young modulus laws of the Al source electrode bulk are among the most important properties that could change. Therefore, it would be essential to investigate the deformation behavior in the Al-Ti-ILD/SiO_2 interfaces, especially at the zone where cracks are formed and the Al phase transition occurs. As a result, the wide temperature range may influence the mechanical strength critical time and the associated critical energy. Using [11, 12], Al CTE is changing from 23ppm/K at 300K in the solid state to 110ppm/K in the liquid state. Its Young Modulus E(T) is also changing from 70GPa at 300K in the solid state to null in the liquid state! To model such sudden change, authors suggested using the same approach as for the Al Cp(T) phase change modeling in §3 (Fig. 3 from [9]) by physically integrating the $C_p(T)$ Gaussian law over the solidus to liquidus temperature range using the smoothed error-type special function erf(x) in equations (3) and (4) and drawn in Fig. 6.

$$\alpha(T) = \frac{1}{2}\left(1 + \mathrm{erf}\left(\frac{T - T_f}{\sigma\sqrt{2}}\right)\right) \quad (3)$$

$$\mathrm{erf}(x) = \frac{2}{\sqrt{\pi}}\int_0^x e^{-t^2}\,dt \quad (4)$$

Where: T is the temperature in K, T_f is the mean (melting temperature of Al = 933K), σ is the standard deviation or variance representing the duration of the phase transition (fixed to be σ = 5K), and t is the time in second. This smoothed evolution through the σ parameter is also necessary to soften the convergence in the calculus. The material properties of Al at the entire ranges of temperatures were consequently defined as a function of α(T) as shown in equation (3), where the term "Prop" is either thermal expansion coefficient (CTE_{Al}), Young modulus (E_{Al}), or poisson ratio (ν_{Al}). It should be noted that for E_{Al} and ν_{Al}, these parameters were assumed to have very low values for the liquid phase of Al because both parameters do not exist in liquids.

$$\mathrm{Prop}(T) = \mathrm{Prop}_{\mathrm{solid}}(T) * \big(1 - \alpha(T)\big) + \mathrm{Prop}_{\mathrm{liquid}}(T) * \alpha(T) \quad (5)$$

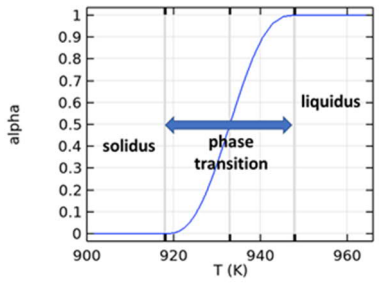

Fig. 6: Al's transition factor α(T) vs. temperature.

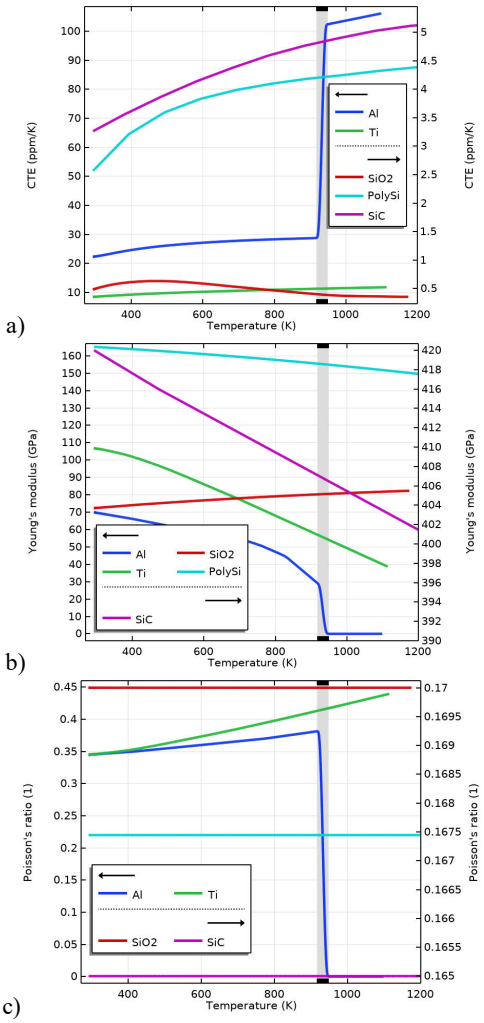

Fig. 7 a) The evolution of CTE with temperature for Al [11], [13], SiO_2 [14], Ti [15], SiC [16], and poly-Si [17], b) The evolution of Young modulus with temperature for Al [12], SiO_2 [18], Ti [19], SiC [20], and poly-Si [21], c) The evolution of poisson ratio with temperature for Al [22], SiO_2 [18], Ti [23], SiC [20] and poly-Si [24].

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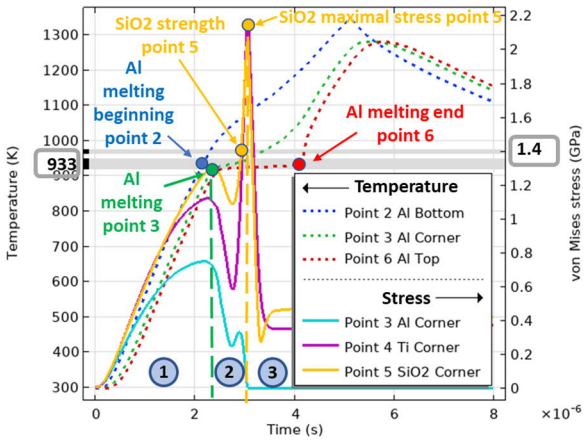
Fig. 7 shows the CTE, E, and ν laws of Al, SiO_2, Ti, poly-Si, and SiC materials as a function of temperature. The grey zone in these figures represents the zone of melting of Al. Regarding the thermal and physical properties of all these materials, their evolution is also considered based on the literature [25]–[29].

In this simulation, symmetry boundary conditions were fixed on the vertical borders, and zero displacements were imposed on the upper and lower borders pending a full simulation of the upper assembly, including the thin Si_3N_4 barrier layer and the thick epoxy case. Fig. 8.a) shows the new temperature and mechanical stress chronograms at the various points of interest. Note that in order to study all thermomechanical quantities in more detail, new points of interest were defined as illustrated in Fig. 8.b). When comparing Fig. 8.a) with Fig. 5.b), it can be seen that the temperature chronograms have not changed. The start and end times for Al's electrode melting are the same. On the other hand, the stress chronograms have changed significantly compared to the results shown in Fig. 5b) in §4.1 due to the temperature dependence of the mechanical parameters over a very wide range, and in particular, the drop in Young's modulus of Al from 750K onwards, followed by its collapse at 933K and the sharp increase in its CTE (x5 from 300K to 933K), as shown in Figs. 7a) and 7b). Various new phases of thermomechanical behavior can thus be identified. During the first phase (small circle marked "1"), corresponding to the overall temperature rise of the structure, the resulting decrease in Young's modulus of Al (Fig. 7b) simultaneously attenuates the dynamic increase in stresses at points 3-4-5 on the Ti barrier and ILD/Si02. The second phase (small circle, marked "2"), corresponding to the onset of local Al melting at point 3, further accelerates the decrease in Young's modulus of Al until its collapse and leads to a sharp drop in all resulting stresses at points 3-4-5 on the Ti barrier and ILD/SiO_2. However, this drop in Young's modulus of Al is simultaneous with the sharp increase in its CTE, as illustrated in Fig. 7a) (blue curve). Although during the phase transition, Al expands much more, generating a further rise in stresses at the end of phase 2. These are exacerbated by the high Young's modulus of the Ti barrier compared to Al (x1.8) and the strong CTE differential existing at 933K between Ti (11.4ppm/K) and ILD/SiO_2 (2.2ppm/K). Finally, the third phase (small circle, marked "3") corresponds to a progressive stress stabilization stage (transient mechanical relaxation) until the Al completely melts.

Fig. 9 clearly illustrates the correlation between Al's metallurgical phase change and the resulting strong local variation in stress. Indeed, it can be seen that the dynamic stress evolution in Al follows its phase change, which explains the strong variation in stresses over time, just before, during, and just after the metallurgical phase transition around 933±15K.

a)



b)

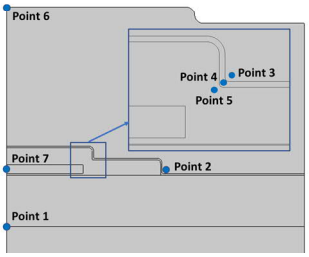


Fig. 8 a) New transient thermo-mechanical strain-stress simulation considering temperature dependency for parameters b) New points of interest.

It is important to note that the temperature dependence of the mechanical parameters implemented into our model is fundamental, as it has a retarding effect on the increase in stress at points 3, 4, and 5. The consequence is that the maximum stress limit set at 1.4GPa for the gate oxide occurs now slightly after the start of Al melting, leading to an increase in the critical mechanical time (SiO_2 strength) from 1.9µs (Fig. 5a)) without considering the effect of temperature on the material properties to 2.9µs when taking high temperature into account (Fig. 8a)), i.e., an increase of 52%. This result also leads to a better correlation between the Fig. 5c) experiment and the multiphysics model proposed in Fig. 8a). This new result is also a step in the right direction in terms of the mechanical robustness of the structure since the close control has more time to secure the component when a short-circuit is detected, and thus avoid mechanical degradation of the ILD/SiO_2.

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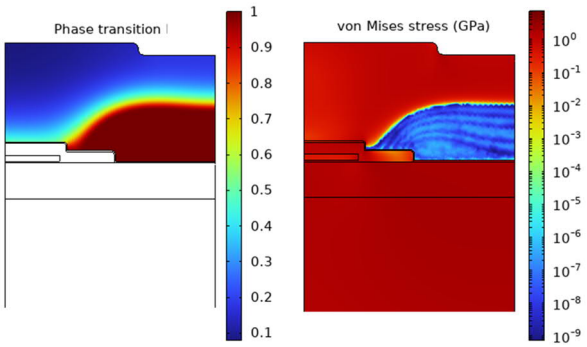

Fig. 9. Al Stress and phase transition fronts at the same time.

5. Conclusion

A complete 2D transient multiphysics electro-thermo-mechanical and metallurgical model of a 1.2kV-80mΩ SiC MOSFET power chip has been developed and validated. Critical time range 1.9µs - 2.9µs (which represents only 24% and 36% of the device's T_{scw} failure-mode pulse time) and critical energy absorption density 3.83J.cm^{-2} were extracted by this model relying on the ILD-SiO_2 rupture strength and the Al-source melting. Moreover, for the first time, the temperature dependence of all physical parameters over a very wide temperature range (300-1500K) was included. The model also incorporates the solid-liquid phase change of the Al source electrode, which occurs at around 933K. This complete and global modeling approach looks fundamental for designers, enabling them to extract numerically the critical thermal and mechanical damage times of components to optimize gate-driver protection and to redesign the device to be more robust. Thermal and mechanical stress chronological evolution in gate-region subjected to a short-circuit was investigated. Temperature rise and stress fields enabled us to localize and date important events in terms of the start of melting of the Al source electrode and the attainment of ultimate strength for ILD/SiO_2 failure. This model offers significant added values compared with previous approaches presented in the literature. However, given the high-stress levels calculated, it needs further to be completed by considering the plasticity phenomena of Al bulk and Ti barrier materials composing the gate region. Plasticity will undoubtedly limit the stress field by saturation, thus further delaying the fracture date of the ILD/SiO_2 region. However, plasticity is likely to introduce an aging effect, which is noticeable in practice when components are cycled.

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