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# Evidence of Trapping and Electrothermal Effects in Vertical Junctionless Nanowire Transistors

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## Abstract

*Understanding trap dynamics and formation of localized temperature hot-spots due to self-heating is crucial for the design optimization of emerging vertical junctionless nanowire transistors (VNWFET). This work investigates the operation of an 18nm VNWFET technology for the first time leveraging pulsed current-voltage measurements. Results indicate increased trap activity as well as electrothermal effects with increasing pulse width. Multiphysics simulations are then used to provide a deeper insight into the nanoscale transport of the VNWFETs.*

**Key words** - vertical junctionless nanowire transistors, electrothermal effects, trapping, multiphysics simulations.

## 1 Introduction

Faced with the limitations of continuous scaling for the classical planar MOSFETs, novel emerging and in particular 3D technologies, such as vertical junctionless nanowire transistors (VNWFET), are being explored as beyond-CMOS alternatives [1]. One of the key advantages of VNWFETs is their inherent 3D structures which can be stacked to increase the number of integrated transistors per unit area for designing more compact, faster and power-efficient hardware targeting neuromorphic computing [2]. In addition, junctionless transistors have a better electrostatic integrity and immunity to short channel effects (SCE) along with a simpler fabrication process [3]. Due to low thermal stability and reduced carrier mobility, electrothermal optimizations are a key design aspect for the VNWFET technology. With the formation of temperature hot-spots within the small device dimensions along with an ultra-thin gate oxide, investigation of self-heating and charge trapping effects in VNWFETs has thus become an important prerequisite. In order to investigate these transport mechanisms, in this work, we perform pulsed I-V measurements with varying pulse widths on a p-type VNWFET (Fig. 1). The pulsed measurement results are then compared with multiphysics simulation of the VNWFETs to understand the behavior of different associated physical parameters. In the following sections, we will discuss the experimental details, the simulation framework followed by a comprehensive analysis of electrothermal and trapping effects.

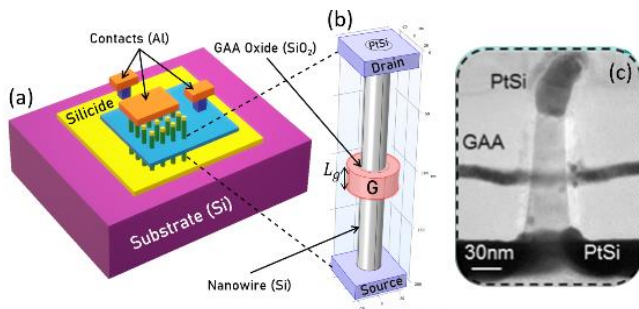


Fig. 1. Schematic representation of (a) Vertical array of GAA nanowires, (b) a single nanowire, (c) SEM image of a fabricated nanowire [4].

## 2 Pulsed I-V measurements

The principle of pulsed I-V measurements relies on applying very short gate pulses on the device so as not to allow sufficient time for its internal temperature to change significantly or activate any charge trapping. For our measurements, a pulse width varying between 1 $\mu$ s and 10ms was used with a duty cycle of 10%. A staircase stepping voltage was applied at the drain to minimize the charging effect [5]. The  $I_D$ - $V_D$  measurement data for all available geometries (nanowire diameters of 22 and 34 nm with 16 and 25 NWs in parallel) over the entire bias range showed a constant increase in the drain current with pulse width, a trend which is diametrically opposite to that of a classical MOS transistor. For further analyses, the VNWFET with 25 NWs having a diameter of 22 nm is selected as a representative device with the highest reproducibility and measurement stability. Fig. 2 shows its pulsed  $I_D$ - $V_D$  under a  $V_{GS}$  of -2.2V, for different pulse widths depicting this trend. It has been hypothesized that this phenomenon is a combined effect of both charge trapping and self-heating.

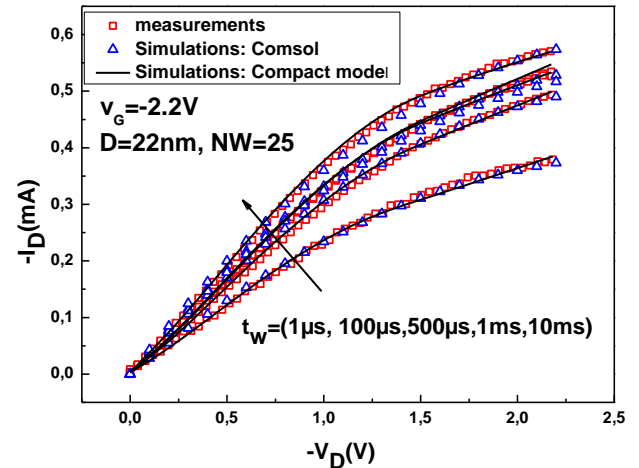


Fig. 2. Pulsed  $I_D$ - $V_D$  measurements compared with simulations.

## 3 Results and discussion

To understand this behavior, we performed finite element method (FEM) based COMSOL Multiphysics simulation of the VNWFETs under the same pulsed conditions as the measurements. The simulation method relies on the partial differential equation (PDE) package in COMSOL for transport equations coupling phonon and electron transport by solving the non-Fourier heat equation and a drift-diffusion model with interface trapping effects [6]. In addition, simulations with the VNWFET compact model [7] have also been performed and the two simulations are compared with the experimental results in Fig. 2 demonstrating good agreement.

## a. Trapping effects

Variation of the threshold voltage ( $V_{TH}$ ) is principally attributed to the temperature induced increase of drain current in junctionless transistors [8]. Charge trapping is known to occur at the Si-SiO<sub>2</sub> interface and within the oxide layer that can also cause a shift in  $V_{TH}$  [9]. However, due to drain induced barrier lowering, an increase in  $V_D$  also causes a variation in  $V_{TH}$ . To avoid this effect, we compared the  $V_{TH}$  for all devices under test at  $V_D = -1V$ , extracted using the transconductance method, in Fig. 3 that shows a continuous increase with the pulse width eventually saturating at the value extracted under DC conditions when pulse width is sufficiently large.

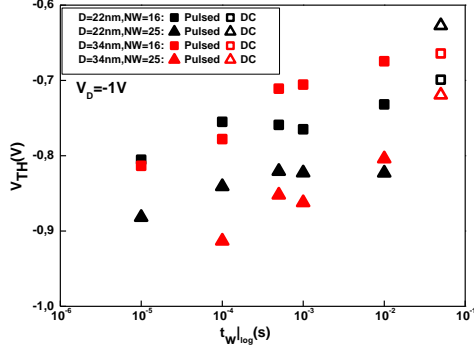


Fig. 3.  $V_{TH}$ - $t_w$  of different VNWFET geometries.

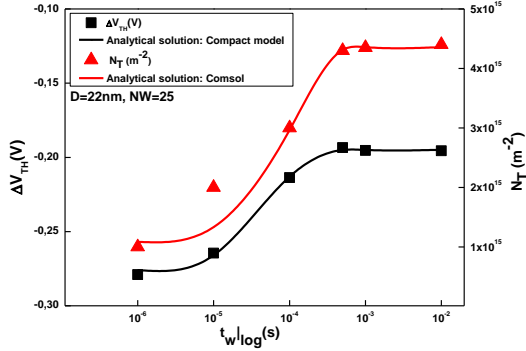


Fig. 4.  $V_{TH}$  and  $N_T$  for different pulse widths compared with analytical solutions.

To analyze the relationship between trap density ( $N_T$ ) and the observed  $V_{TH}$  drift ( $\Delta V_{TH}$ ), generally described by  $\Delta V_{TH} = \alpha q N_T / C_{ox}$ , where  $\alpha$  is a constant,  $q$  is the electronic charge and  $C_{ox}$  is the gate oxide capacitance, pulsed I-V curves are simulated using COMSOL. In addition,  $\Delta V_{TH}$  for each geometry are extracted from the measured I-V and implemented in the analytical equation of  $\Delta V_{TH}$  within the compact model. Both simulations take the  $\Delta V_{TH}$  drift into account and thereby show good agreement with measurements results in Fig. 2. Fig. 4, plots the trap density  $N_T$  extracted from COMSOL and  $\Delta V_{TH}$  from the compact model for different pulse widths. It can be seen that the extracted parameters can be described by an analytical equation of the form  $N_T = N_{SS}(1 - \exp(-t_w/\tau))$ ; here  $N_{SS}$  is the maximum number of available traps,  $t_w$  is the pulse width,  $\tau$  is a time constant associated with the trap activation. This indicates that the increase in the drain current with pulse width is principally governed by the trap activation that results in an equivalent shift of the device threshold voltage.

## b. Self-heating effects

To investigate the dynamics of electrothermal effects associated with the pulsed I-V, COMSOL simulation was used to extract the thermal conductivity and the rise of internal device temperature between the source and drain for different pulse widths (Fig. 5). It can be observed that the device temperature also increases due to phonon accumulation near the drain region at high bias conditions and larger pulse widths indicating the onset of self-heating. Consequently, temperature hot-spots are formed due to a reduction of thermal conductivity caused by phonon confinement in the 22nm nanowires. Phonon confinement can also lead to carrier trapping at the silicon-oxide interface [1] coupled with the electrothermal phenomena. Moreover, under higher biases, scattering mechanisms increase which have significant impact on trapping density.

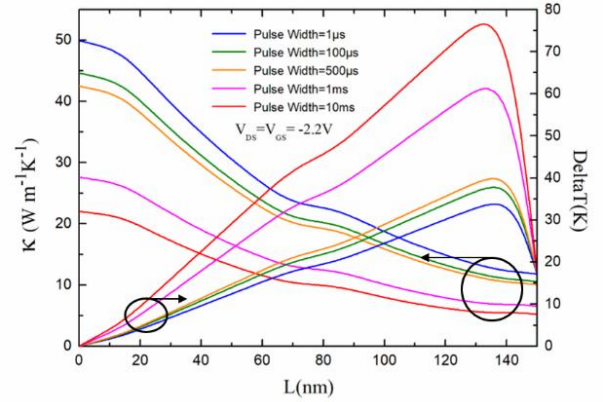


Fig. 5. Thermal conductivity and internal device temperature of the VNWFET.

## 4 Conclusion

In this work, we present, for the first time, a comprehensive analysis of pulsed I-V characteristics of VNWFETs. Experimental results are analyzed with physical simulations indicating the activation of trapping and self-heating with increasing pulse widths. The increase of drain current with larger pulse width has been attributed to an increasing trap density which results in a shift of the threshold voltage. As suggested by the evidences presented in this work, dissociating the trapping and electrothermal phenomena in junctionless transistors remains a challenging task and will be the subject of our future analysis.

### ACKNOWLEDGMENT

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