



HAL
open science

Strategies for Characterization and Parameter Extraction of Vertical Junction-Less Nanowire FETs Dedicated to Design Technology Co-Optimization

Cristell Maneux, Chhandak Mukherjee, Marina Deng, Guilhem Larrieu, Yifang Wang, Bruno Wesling, Housseem Rezgui

► **To cite this version:**

Cristell Maneux, Chhandak Mukherjee, Marina Deng, Guilhem Larrieu, Yifang Wang, et al.. Strategies for Characterization and Parameter Extraction of Vertical Junction-Less Nanowire FETs Dedicated to Design Technology Co-Optimization. ECS Transactions, 2023, 111 (1), pp.209-217. 10.1149/11101.0209ecst . hal-04230924

HAL Id: hal-04230924

<https://hal.science/hal-04230924v1>

Submitted on 6 Oct 2023

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

Strategies for Characterization and Parameter Extraction of Vertical Junction-less Nanowire FETs dedicated to Design Technology Co-Optimization

C. Maneux^a, C. Mukherjee^a, M. Deng^a, G. Larrieu^b, Y. Wang^a, and B. Neckel Wesling^{a, c}

^a Univ. Bordeaux, CNRS, Bordeaux INP, IMS, UMR 5218, F-33400, Talence, France

^b CNRS, LAAS-CNRS, Université de Toulouse, F-31400, Toulouse, France

^c NaMLab gGmbH, Noethnitzer Strasse 64a, 01187 Dresden, Germany

In the era of emerging computing paradigms and artificial neural networks, hardware and functionality requirements are in the surge. In order to meet low power and latency criteria, new architectures for in-memory computing are being explored as alternatives to traditional von Neumann machines, which requires technological breakthrough at the semiconductor device level such as vertical gate-all-around junctionless nanowire field effect transistors (VNWFET), that can address many process challenges such as downscaling, short-channel effects, compactness and electrostatic control. Its integration in the mainstream design flow is not straightforward and requires design technology co-optimization (DTCO) at an early stage. This invited paper explores strategies for accurate characterization and parameter extraction of the VNWFETs to feed the compact models allowing DTCO-efficient strategies.

Characterization Challenges

In the context of emerging technologies for new computing paradigms such as neural networks, vertical nanowire field effect transistors (VNWFET) are a promising technology owing to their naturally 3D architectures [1]. For the circuit design involving such a 3D emerging technology, it is mandatory to build new and accurate compact models to capture the static and dynamic behavior of the device [2]. However, on-wafer test structures of the devices comprise parasitic elements introduced by the RF pads and interconnects that are necessary to probe the devices under test (DUT). An illustration of respective sizes of the DUT and its associated test structure is shown Figure 1. The standard procedure to characterize the parasitic effects of such a device at high frequencies can be divided into two parts. First, the measurement system requires to be calibrated in order to the reference plane is at the probe tips. This can be achieved using standard calibration techniques such as SOLT (Short-Open-Load-Thru). At this point, all the parasitic elements associated with the pads and interconnects are still included in the measurements. In the second step, S-parameters of the open and short test structures are measured and subsequently used to remove the parasitic elements external to the DUT, through a matrix subtraction process known as de-embedding [3].

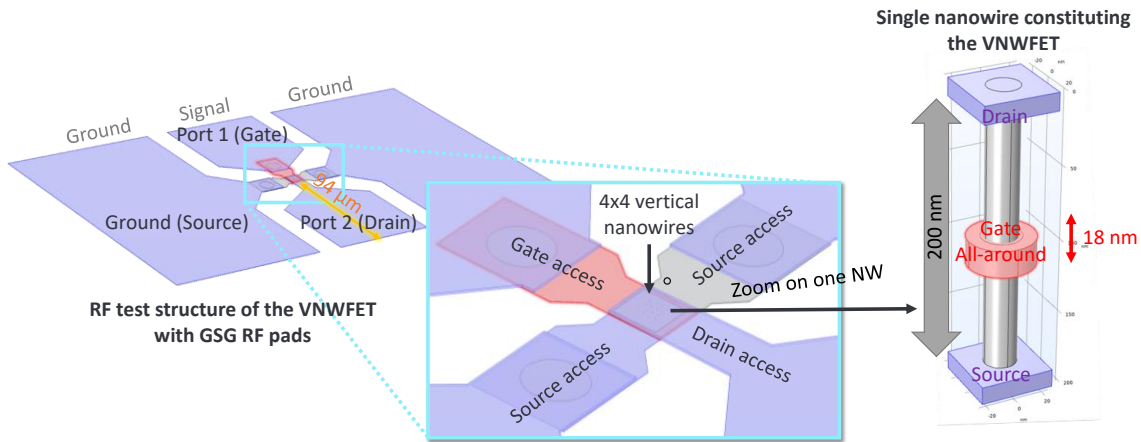


Figure 1. Schematic depicting the size of the test structure featuring GSG pads allowing the use of the RF probe with regards to the size of one single nanowire featuring the channel of the VNWFET.

Although the methodology of parasitic extraction is widely used in technologies targeting high frequency applications, this methodology can also be applied for technologies such as the VNWFET that are mainly designed for logic cells to improve the modeling accuracy, which normally mostly relies on DC measurements [1]. Also, an accurate modeling of the parasitic elements allows the designer to optimize the 3D layout of the logic circuits and interconnects, thereby improving performance metrics such as compactness and energy-delay product of the technology.

Conventional De-embedding Method

Unfortunately, using the conventional de-embedding methodology illustrated in Figure 2 leads to unphysical capacitance values as depicted in the inset of Figure 2 with some negative capacitance values as a function of the frequency. This means that not all parasitic parameters were accounted for, and a more detailed equivalent circuit is mandatory. Therefore, a deeper understanding of the test structure complexity including substrate coupling is requested to efficiently consider the reality of the actual test structure parasitic locations and values.

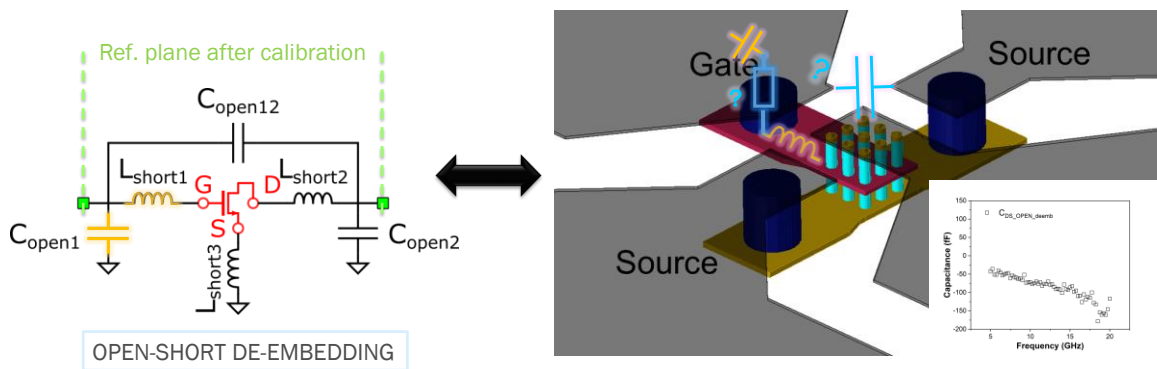


Figure 2. Open-Short de-embedding conventional method featuring compact but simple Small Signal Equivalent Circuit, SSEC. The inset represents the Drain-to-Source capacitance values as a function of the frequency.

Dedicated De-embedding Method for VNWFETs

To construct the SSEC of the OPEN test structure, electromagnetic, EM simulations of different sections of the complete structure were performed, thus allowing to estimate their individual contributions. The pad was considered as an LC network in series with a contact resistance and a π -network was used to model the coupling capacitances between the gate, drain, and the source accesses. The pad capacitance and impedance are estimated from the EM simulations of the virtual OPEN_PAD and SHORT_PAD structures presented in Fig. 3 (a) and (b), respectively. The coupling capacitances are obtained from the OPEN_DUT shown in Fig. 3 (c). A figure of the substrate used in ADS software for the EM simulation is shown on Fig. 3 (d). The extracted elements are then combined to construct the more realistic distributed circuit.

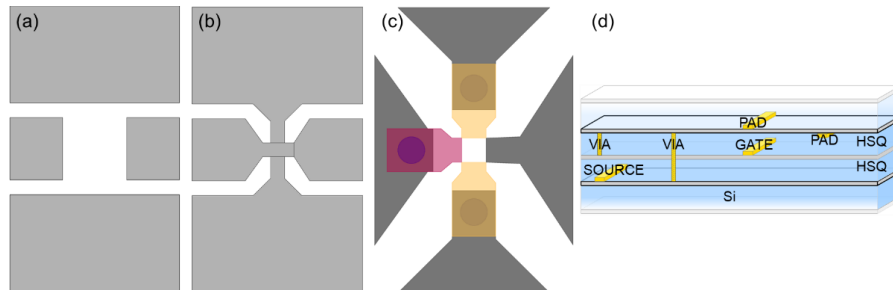


Figure 3: Virtual structures for the EM simulation, a) OPEN_PAD, b) SHORT_PAD, c) OPEN_DUT and (d) the substrate definition on ADS for EM simulation.

Moreover, analyzing the device layout and the fabrication process, one can identify additional substrate parasitic elements related to the low silicon resistivity value [4, 5] and the absence of a ground shield metal underneath the signal pads [6]. The substrate parasitic elements introduce a lossy path, C_{pad2} - R_{sub} - C_{pad3} , shown in Figure 4 along with a fringe capacitance C_{pad1} [7]. The values of all these parasitic elements constituting the SSEC were calculated through analytical equations from the physical dimensions and material properties of the device as well as from EM simulations. The overall SSEC is given Figure 5 along with their respective values. At this stage, the successful de-embedding of the intrinsic S-parameters measurements [8] allows us to continue our investigations towards the next step: The VNWFET compact modeling allowing DTCTO-efficient strategies.

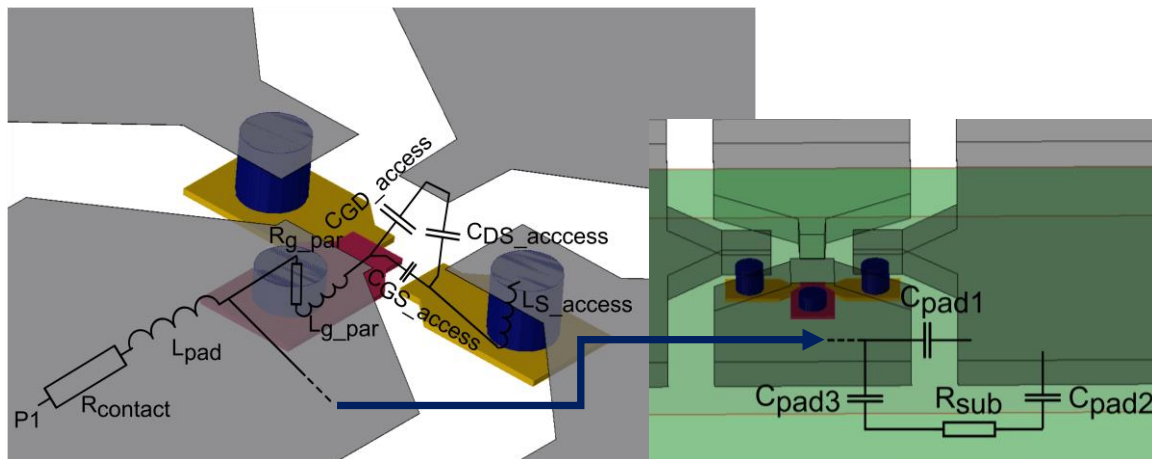


Figure 4: 3D view of the distributed model.

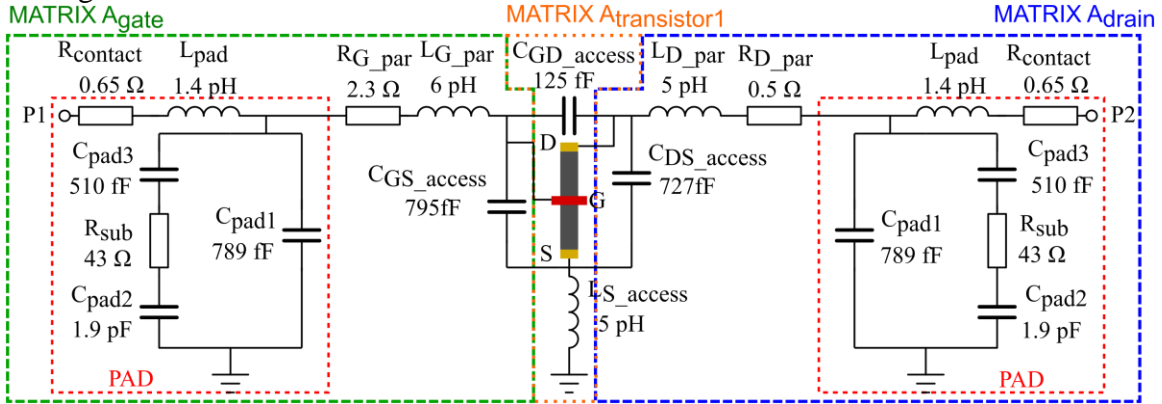


Figure 5: The complete SSEC of the passive elements.

Modelling Challenges

The DTCO is driven by the use of VNWFETs in highly compact 3D logic circuits. Design of these logic circuits relies heavily on compact models, containing a set of physics-based analytical equations for the junctionless transistors. The compact model developed for the 18 nm VNWFET technology [9] has been extensively validated against measurements depicting very good agreement over the entire bias range. To leverage the model for predictive design through DTCO, we further explored the scalability for all available transistor geometries that showed a visible improvement in current scalability for larger devices (Figure 6). However, process variation has limited linear current scaling in smaller nanowire diameters that are of more interest for junctionless transistor operation. In contrast, for a given number of parallel nanowires, maintaining gate electrostatic control over the channel in larger diameters becomes more difficult along with a degradation of the drain current on/off ratio, despite better current scaling (Figure 7). So as a design trade-off for the DTCO, we chose transistors with an optimal diameter (where junctionless functionality and gate electrostatic control are maintained for individual nanowires) with a higher number of nanowires in parallel to boost the drive current.

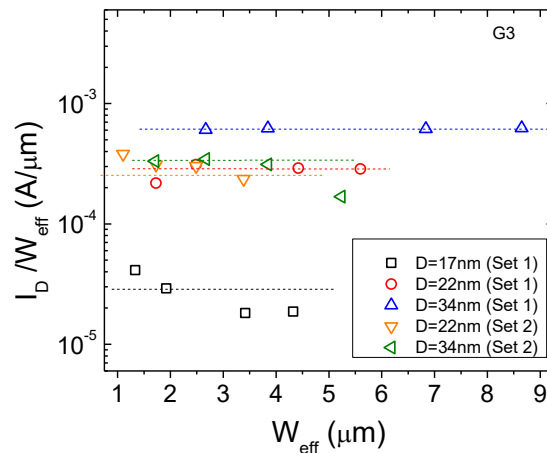


Figure 6: Normalized drain current of the VNWFETs depicting better current scaling in larger geometries.

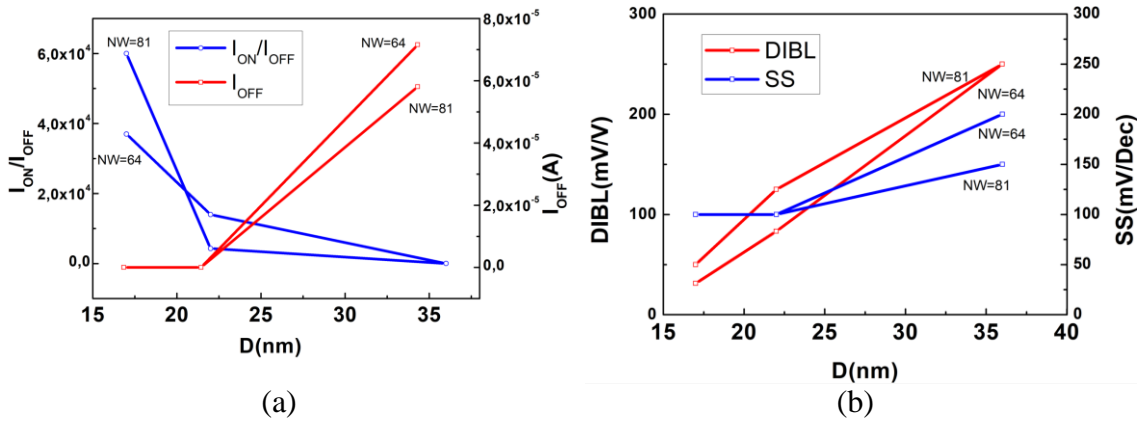


Figure 7: (a) On and off currents and (b) DIBL and subthreshold slope as a function of the nanowire diameters

Reliability assessment through electro-thermal measurements of VNWFETs is crucial when designing 3D logic circuits within DTCO framework, particularly for evaluating long-term performances. Conventional methods for thermal investigation were not applicable for the VNWFETs as the drain current shows steady increase with temperature in contrast with classical devices (Figure 8a) where the current reduces due to temperature induced mobility degradation. Since activation of self-heating could not be confirmed using traditional methods, a new methodology for thermal resistance estimation in VNWFETs is developed. It relies on estimating the temperature coefficient of threshold voltage from I_D - V_G curves at different measurement temperatures (T_A) and power dissipations (P_{diss}) corresponding to same V_G and I_D . From the definition of device/junction temperature, $T_j = T_A + R_{TH} * P_{diss}$, one can extract the thermal resistances (R_{TH}) from the relation $R_{TH} = \frac{1}{I_D} \frac{\Delta V_T}{\Delta V_D} / \frac{\Delta V_T}{\Delta T}$. Theoretical calculations corroborated extracted results with R_{TH} values ranging between 4 and 28×10^4 K/W (Figure 8b). Other non-conventional methods were also explored such as low-frequency S-parameter measurements or R_{TH} extraction using the slope of drain current versus temperature plot at different dissipated powers, all of which offered similar results. A final verification using full device thermal simulation in COMSOL multiphysics, accounting for both ballistic and diffusive heat flux, showed good agreement with experimental results. This is the first demonstration of thermal resistance extraction in highly-scaled VNWFETs identifying the location of the two thermal contributions: NW channels and PtSi contacts (Figure 8c).

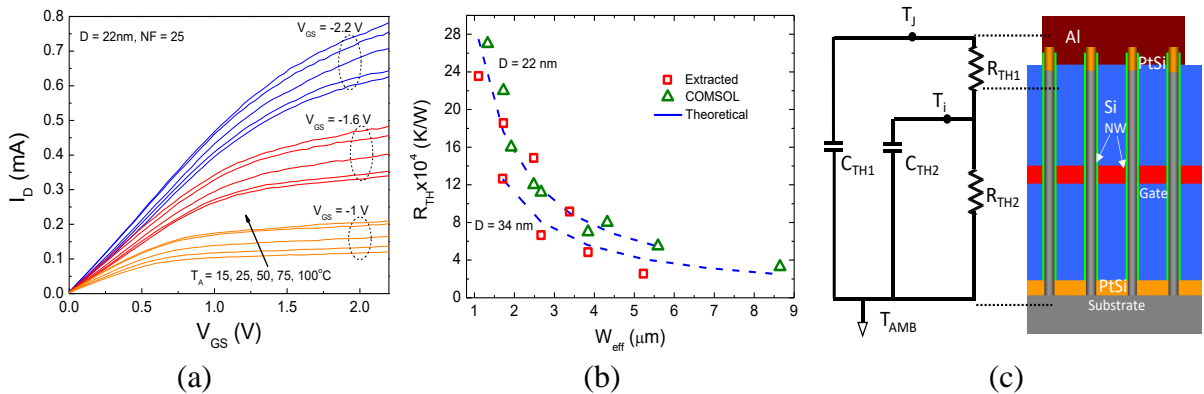


Figure 8: Junctionless transistor Thermal properties: (a) Temperature dependence of the drain current of the VNWFETs, (b) Thermal resistance as function of device width (c) Location of the thermal contributions: NW and PtSi.

Conclusion

Vertical nanowire field effect transistors (VNWFET) represents a promising dedicated emerging technology for dense neural networks. For this proof of concept meet the 3D circuit cell design requirements DTCO approach relies on the compact modeling.

In this invited paper, we have demonstrated that Two major steps have been taken towards the reality of compact VNWFET modelling.

A clear and secure de-embedding methodology involving an EM simulation step has allow to sort the intrinsic VNWFET dynamic characteristics out of its test structure measurements.

Also, this is the first demonstration of thermal resistance extraction in highly-scaled VNWFETs leading to identify the location of the two thermal contributions: NW and PtSi. In the future scope of this work, the elements of the thermal network will be integrated in the JLNT compact model for design-technology co-optimization (DTCO) [1] and will play an important part in redefining the semiconductor value chain spanning across device and system levels involving these emerging 3D vertical technologies.

Acknowledgments

This work was supported by the project FVLLMONTI funded by the European Union's Horizon 2020 research and innovation program under grant agreement N°101016776, by LEGO project (Grant

ANR-18-CE24-0005-01) and by the LAAS-CNRS micro and nanotechnologies platform, a member of the Renatech French national network.

References

1. C. Maneux et al., (Invited). 67th Annual IEEE IEDM, San Francisco, Dec. 11-15, 2021.
2. C. Mukherjee et al., Solid-State Electronics, vol. 183, p. 108125, Sep. 2021, doi: 10.1016/j.sse.2021.108125.
3. M. C. A. M. Koolen et al., in Proceedings of the 1991 Bipolar Circuits and Technology Meeting, Minneapolis, MN, USA, 1991, pp. 188–191. doi: 10.1109/BIPOL.1991.160985.
4. G. Larrieu et al., Solid-State Electronics, vol. 130, pp. 9–14, Apr. 2017, doi: 10.1016/j.sse.2016.12.008.
5. M.-J. Lee et al., IEEE Electron Device Lett., vol. 29, no. 10, pp. 1115–1117, Oct. 2008, doi: 10.1109/LED.2008.2000717.
6. Sangwook Han et al., in 2006 IEEE International Conference on Microelectronic Test Structures, Austin, TX, USA, 2006, pp. 76–81. doi: 10.1109/ICMTS.2006.1614279.
7. A. Aktas et al, IEEE Circuits Devices Mag., vol. 17, no. 3, pp. 8–11, May 2001, doi: 10.1109/101.933786.
8. B. Neckel Wesling et al., Solid-State Electronics, vol. 194, p. 108359, Aug. 2022, doi:10.1016/j.sse.2022.108359.
9. C. Mukherjee et al., Solid-State Electronics, Elsevier, 2021, 183, pp.108125. ;10.1016/j.sse.2021.108125