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Improving off-state capacitance of SOI-CMOS RF switches: how good are air microcavities?

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Abstract— This paper investigates the reduction of the off-state capacitance (C_{OFF}) of SOI-CMOS RF switches induced by the introduction of air microcavity in the back-end interconnection network. A detailed methodology combining electromagnetic and semiconductor transport simulations is used to separately evaluate the respective contributions of the interconnects and junction capacitances. A baseline switch and an optimized version of the same are studied to evaluate their ability to take advantage of air microcavities. Simulations show a reduction of 73 fF/mm regardless of the switch structure considered, resulting in a 24.6% and 30.6% improvement in C_{OFF} for baseline and optimized switches, respectively, bringing the optimized version to a 60fs record $R_{ON} \times C_{OFF}$. This concept was experimentally implemented using a partial etch process that resulted in a reduction of 21.7 fF/mm, i.e., 7.2%. Finally, the implementation of a more isotropic and selective etching process using HF in vapor phase is shown to approach the optimal configuration of air microcavities.

Keywords— RF switch, Air microcavities, CMOS, SOI, Off-state capacitance, Vapor phase selective etching

I. INTRODUCTION

THE constant demand for evolution in communications forces standards to push their limits in terms of data rate, latency or security. As such, the latest 5G standard is based on key technologies such as spectrum sharing, massive MIMO or carrier aggregation for optimized usage of available bandwidth. We also note the deployment of a millimeter wave frequency bands (mmW) referred to as FR2 band covering the 24.25-52.6 GHz range to expand into high data rate marked at fixed locations [1][2]. As a consequence of the growing complexity of communication systems, an increase of switches becomes necessary to selectively propagate high frequency signals through the transmit/receive pathways. This constraint of complexity must of course be handled without impacting the systems in terms of insertion loss, linearity, power handling and isolation [3]. In order to limit the accumulation of losses along the propagation path, RF switches must offer low insertion losses reflected by a small on-state resistance with a sufficient isolation in the off-state. The two important parameters, R_{ON} and C_{OFF} , precisely reflect the performance of a switch in terms of insertion loss and isolation, respectively. Minimizing them also means reducing their product ($R_{ON} \times C_{OFF}$), the main figure of merit (FoM) used to compare switches with various layouts implemented in different semiconductor technologies. Strategies for optimizing switch performance are manifold, such as reducing the SOI film thickness to reduce C_{OFF} and

downscaling the gate length to lower R_{ON} . Several reports have shown that these optimization levers can be implemented without compromising linearity and power handling [4][5][6][7]. Nevertheless, these papers do not sidestep the point that the optimization of both insertion losses and isolation is a matter of compromise since any path leading to the reduction of R_{ON} inevitably degrades C_{OFF} and the RF breakdown voltage as well. Improving these two parameters together is all the more difficult given the level of optimization already achieved to date, e.g., by simultaneously reconsidering the junction design, introducing offset spacers, boosting the stress level in the Contact-Etch-Stop-Layer (CESL), reducing the gate length and thickness as well as optimizing the circuit layout and the routing strategy of metal interconnect tracks [8]. In that context, the use of air microcavities within the metal interconnect network, also known as back-end-of-the-line (BEOL), appears as a legitimate option to investigate in an attempt to lower C_{OFF} independently of R_{ON} . The contribution of BEOL to the overall C_{OFF} is significant and typically ranges from 30 to 40%. [4][9]. The replacement of the intermetal dielectric with air theoretically enables the reduction of the material permittivity from $\epsilon_r \sim 4$ to $\epsilon_r = 1$, thus holding the promise of a substantial reduction of C_{OFF} . In the present study, the impact of air microcavities in the BEOL is analyzed on two generations of switches, the first one serving as a baseline [4] and the second one being a significant evolution integrating many optimization factors [8]. Through this comparison, the specific question that is addressed here is whether the same C_{OFF} reduction margin can be achieved on a baseline structure and on an optimized structure. In this perspective, this paper first presents a simulation strategy to finely evaluate the impact of air microcavities in BEOL of RF switches. It follows by detailing a selective etching method to create microcavities in a post-process sequence. Subsequently, the efficiency of the proposed approach is experimentally validated by extracting C_{OFF} from S-parameter measurements on switches incorporating microcavities. Finally, perspectives for improvement of the etching process using a selective vapor phase are discussed in order to perfect the etching of the intermetallic dielectric down to the CESL, i.e., at the bottom of the metal 1 (M1) interconnect layer.

II. RF SWITCH LAYOUT AND BEOL ROUTING

As outlined previously, the baseline switch, referred to as [A] is based on a previous 130nm technology [4]. The improved switch structure, referred to as [B], is an upgrade of structure [A] in many points [8]. Here we focus on one of the

fundamental differences between structures [A] and [B], namely the organization of its layout and routing strategy of source/drain terminals and body contact. The respective layouts are available in Fig. 1. The structure [A] is composed of 25 MOS transistors in parallel, each with a gate width of $10\ \mu\text{m}$, i.e., a cumulative width of $250\ \mu\text{m}$. Several variations of this structure exist in terms of polysilicon gate pitch ($0.86\ \mu\text{m}$ $0.92\ \mu\text{m}$) and gate length ($0.14, 0.16, 0.18$ and $0.22\ \mu\text{m}$). In the following of the study, we will restrict considerations on structure [A] with a grid length of $0.14\ \mu\text{m}$ and a poly pitch of $0.92\ \mu\text{m}$. The structure [B] is different in its layout and routing of the M1 layer. First, it consists of 50 transistors in parallel with a gate width of $5\ \mu\text{m}$ giving a cumulative width identical to structure [A]. The structure [B] also features variations on the polysilicon gate pitch and length. To obtain comparable and consistent results, a geometrical configuration similar to structure [A] is selected. Another main difference between the structures is the access to the active zone. On the one hand, structure [A], which has 4 metal layers, uses M1 and M2 levels to contact the source/drain terminals and for the body bias, resulting in a rather congested central region. Structure [B] has only 3 metal levels and uses only M1 over the active zone to reduce as much as possible parasitic capacitive coupling. This layout and routing simplification is achieved by using the active silicon layer to distribute the body bias along the chain of 50 transistors in parallel.

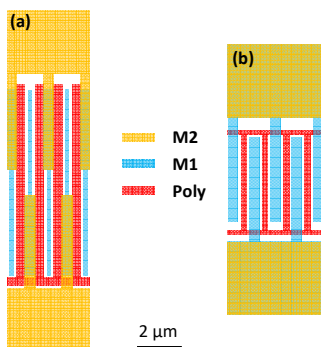


Fig. 1. (a) Partial layout of the RF switch test structure [A] (b) Partial layout of the RF switch test structure [B]

III. SIMULATION STRATEGY AND RESULTS

Since the efficiency of air microcavities is very strongly related to the BEOL density of metal tracks in the central zone of the switch, structure [B] is expected to limit the potential C_{OFF} reduction as we start from an already optimized structure. To verify this assertion, a comprehensive simulation strategy was set up to appreciate with accuracy the impact of air microcavities. RF modeling is partitioned into two parts. The first consists in a 2D simulation of the transistors at the FEOL level using the IMPACT software to solve the small-signal transport equations based on the drift-diffusion (DD) approach. The second simulation task manages the complex interconnects in three dimensions (3D) due to the complexity of BEOL geometry. This is realized by solving Maxwell's equations with the Momentum module of the ADS software. In both simulation methods, C_{OFF} is extracted from the identification of the calculated Y-parameters to a lumped equivalent circuit [10]. The effect of air microcavities is essentially captured by simulations of the BEOL part of the switch. The DD simulation of the transistor is therefore used to calibrate results against measurements as the overall C_{OFF} derives from the sum of the BEOL and FEOL contributions. Under these conditions, the

modelling approach is therefore able to determine the relative contributions of FEOL and BEOL to C_{OFF} before the introduction of air microcavities. For structure [A], we obtain $C_{\text{OFF-FEOL}} = 190.1\ \text{fF/mm}$ (63%) and $C_{\text{OFF-BEOL}} = 111.7\ \text{fF/mm}$ (37%) for a total figure of $301.8\ \text{fF/mm}$. On the other hand, structure [B] features $C_{\text{OFF-FEOL}} = 134.2\ \text{fF/mm}$ (53%) and a $C_{\text{OFF-BEOL}} = 116.5\ \text{fF/mm}$ (47%) which yields a total C_{OFF} of $250.7\ \text{fF/mm}$. It is worth noting that the relative weight of the BEOL in the total capacitance is more important in structure [B] given the optimizations made to the intrinsic transistor. The relative contribution of air microcavities is therefore expected to be more consequent when compared to structure [A]. The electromagnetic simulation of the interconnect network (BEOL) is built from the circuit layout and the description of the metal/dielectric multilayer stack, each layer being described by its material and the relevant electrical parameters. The simulation methodology consists in replacing the inter-metal dielectric by air above a uniform etching front penetrating the interconnection network stack. The attenuation of the parasitic capacitive coupling induced by the BEOL can thus be appreciated as a function of the etching depth. The results of this simulation study are available in Fig. 2, from which two main conclusions can be drawn. First, it is clearly established that the attenuation of C_{OFF} is extremely sensitive as the etching front falls below the M2 level and reaches its maximum when the dielectric removal is complete down to the bottom of M1. This defines the optimum target area to reach by etching. The second point relates to the C_{OFF} reduction margin obtained for each structure. C_{OFF} of structure [A] is reduced from $301.8\ \text{fF/mm}$ to $227.4\ \text{fF/mm}$ representing a reduction of 24.6%. For the structure [B], a reduction of 30.5% is obtained from $250.7\ \text{fF/mm}$ to $174.1\ \text{fF/mm}$.

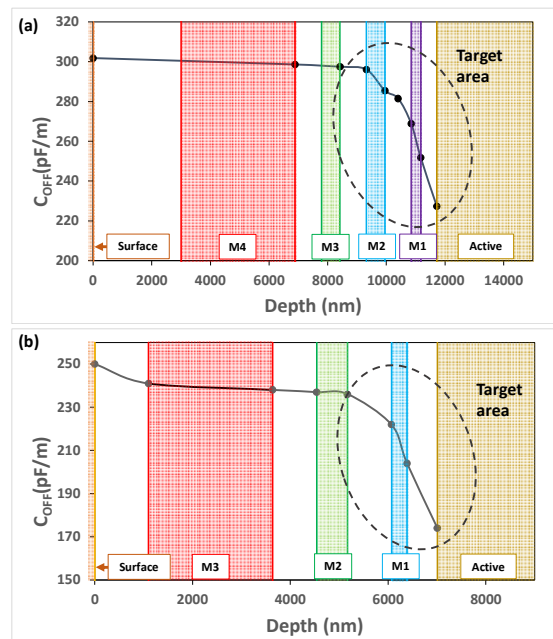


Fig. 2. (a) Simulated C_{OFF} as a function of the air microcavity etching depth for (a) structure [A] and for (b) structure [B]

These results show that air microcavities lead to a larger relative reduction of C_{OFF} on structure [B] despite an absolute improvement of about $73\ \text{fF/mm}$ for the two styles of switch structures. In both cases, the simulations confirm the interest and efficiency of air microcavities for C_{OFF} reduction, even in the case of structure [B] whose layout had been optimized in

order to lighten the M2 metal density. Fig. 3 represents the classical $R_{ON} \times C_{OFF}$ figure of merit of the simulated structures [A] and [B] along with some other measured results taken from the literature. The 4 clouds of points with labels [A], [A₂], [A₃], and [A₄] correspond to measurements performed on the baseline switch structure. The measured performance achieved by structure [B] is also highlighted [8]. Data points labelled [A'] and [B'] correspond to the simulated ultimate case where the intermetal dielectric is totally removed down to the CESL layer, i.e., 227.4 fF/mm and 174.1 fF/mm for structures [A] and [B], respectively. The interest of air microcavities in the BEOL is well emphasized as structure [B'] establish a new state-of-the-art.

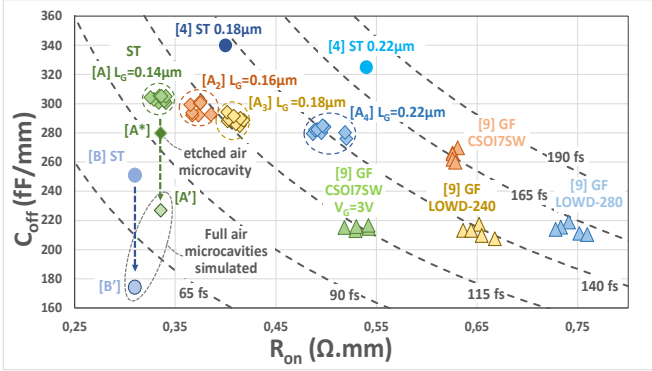


Fig. 3. $R_{ON} \times C_{OFF}$ figure of merit with the simulated impact of the cavities

IV. AIR MICROCAVITY PROCESS

A post-process etching sequence has been set up for implementing the concept of air microcavities theoretically studied so far. The process flow is schematically illustrated in Fig.4 and comprises 3 localized etching steps using a focused ion beam (FIB) and a final finishing step based on reactive ion etching (RIE). Among the FIB steps, the first two create rectangular cavities, $50 \times 30 \mu\text{m}^2$ and $30 \times 10 \mu\text{m}^2$, respectively, as shown in Fig. 5(a). These two cavities enable to go down 9 μm and reach the top of the M2 metal level. The separation in two distinct steps is used to recalibrate the etching depth at each transition between two metal levels, here M4 and M3, successively. The third FIB step creates narrow trenches of $0.6 \times 5 \mu\text{m}^2$ between the fingers of the M2 level as shown in Fig. 5(b) and penetrate to a depth of 1.5 μm down the top of M1 level. This step is the most critical in the process as any misalignment of the trenches can lead to a degradation of the metal interconnections. Finally, the last step, carried out by RIE etching, removes as much oxide as possible from the bottom of the trenches. The RIE chemistry used is composed of CF_4 and Ar in order to achieve etch selectivity with respect to the aluminum layers, the nitride CESL layer and the polysilicon gate fingers in case of CESL over etching. The result after RIE etching is given in Fig. 5 (c) and (d). It is worth noting that the obtained result is still imperfect but is sufficient to evaluate the impact of air microcavities.

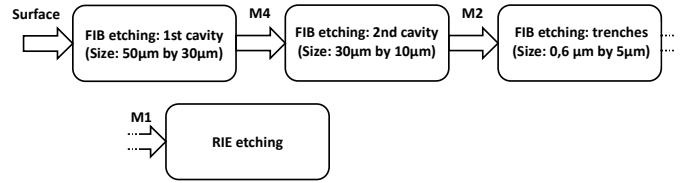


Fig. 4. Air microcavity etching process flow focused on RIE etching

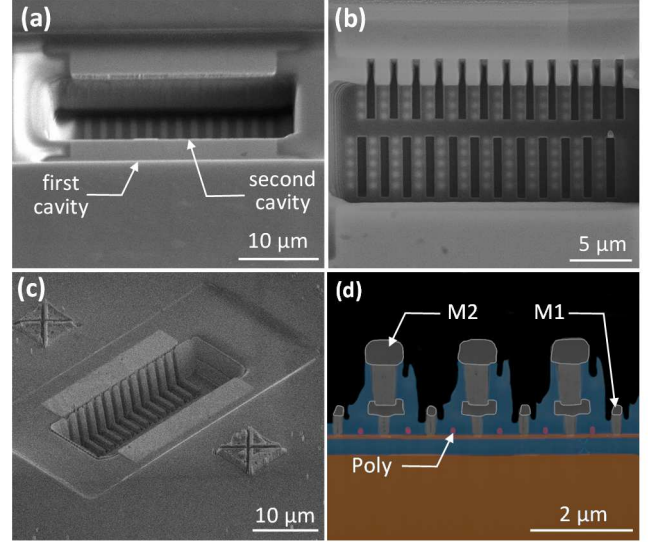


Fig. 5. SEM pictures taken during successive steps of the process: (a) Top view of the first two cavities. (b) Tilted view of the trenches. (c) Tilted view of the final structure. (d) Cut view of the structure after RIE etching

The C_{OFF} small signal characterization of the etched structure gives 279 fF/mm, i.e., an improvement of 22 fF/mm (7.3%) as shown by marker [A*] in Fig.3. This figure does not match the simulated best result that reaches 227.4 fF/mm. To explain this discrepancy, the remaining volume of oxide due to incomplete etching at the M1 level must be carefully taken into account. It is possible to calculate an equivalent permittivity for each dielectric layer constituting the BEOL stack by considering the volume of oxide removed during the etching. The calculation is governed by the following formula:

$$\epsilon_{eq} = \left(\frac{V_{etched}}{V_{layer}} \right) \cdot \epsilon_{air} + \left(1 - \frac{V_{etched}}{V_{layer}} \right) \cdot \epsilon_{oxide}$$

After applying these modifications in the BEOL stack description, Momentum simulation gives a revised C_{OFF} of 274 fF/mm, in excellent agreement with the experimental result. This model can be used regardless of the shape of remaining oxide obtained during the process by introducing effective permittivities.

V. PROCESS OUTLOOK AND CONCLUSION

In order to completely remove the intermetallic oxide from the BEOL, a final vapor phase etching step is desirable to promote the isotropic penetration of the etchant. A second prerequisite is to ensure etch selectivity with respect to the metal interconnects. Hydrofluoric acid (HF) in vapor phase fulfills both of these requirements and has therefore been implemented in a simplified etching scheme given in Fig. 6 [11][12].

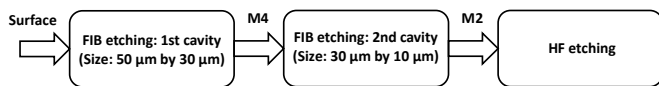


Fig. 6. Air microcavity etching process flow focused on HF etching

Fig.7 proposes pictures taken after vapor phase HF etching oxide into the cavity for 9 min. The implementation of this process highlights the efficiency deep into the cavity and the aggressiveness on top surface of the chip. This process matches expectations by reaching the polysilicon gates and by etching the oxide between the vias and contacts. Compared to the process using RIE etching, the efficiency of this process is closer to the complete oxide removal scenario on which simulations are based.

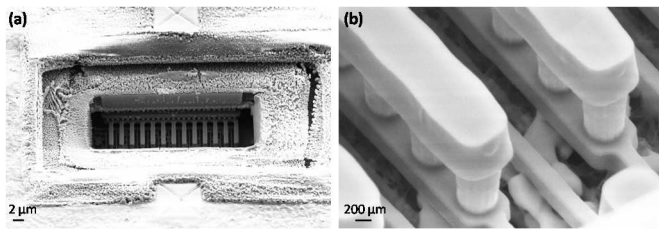


Fig. 7. SEM picture taken after vapor phase HF etching: (a) Tilted view of the complete structure. (b) Tilted view focused at the bottom of the structure

No characterization could be performed on these chips due to the damage of vapor HF on the contact probing pads located at the top surface of the chip. To cope with this problem, the process has been revisited by adding a protective layer so that the surface of the chip is not exposed to vapor HF. A 60 nm thick Al_2O_3 layer meets all requirements and was implemented using atomic layer deposition (ALD) after the second FIB etching step. This additional protective layer requires a new FIB etching step to expose the cavity bottom to vapor HF. The final process given in Fig. 8 has been implemented as illustrated in Fig.9 showing that the Al_2O_3 protective coating preserves the chip integrity.

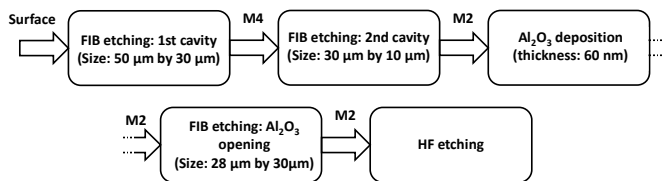


Fig. 8. Air microcavity etching process flow focused on HF etching with Al_2O_3 protection layer

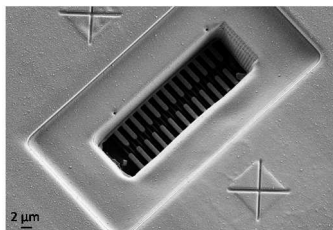


Fig. 9. SEM picture taken after vapor phase HF etching (with Al_2O_3)

The degree of completion of the latest process scheme opens the way to a complete demonstration of the concept of air microcavities in the BEOL. The results obtained have allowed to appreciate how much the efficiency of this concept depends on a total elimination of the dielectric down to the base of the first metal level. Future work will focus on confirming the

principle of air microcavities through a series of characterization on C_{OFF} , R_{ON} and the RF breakdown voltage. Particular attention will also be given to the impact of microcavities on thermal dissipation. Beyond its implementation in a post-process approach, this proof of concept must also be extended for an industrial deployment, which requires replacing the FIB steps, which is achievable through a modification of the BEOL process.

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