



HAL
open science

Application of the Double Source Switching Test to GaN HEMTs

Tamiris Grossl Bade, Maroun Alam, Hervé Morel, Dominique Planson

► **To cite this version:**

Tamiris Grossl Bade, Maroun Alam, Hervé Morel, Dominique Planson. Application of the Double Source Switching Test to GaN HEMTs. 25th Conference on Power Electronics and Applications (and Exhibition), EPE '23 (IEEE) ECCE Europe (Energy Conversion Congress and Expo Europe), Sep 2023, Aalborg, Denmark. 10.23919/EPE23ECCEurope58414.2023.10264519 . hal-04225311

HAL Id: hal-04225311

<https://hal.science/hal-04225311>

Submitted on 2 Oct 2023

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

Application of the Double Source Switching Test to GaN HEMTs

Tamiris Grossl Bade, Maroun Alam, Hervé Morel, Dominique Planson
Univ Lyon, INSA Lyon, Université Claude Bernard Lyon 1, Ecole Centrale de Lyon, CNRS,
Ampère, UMR5005, 69621 Villeurbanne, France
21 Av. Jean Chapelle, 69621
Villeurbanne, France
Tel.: +33 4 72 43 87 24
E-Mail: herve.morel@insa-lyon.fr
URL: <http://www.ampere-lab.fr>

Index Terms—Wide bandgap devices, Gallium Nitride (GaN), Double pulse test, Hard switching, Dynamic Ron.

Abstract—This paper demonstrates the advantages of the switching test circuit “double source test” (DST) on reliability and robustness tests on GaN HEMTs. This circuit performs switching tests with an auxiliary switch to short-circuit the DUT while on stand-by, allowing to control of the duration of the drain-source static stress over the DUT. This feature can contribute to the study of the impact of hard switching events on the current collapse of GaN HEMTs independently of the static drain-source stress, when the tests reported in present literature show these effects superposed. Moreover, the DST when programmed for minimum drain-source stress considerably reduced the current collapse on p-GaN gate devices, allowing longer repetitive tests.

I. INTRODUCTION

Gallium nitride (GaN)-based power transistors are good candidates for the next generation of high-efficiency and high switching frequency converters [1]–[5]. They present a high breakdown voltage, and are based on a 2-dimensional electron gas (2DEG) channel with very low on state resistance [6].

However, even if the on state resistance is low, it is frequently compromised by the current collapse phenomenon [7]. The current collapse occurs when the charge trapping around the 2DEG channel reduces the flow of electrons, increasing the effective on-state resistance.

This phenomenon is particularly troublesome for HEMTs with a p-GaN gate, used in technologies such as gate-injection transistors (GIT) or enhanced-mode HEMT (E-mode HEMT), which are the most commonly found normally-off HEMTs [8]–[10]. For this technology

current collapse takes place due to both hard switching and the drain-source voltage stress on the off state [11].

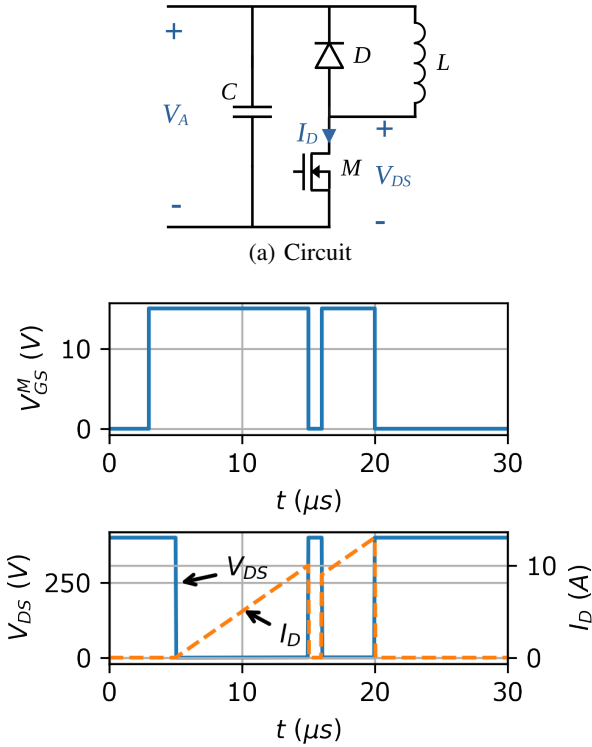
The hybrid-drain gate injection transistor (HD-GIT) technology was designed to mitigate the current collapse [12], what successfully occurs for hard switching conditions but not for soft switching [11], [13].

The classic switching test circuit is the double pulse test (DPT) [14], and it is frequently used on reliability and robustness studies. However, the present literature demonstrated that current collapse is likely to place during repeated switching events with a DPT circuit, strongly reducing the maximal duration of the test [11], [17]. Therefore, in the case of reliability tests involving GaN HEMTs the DPT circuit might not be the best option, and recent studies have proposed better adapted switching tests circuits [15], [16].

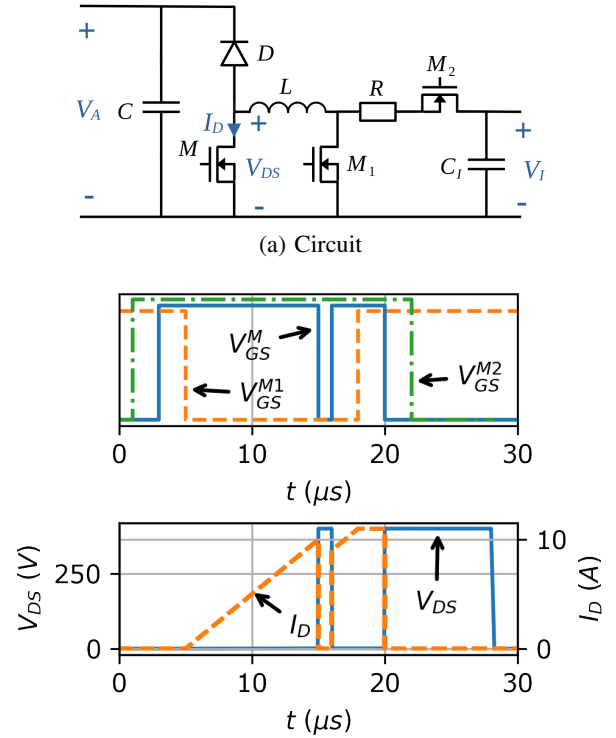
Moreover, the results from Li [11] show that the current collapse after multiple switch pulses is mainly due to the static drain-source stress on a gate injection transistor (GIT), one of the p-GaN gate technologies. The hard switching events increase only marginally the effects on current collapse when compared to soft-switching configurations. From these findings rises the interest in studying in more detail the impact of hard-switching in the current collapse, with minimum drain-source voltage stress during the switching test.

Secondly, in the typical switching DPT the device duty cycle is well below 0.1, what may be considerably different from most real applications [1]. If the duration of drain-source voltage stress previous to each hard switch event can be controlled, the application conditions could be better emulated during characterization tests.

This paper demonstrates that the Double Source Test (DST) provides the necessary control over the off-state stress duration to allow the impact of the hard-switching



(b) Command signal and waveforms
 Fig. 1: Double Pulse Test (DPT)



(b) Command signals and waveforms
 Fig. 2: Double Source Test (DST)

events on the current collapse to be decoupled from the static stress. This circuit was first proposed by Garrab et. al. for the switching characterization of silicon diodes in [18], and is a good alternative for reliability tests on GaN HEMTs.

This article is structured as follows: section II describes the double source test and highlights its main differences with the traditional double pulse test, section III describes the experimental method applied to compare the two testing circuits, and section IV details the results of the switching tests.

II. THE DOUBLE SOURCE TEST (DST)

A simplified schematic of the well-established Double Pulse Test (DPT) is shown in Fig. 1, along with the waveform of the variables of interest. This circuit has the advantage of being simple, but two main disadvantages can be cited: firstly, the current at the turn on depends on V_A , and its discharge during the off state can change drastically with its duration t_{OFF} ; secondly, it imposes a constant drain-source voltage (V_{DS}) stress when the Device Under Test (DUT) is in the off state.

Particularly for p-GaN gate HEMTs, the V_{DS} stress in the off state is one of the main causes of the current collapse phenomenon, along with hard switching. From

this arises the interest of a testing circuit in which the duration of the V_{DS} stress can be easily controlled.

The Double Source Test (DST) satisfies this goal. A simplified schematic of the DST is given in Fig. 2a, and it works as follows: once the control switch M_2 is ON and the protection switch M_1 is OFF, the test can take place; the DUT gating is similar to that of the DPT; the switched current can be better controlled by the additional voltage source V_I and the charging time of the inductance L .

Note that the switch M_1 is turned on to remove the V_{DS} stress off the DUT when the test bench is in stand-by. Another advantage of the DST is that the current drop during the DUT off state can be reduced in comparison with the DPT, as long as $V_A > V_I$.

Thanks to the M_1 switch, the duration of the static stress from the voltage V_{DS} can be reduced to a minimum. It is imposed on the DUT during the off state of the test t_{OFF} and during the period of discharging of the inductance L , which lasts t_{dis} given in (1). A chronograph of the voltage and current on the DUT during the DST is given in Fig. 2b.

$$t_{dis} = L \frac{I_L}{V_A} \quad (1)$$

TABLE I: Comparison between DPT and DST, assuming $V_A > V_I$ and number of switching cycles N

	DPT	DST
I_L charging	I_L depends on V_A Charging inductance L is faster	I_L depends on V_I Smaller current drop ΔI_L between turn off and turn ON
V_{DS} stress	Constant V_{DS} stress on off state Strong current collapse, due mainly to V_{DS}^{OFF} stress [11], [13]...	V_{DS} stress minimized, duration = $N(t_{OFF} + t_{dis})$ Reduced current collapse

The main differences between the two switching test circuits are resumed in table I. Two interesting aspects are considered: the behavior of the current on inductance L , and the voltage stress on the DUT in the off state.

For current I_L , the voltage that induces the charging of inductance L is V_I in the DST circuit, what gives more control on the behavior of the current. The circuit was designed for $V_A > V_I$, so that the current drop in the off state of the DUT is smaller. This allows the reduction of inductance L and gives more liberty in the choice of t_{OFF} .

However, the main interest of applying the DST circuit to GaN HEMTs is the reduction of the off state V_{DS} stress duration, due to the M_1 switch. Note the difference on V_{DS} on Figs. 1b and 2b: in the DPT test it stays high between switching cycles, while in the DST it is put to zero with the aid of the M_1 switch.

To compare the advantages of these two switching circuits, they were performed under similar conditions in a modular test bench, with a inductance L large enough to guarantee that the switching tests are equivalent. Fig. 3 exemplifies this point: the only difference between the two tests is the second point of connection of the inductance L : either the high or low points of the switching cell, both configurations giving the same switching waveform.

III. METHOD

To test if the Double Source Test (DST) has indeed advantages when compared to the Double Pulse Test (DPT), these two switching tests were repeatedly performed on HEMT devices, and the degradation induced by each test was assessed with a series of static I/V measurements used as a characterization set.

The DST and DPT tests were performed in a modular bench test, particularly using the same inductor L , an

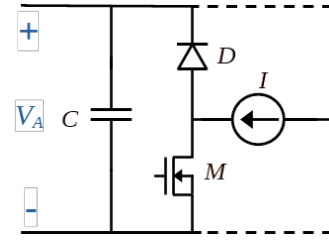


Fig. 3: Equivalency between the DPT and DST testing circuits

air-core solenoid. This inductance was designed to be strong enough to emulate a current source connected to the middle point of the switching test (see Fig. 3).

The number of switching cycles in each test went from $N = 360 \times 10^3$ up to $N = 10 \times 10^6$ switches. Each switching test was performed with a virgin device. Each device was characterized with the static measurements set before being put to test. The characterization test was repeated for every device that survived the switching test precisely 10 minutes after the test was over.

The waiting time between switching pulses was increased and the switched current was reduced to guarantee that the temperature would remain stable and around $25^\circ C$. The waiting time was kept around $10 ms$ to avoid any self-heating.

The switching tests were monitored with scope measurements of the switching V_{GS} , V_{DS} , and I_D . Normally, this monitoring is done with a clamped measurement of V_{DS} , so that the dynamic R_{DS}^{ON} can be measured with sufficient accuracy [19]. However, in this study the focus is on the long term effects of the stress during the switching test, and for that reason the V_{DS} measurement was performed in full scale.

Two p-GaN gate technologies were put to test in this study. The first device is the E-mode HEMT from GaN-Systems GS6530-2L, with a p-GaN gate with Schottky contact. The second device is a GIT with a p-GaN gate made with ohmic contact and a hybrid drain to mitigate current collapse: the HD-GIT Infineon IGT60R070D1. The details of each device are given in table II. The gate voltages to drive each HEMT device followed the indications of their application notes: $V_{GS} = [-6, 3] V$ in both cases.

The characterization set used to access the degradation state due to stress in each component is composed of three measurements: the static ON-state resistance R_{DS}^{ON} , the leakage current I_D^{OFF} under $V_{DS} = 100 V$, and the threshold voltage V_{th} measured with the triple-sense protocol [20], [21]. The measurements were performed with

TABLE II: Technology, manufacturer, designation, and rating values of the devices under test (DUT). R_{DS}^{ON} : typical value of ON state resistance without current collapse, I_{DSS} : typical off state leakage current

Technology	Designation of the DUT	max V_{DS}	R_{DS}^{ON}	V_{th}	I_{DSS}
E-mode HEMT	GaNsystems GS-065-030-2-L	650 V	50 m Ω	1.7 V	2 μ A
HD-GIT	Infineon IGT60R070D1	600 V	70 m Ω	1.2 V	1 μ A

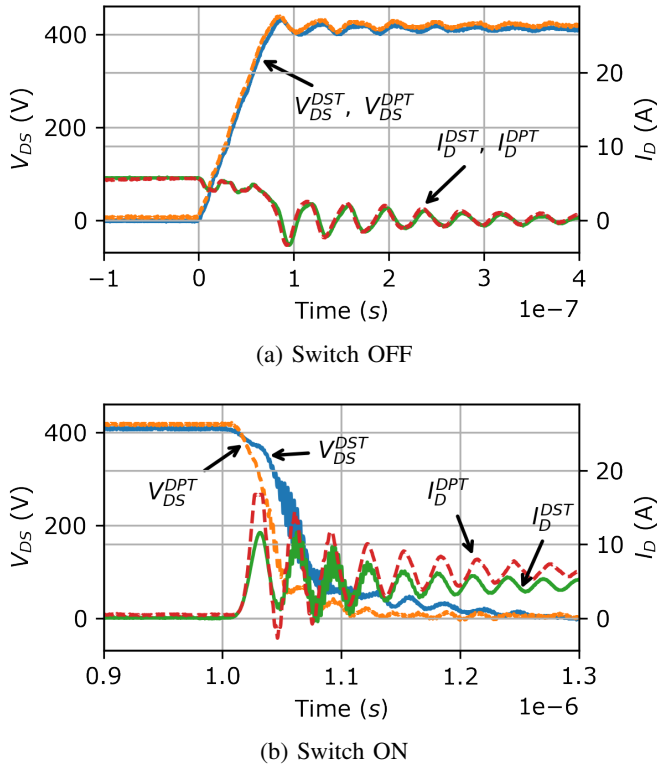


Fig. 4: Comparison of the switching waveform obtained with the DST and DPT tests

the Keysight B1505A Device analyzer, its parameters and details are given in table III.

The two tests were performed in the same modular test bench, with the connection of the inductance changed to switch between the two tests. The test bench was configured so that equivalent switching waveforms could be obtained. They are compared in Fig. 4.

The parameters of the switching waveform are resumed in table IV, where t_r is the rise time, t_f the fall time and "PO" the percentage overshoot of the signal.

The oscillation seen in the turn on switch (Fig. 4b) is originated from the resonance between the wiring in-

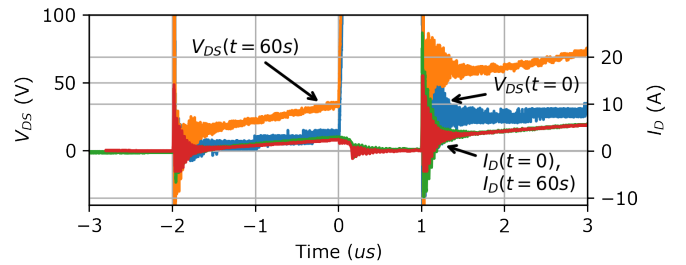


Fig. 5: Current collapse taking place on E-mode HEMT with DPT

ductance and the parasitic capacitance in the test bench. Indeed, for the bench to be modular planar connections ensured with pressuring nylon screws were used, and even if their parasitic capacitance was reduced to a minimum they are still present in the circuit. Also, the turn ON curves do not superpose perfectly because of the the two technologies have different switching dynamics. It is possible longer t_f observed in both Fig. 4b and table IV is due to the recombination phase under the p-GaN layer of the hybrid drain before the actual switch takes place.

IV. RESULTS AND DISCUSSION

The current collapse phenomenon considerably reduces the limits of the DPT switching test. Indeed, the dynamic drain-source resistance R_{DS}^{ON} increases rapidly with time, as can be seen in the measurements from the E-mode device plotted on Fig. 5. In this plot, two sets of measurements of the voltage V_{DS} and the current I_D are superposed. The measurements are taken at the beginning ($t = 0$) and at $t = 60$ s after the start of the switching test.

The increase on the voltage drop on the ON state after the 60 s stress is visible. Note that the increase on V_{DS} is important enough for it to be measured even without a voltage clipping circuit, seen that the measurements in Fig. 5 were performed with a 600 V range.

As a result of the degradation due to current collapse, the E-mode device cannot withstand long DPT tests. The current collapse also takes place in the HD-GIT device, but on a smaller scale.

To increase the duration of the switching test, the switching current of the DPT with the E-mode device was smaller than for the DST test.

The comparison between the DPT and DST effects on the E-mode HEMT is illustrated in Fig. 6a. Note how the current collapse on the DPT is considerably bigger

TABLE III: Characterization set: series of static I/V measurements used to assess the state of the devices

Variable	V_{DS}	I_D		V_{GS}		Comments
		E-mode HEMT	HD-GIT	E-mode HEMT	HD-GIT	
R_{DS}^{ON}	-	5.5 A	8 A	6 V	4 V	HD-GIT: $I_G = 26 mA$
I_D^{OFF}	100 V	-	-	0 V	0 V	
V_{th}	$= V_{GS}$	7.5 mA	2.6 mA	sweep		triple sense [21]: V_{th}^{DOWN} after $V_{GS} < 0$, V_{th}^{UP} after $V_{GS} > 0$

TABLE IV: Parameters of the switching waveform of the two tests

V_{DS}	DST	DPT
t_r	59 ns	57 ns
t_f	94 ns	56 ns
PO	4.5%	4.6%

than on DST, even with the reduced value of I_D on the DPT test.

The endurance of the E-mode devices under both DPT and DST test is illustrated in Fig. 6b. In this figure, the duration of test in number of switches (N) is plotted in function of the switched current, with filled markers indicating a successful test and the 'x' markers indicating a breakdown.

It is clear that the DPT causes a much more serious degradation on the device, seen that the breakdown events were more frequent and occurred for lower currents. It is likely that these breakdown events are due to self-heating induced by the current collapse.

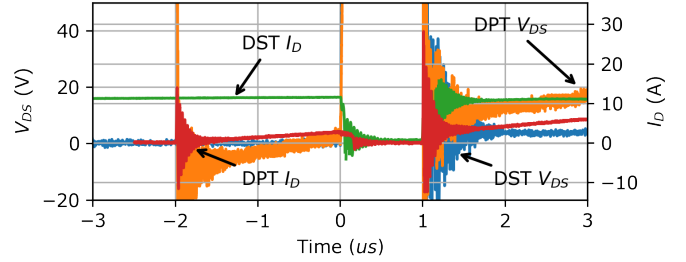
For the HD-GIT the current collapse was also more pronounced during the DPT test than the DST, as shown in Fig. 7. However, the hybrid-drain technology was robust enough for the realization the DPT of long duration and with the same current as in the DST.

For the HD-GIT device, the comparison between the impact of the two tests on the device performance was possible. The two tests DPT and DST were performed with $N = 7 \times 10^6$ switches and with a switched current $I_D = 15 A$.

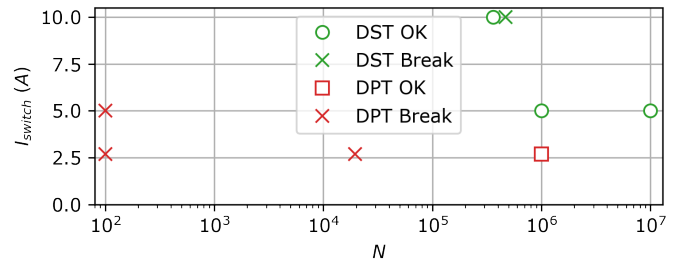
The characterization set described in table III was used before, precisely 10 min after, and 24h after the end of the switching tests. The characterization results are given in table V.

These results show that even if the HD-GIT device can withstand the DPT test with $N = 7 \times 10^6$ switches, its performance was considerably affected by it. Two main changes occurred:

- The threshold voltage was reduced by half;



(a) Current collapse



(b) Breakdown points

Fig. 6: Effects of current collapse on the E-mode HEMT device on each of the two tests DST and DPT; a) Worst-case current collapse, followed by breakdown on DPT, and b) State of the DUT after each test, in function of the switching current and the number of switches: "x" marks a breakdown

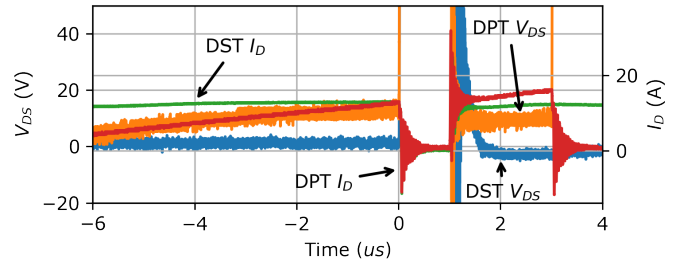


Fig. 7: Effects of current collapse on the HD-GIT device on each of the two tests DST and DPT

TABLE V: Comparison of the state of the devices before and after the two switching tests with $N = 7 \times 10^6$ switching cycles and $I_D = 15 A$.

	DPT			DST	
	before	after 10'	after 24h	before	after 10'
R_{DS}^{ON}	57.37m Ω	57.11m Ω	57.64m Ω	58.42m Ω	58.13m Ω
V_{th}^{UP}	1.28V	623.97mV	1.28V	1.22V	1.23V
V_{th}^{DOWN}	1.27V	614.21mV	1.28V	1.22V	1.22V
I_D^{OFF}	75.62nA	20mA ^C	60.08nA	71.46nA	76.21nA

^C: attained compliance value of the measurement

- The leakage current rose the level of a broken device.

The device recovered, however, after the 24h rest on ambient temperature. But these results seem to indicate that it came close to failure during the DPT.

Note that the same effect did not take place on the DST, a test for which the static characteristics of the device had but a negligible variation. This is in agreement with the results found in the literature [11], [13]: the impact of the V_{DS} stress on the current collapse is much greater than that of the hard switching, even if the number of switching cycles is higher in the present study.

In conclusion, this results show that the DST circuit was able to reduce the effects of the current collapse, in reducing the duration of the V_{DS} stress in the off state applied to the device. Indeed, the E-mode device could withstand repeated DSTs, while the DPT were destructive to it. As for the HD-GIT, the impact of current collapse during the DST test were gone after the 10 minutes pause, while for the DPT a longer rest time was necessary for the device to recover.

This characteristic allows the study of the effects of the hard-switching alone on the current collapse, instead of coupled with the V_{DS} stress. Therefore, the DST circuit can be useful for current research in allowing the two main stressing factors of the GaN HEMTs to be studied separately.

V. CONCLUSION

The current collapse phenomenon is more impacted by the constant V_{DS} off state stress than the hard-switching events during a double pulse test (DPT). The double source test (DST) circuit described in this paper allows switching test to be performed for higher switching currents and for a longer duration on time, by allowing the tests to occur with minimum V_{DS}

stress. It allows the current collapse due to the hard-switching events to be studied and compared without the influence of the V_{DS} static stress. For the E-mode HEMT technology it has been shown that less breakdown events took place, and that the measured current collapse after a few switches is considerably smaller in the DST test. In the HD-GIT device the long exposure to off state V_{DS} stress on the DPT caused a 50 % fluctuation on the V_{th} , while on the DST the long switching test did not cause any long term impact on the device characteristics. This circuit can be used to single out the hard-switching stress on GaN HEMTs, and contribute to the research on the impact of hot-electrons in the channel during hard-switching events.

REFERENCES

- [1] K. J. Chen, O. Haberen, A. Lidow, C. I. Tsai, T. Ueda, Y. Uemoto, and Y. Wu, "GaN-on-Si Power Technology: Devices and Applications," vol. 64, no. 3, pp. 779–795, Mar. 2017.
- [2] X. Hao, J. Zou, K. Yin, X. Ma, and T. Dong, "Enhanced power conversion capability of class-e power amplifiers with GaN HEMT based on cross-quadrant operation," vol. 37, no. 11, pp. 13 966–13 977, 2022.
- [3] J. Lu, K. Bai, A. R. Taylor, G. Liu, A. Brown, P. M. Johnson, and M. McAmmond, "A modular-designed three-phase high-efficiency high-power-density ev battery charger using dual/triple-phase-shift control," vol. 33, no. 9, pp. 8091–8100, 2018.
- [4] Y. Zhang, C. Chen, Y. Xie, T. Liu, Y. Kang, and H. Peng, "A high-efficiency dynamic inverter dead-time adjustment method based on an improved GaN HEMTs switching model," vol. 37, no. 3, pp. 2667–2683, 2022.
- [5] Y.-F. Wu, J. Gritters, L. Shen, R. P. Smith, and B. Swenson, "kv-class GaN-on-Si HEMTs enabling 99vol. 29, no. 6, pp. 2634–2637, 2014.
- [6] M. Meneghini, C. De Santi, I. Abid, M. Buffolo, M. Cioni, R. A. Khadar, L. Nela, N. Zagni, A. Chini, F. Medjdoub, G. Meneghesso, G. Verzellesi, E. Zanoni, and E. Matioli, "GaN-based power devices: Physics, reliability, and perspectives," *J. Applied Physics*, vol. 130, no. 18, p. 181101, Nov. 2021.
- [7] S. Yang, S. Han, K. Sheng, and K. J. Chen, "Dynamic On-Resistance in GaN Power Devices: Mechanisms, Characterizations, and Modeling," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 7, no. 3, pp. 1425–1439, Sep. 2019.
- [8] G. Greco, F. Iucolano, and F. Roccaforte, "Review of technology for normally-off HEMTs with p-GaN gate," *Materials Science in Semiconductor Processing*, vol. 78, pp. 96–106, 2018.

- [9] Y. Uemoto, M. Hikita, H. Ueno, H. Matsuo, H. Ishida, M. Yanagihara, T. Ueda, T. Tanaka, and D. Ueda, "Gate injection transistor (GIT)—A normally-off AlGaIn/GaN power transistor using conductivity modulation," vol. 54, no. 12, pp. 3393–3399, 2007.
- [10] Y. Ohmaki, M. Tanimoto, S. Akamatsu, and T. Mukai, "Enhancement-mode AlGaIn/AlN/GaN high electron mobility transistor with low on-state resistance and high breakdown voltage," *Japanese Journal of Applied Physics*, vol. 45, no. 11L, p. L1168, nov 2006.
- [11] R. Li, X. Wu, S. Yang, and K. Sheng, "Dynamic on-State Resistance Test and Evaluation of GaN Power Devices Under Hard- and Soft-Switching Conditions by Double and Multiple Pulses," *IEEE Transactions on Power Electronics*, vol. 34, no. 2, pp. 1044–1053, Feb. 2019.
- [12] K. Tanaka, T. Morita, H. Umeda, S. Kaneko, M. Kuroda, A. Ikoshi, H. Yamagiwa, H. Okita, M. Hikita, M. Yanagihara, Y. Uemoto, S. Takahashi, H. Ueno, H. Ishida, M. Ishida, and T. Ueda, "Suppression of current collapse by hole injection from drain in a normally-off GaN-based hybrid-drain-embedded gate injection transistor," *Applied Physics Letters*, vol. 107, no. 16, p. 163502, Oct. 2015.
- [13] E. Fabris, M. Meneghini, C. De Santi, M. Borga, Y. Kinoshita, K. Tanaka, H. Ishida, T. Ueda, G. Meneghesso, and E. Zanoni, "Hot-Electron Trapping and Hole-Induced Detrapping in GaN-Based GITs and HD-GITs," *IEEE Transactions on Electron Devices*, vol. 66, no. 1, pp. 337–342, Jan. 2019.
- [14] J. B. Witcher, "Methodology for switching characterization of power devices and modules," Master's thesis, Virginia tech, 2003. [Online]. Available: <https://vtechworks.lib.vt.edu/handle/10919/31205>
- [15] M. F. Tayyab, M. Silvestri, M. Bernardoni, T. Basler, and G. Curatola, "Dynamic high temperature operating life test methodology for long-term switching reliability of GaN power devices," *Microelectronics Reliability*, vol. 138, p. 114613, Nov. 2022.
- [16] A. Barbato, M. Barbato, M. Meneghini, M. Silvestri, T. Detzel, O. Haerberlen, G. Spiazzi, G. Meneghesso, and E. Zanoni, "Fast System to measure the dynamic on-resistance of on-wafer 600 V normally off GaN HEMTs in hard-switching application conditions," *IET Power Electronics*, vol. 13, no. 11, pp. 2390–2397, Aug. 2020.
- [17] A. Ikoshi, M. Toki, H. Yamagiwa, D. Arisawa, M. Hikita, K. Suzuki, M. Yanagihara, Y. Uemoto, K. Tanaka, and T. Ueda, "Lifetime evaluation for hybrid-drain-embedded gate injection transistor (HD-GIT) under practical switching operations," in *2018 IEEE International Reliability Physics Symposium (IRPS)*. Burlingame, CA: IEEE, Mar. 2018, pp. 4E.2–1–4E.2–7.
- [18] H. Garrab, B. Allard, H. Morel, K. Ammous, S. Ghedira, A. Amimi, K. Besbes, and J.-M. Guichon, "On the extraction of PiN diode design parameters for validation of integrated power converter design," *IEEE Transactions on Power Electronics*, vol. 20, no. 3, pp. 660–670, May 2005.
- [19] B. Lu, T. Palacios, D. Risbud, S. Bahl, and D. I. Anderson, "Extraction of dynamic on-resistance in GaN transistors: Under soft- and hard-switching conditions," in *2011 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)*. Waikoloa, HI, USA: IEEE, Oct. 2011, pp. 1–4.
- [20] T. G. Bade, H. Hamad, A. Lambert, H. Morel, and D. Planson, "Threshold Voltage Measurement Protocol 'Triple Sense' Applied to GaN HEMTs," *Electronics*, vol. 12, no. 11, article n. 2529, may 2023
- [21] JEDEC comitee JC-70.2, "JEP184 - guideline for evaluating bias temperature instability of silicon carbide metal-oxide-semiconductor devices for power electronic conversion," Mar. 2021. [Online]. Available: https://www.jedec.org/document_search?search_api_views_fulltext=JEP184