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# Concept and technology for full monolithic MOSFET and JBS vertical integration in multi-terminal 4H-SiC power converters

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For electric vehicles, there is a growing interest for the monolithic integration of dedicated power conversion functions in SiC dies [1]. Power converters are today realized using single VDMOS bonded on a power substrate using multiple bond wire interconnections [2], these last requiring an expensive operation time-consuming and source of aging problems [3]. In silicon carbide, few works are reported on the monolithic integration of power functions built with vertical VDMOS, most of them focused on the integration of auxiliary low-voltage functions [4].

The present paper explores the monolithic integration in SiC, within a single chip, of vertical switching cells based on JBS diodes and VDMOS. It proposes new and original medium power multi-terminal SiC converter architectures: Buck, Boost, H-bridge high-side row chip common drain-type and low-side row chip common source-type. This ultimate efficient power vertical integration proposed, using a minimum number of chips, will improve further the performance, reliability and cost reduction of the currently used discrete-dies-based switching cells.

These vertical multi-terminal integrated architectures, presented in Fig. 1 (Buck and Boost) and Fig. 2 (H-bridge high-side and low-side dual-MOSFET) have been designed in order to support an applied voltage, up to 800 V, both vertically and laterally at the upper-side of the chip, and to carry a nominal current of 10 A. The operating modes, off-state, on-state and switching, were validated through 2D TCAD Sentaurus<sup>TM</sup>. Mixed-Mode simulations [5]. Particular attention was paid to the distribution of equipotential lines and current density within the elementary chip (Fig. 3 and Fig. 4) in order to limit the electric field peaks to 2.1 MV/cm, lower than the critical electrical field in SiC. Technological parameters have been determined as thickness and doping layers, junction termination extension (JTE) length, or minimal lateral distances to withstand the high voltage between the different integrated vertical MOSFET and JBS diodes (Fig. 5). The switching on/off waveforms of the individual part of the multi-terminal structures are presented in Fig. 6.

A first key technological step has been developed to insulate vertically the individual integrated transistors and diodes. Electrical insulation using a deep trench in the back-side and a p-type highly doped, deep well, above this trench is introduced. P<sup>+</sup>-layers are created by aluminum ion implantation and high temperature activation annealing [6]. The trench in the back-side SiC wafers is created by mask patterning, fluorinated plasma etching and electrochemical etching utilizing p-type created wells as stopping layers to selectively etch the N<sup>+</sup>-substrate (Fig. 7). A second key technological step has been developed for the Buck and Boost structures. A via in trench is created in the front-side by fluorinated plasma etching, filled with Ni metal by electroplating (Fig. 8) to connect the VDMOS and the JBS from one side to the other of the SiC wafer. Ni is preferred to Cu due to the MOSFET process compatibility.

At the conference and in the final paper, results from the first fabricated run will be presented.

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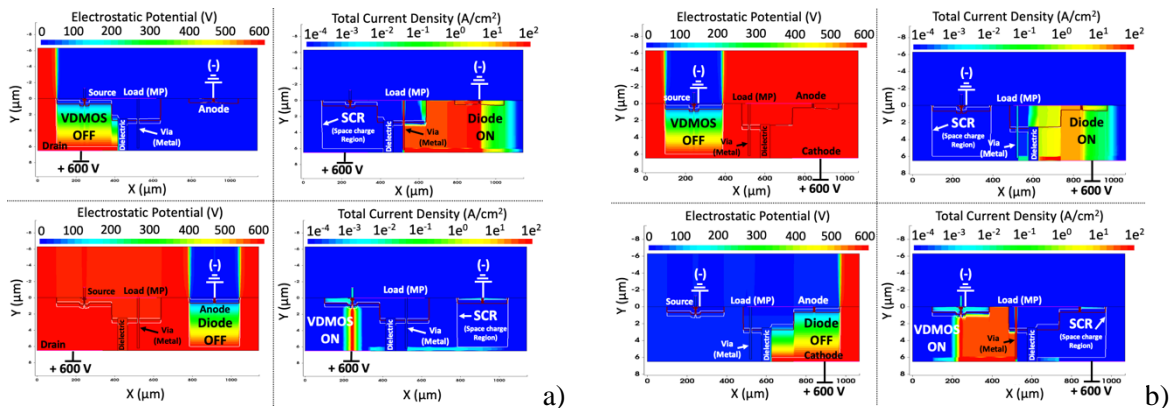
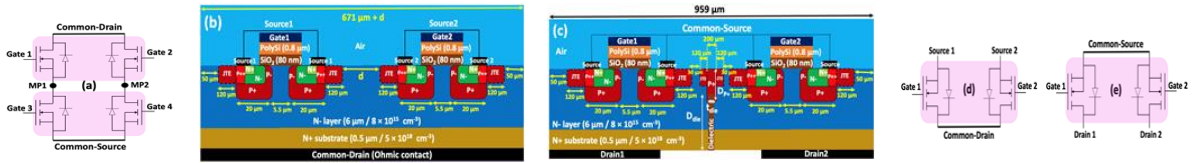
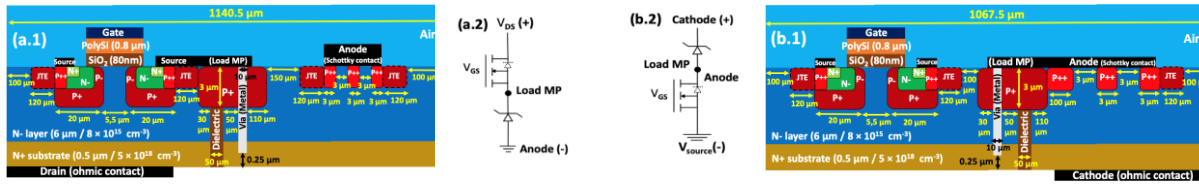


Fig. 3. Equipotential lines and current density distribution in the Buck (a) and Boost-type (b) switching cell

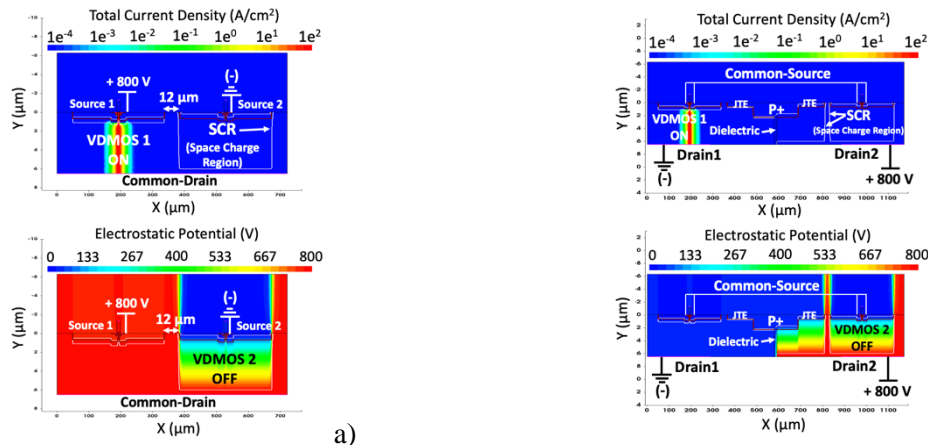


Fig. 4. Equipotential lines and current density distribution in the common-drain (a) and common-source (b) type three-terminal H-bridge SiC MOSFET power chip (X to Y ratio: 30)

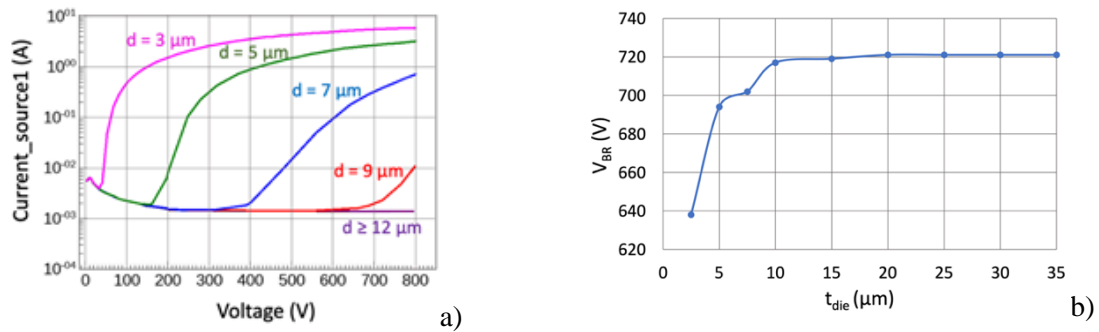


Fig. 5. Variation of the breakdown voltage of the common-drain H-bridge structure as a function of the distance “d” between the two MOSFET (a) and as a function of the dielectric thickness “ $t_{die}$ ”.

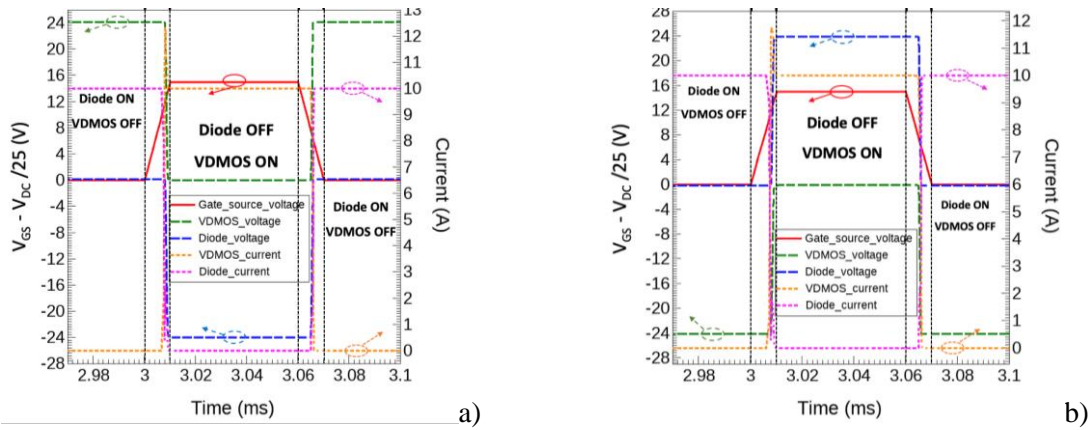


Fig.6. MOSFET-part and JBS-part switching waveforms of the proposed 3-pole Buck (a) and Boost-type (b) switching cell at  $V_{DC} = 600\text{V}$ ,  $I_{LOAD} = 10\text{A}$ ,  $V_{GSmax} = 15\text{V}$ ,  $T_{CASE} = 300\text{K}$ .

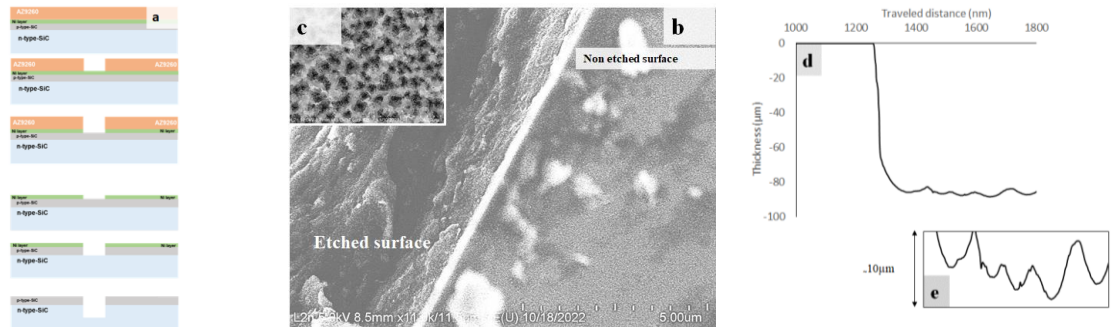


Fig. 7. Surface patterning with p-type layers (a), SEM image of electrochemical etched surface (b). Inset showed the obtained porous surface (c),  $\alpha$ -step thickness (d) and roughness (e) measurements.

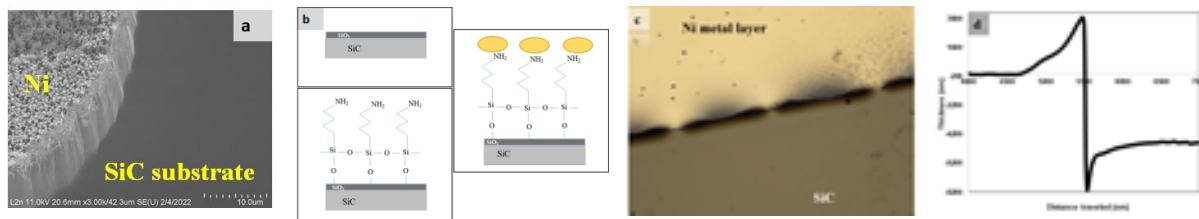


Fig. 8. SEM images of a  $10\mu\text{m}$  thickness SiC substrate etched with Ni mask to perform the metallic via between the back-side cathode JBS-part and the front-side VDMOS-part (a), electroplating process to fill the via with Ni (b), optical image of the Ni electroplated layer on the SiC (c) and  $\alpha$ -step measurement of the Ni metal layer performed (d).

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