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***Abstract*—** The spin of an electron confined to a semiconductor quantum dot is one of the main technology platforms currently evaluated in the pursuit of qubit implementation. In this study, we developed and optimized a full simulation process flow used to model an Ultra-Thin Body and Buried oxide (UTBB) Fully Depleted Silicon-On-Insulator (FD-SOI) quantum dot device fabricated using STMicroelectronics' standard manufacturing process. Here, we report optical, geometrical, electrical, and quantum numerical results that allowed us to assess the device performance before its eventual fabrication.

Keywords- FD-SOI CMOS, silicon quantum dots, quantum information, optical lithography modeling, 3D TCAD simulations, cryogenic temperatures

I. INTRODUCTION

Compared to its classical counterpart, a quantum computer promises to solve certain computation problems considered notoriously difficult even for today's most powerful supercomputers, and even promises exponential speedup for certain applications such as simulation of quantum systems [1]. The quantum equivalent of bits of information used in classical computers is known as a quantum bit or qubit. Among the several physical systems currently explored for the realization of qubits, spin-based qubits implemented in quantum dots hosted in silicon nanostructures have attracted a wide interest [2]. In such systems, quantum information is processed by manipulating the spin of a single electron or hole confined in the dot.

One of the most striking features of this approach is its ability to leverage the well-matured mass-production processes from the field of microelectronics, which have undergone a decades-long trajectory of development and standardization. The CMOS compatibility makes it possible to envision mass production of spin qubits in the silicon foundries used in modern computer industries, ensuring manufacturing yield, uniformity, and reproducibility of devices [3-5].

The quantum dot device presented here is based on STMicroelectronics' industry-standard 28 nm Ultra-Thin Body and Buried oxide (UTBB) Fully Depleted Silicon-On-Insulator (FD-SOI) technology [6-7]. In order to meet the device dimensions and characteristics required for quantum information processing, while shortening the time-consuming fabrication and characterization optimization loop, it is crucial to simulate and evaluate its performance prior to its eventual fabrication.

In this paper, we present our simulation process flow used for the implementation of our FD-SOI quantum dot device. The proposed flow consists of a sequence of simulations, starting from the optical lithographic fabrication of our structure, moving on to the geometric representation and electrical behavior, and ending with the quantum-mechanical features. For the modeling of our device, we used respectively STMicroelectronics' internal software Optical Friendly DEsign Check (OFDEC), the 3D TCAD Sentaurus Process [8], and 3D Quantum TCAD [9, 10] simulation tools. The numerical results presented here indicate that the formation of unwanted corner quantum dots and barrier control issues that arose in our previous-generation nanostructure [11] have now disappeared. Moreover, our simulations suggest that control of the wavefunction location may be achieved through back-gate biases, which forecasts advantages of the FD-SOI technology for quantum computing applications over other competitor technologies [12].

II. QUANTUM DOT DEVICE LAYOUT

A schematic representation and TEM images of the quantum dot device studied here are shown in Figure 1. The figure illustrates some of the main characteristics of the 28 nm UTBB FD-SOI technology, namely, the epitaxially grown source and drain, two-level spacers, top polysilicon gates, and the back plane serving as a back gate. Compared to our previous-generation device, the

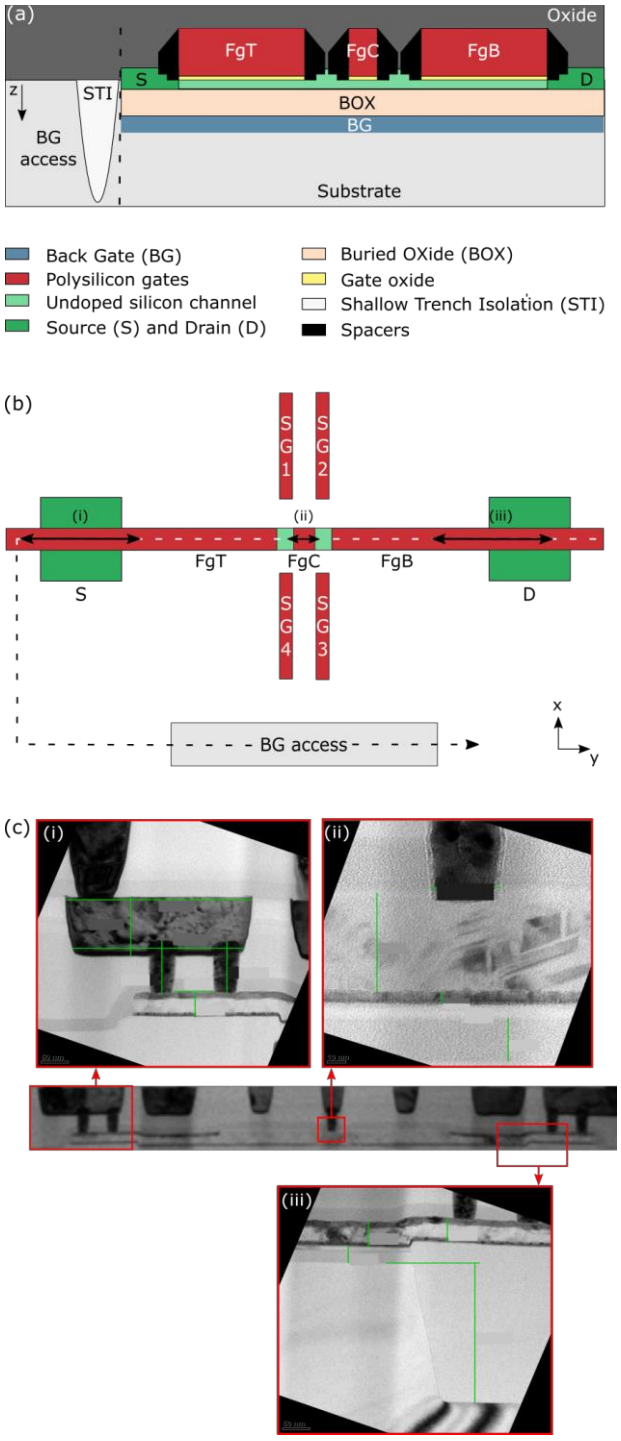

Figure 1. (a) Schematic representation of the cross-section of the quantum dot device parallel to the z-axis. A lateral access to the back gate is illustrated following the linecut in Fig. 1 (b) for simplicity. (b) Schematic representation of the top view of the quantum dot device in the xy-plane. (c) TEM image of the fabricated quantum dot device extracted along the conduction channel in the direction of the dashed white line, as depicted in Figure 1 (b).

width of the conduction channel was reduced to match that of the front gates FgT, FgC, and FgB, avoiding in this way the generation of corner quantum dots by the side gate activation [11]. The square gate, FgC, is designed to control the electrostatic potential of the quantum dot expected to form at this area and splits the front gate into the two parts FgT and FgB. Several interconnection layers offer vertical access to the FgC gate, allowing to envision scalable 2D and 3D split-gate architectures capable of hosting a larger number of quantum dots. Finally, the four lateral gates, SG1, SG2, SG3, and SG4, were designed to control symmetrically the tunnel barriers created by the gaps between FgT, FgC, and FgB.

III. Precision of Gate Pitch

In view of the inaccuracy of the design transfer onto the wafer during the photolithography process, several critical dimensions variations were tested in the layout by simulating the structure using the OFDEC optical lithography simulation tool. Focusing on the most challenging part of the device for fabrication, i.e., the region where the quantum dot is expected to form, Figure 2 (a) shows the modeled top gates and conduction channel (right) based on the device layout used for the Multi-Project Wafer (MPW) manufacturing run (left). Here, the outline of the layout design is displayed on top of the simulated device for comparison. The modeled conduction channel is depicted in yellow, the top gates in purple, and the contact to the first interconnection layer in pink.

For each simulated element, several variations of certain photolithographic parameters were investigated resulting in various critical dimensions and feature widths which are depicted here as a set of overlapping contours. The simulations showed that the square contact was photolithographically transferred onto the wafer as a circular pattern, as expected. In addition, the simulation of the transfer of the gate pattern from the mask onto the SOI wafer resulted in wider gates with rounded corners. Corner rounding and line shortening is generally expected in photolithography and is within the acceptable limits of features infidelity [13]. Finally, the OFDEC simulations helped us select the appropriate design to obtain the desired gaps between the gates FgT, FgB, and FgC, i.e., in the range of 20-50 nm depending on the optical lithography parameters.

Following the OFDEC simulations, the structure was simulated using the Finite Element Modeling (FEM) 3D TCAD Sentaurus Process software developed by Synopsys [8]. In this context, each step of STMicroelectronics' standard FD-SOI manufacturing process was simulated allowing to visualize the 3D structure geometry before its actual fabrication and to estimate the critical dimensions of the device. Figure 2 (b) presents the simulated structure. For a better visibility over the structure, the modeled oxide and nitride layers, namely the BOX, STI, and spacers, were excluded in the figure presented here. In addition, the various copper interconnect layers routing the device to the bonding pads were not considered during the simulations.

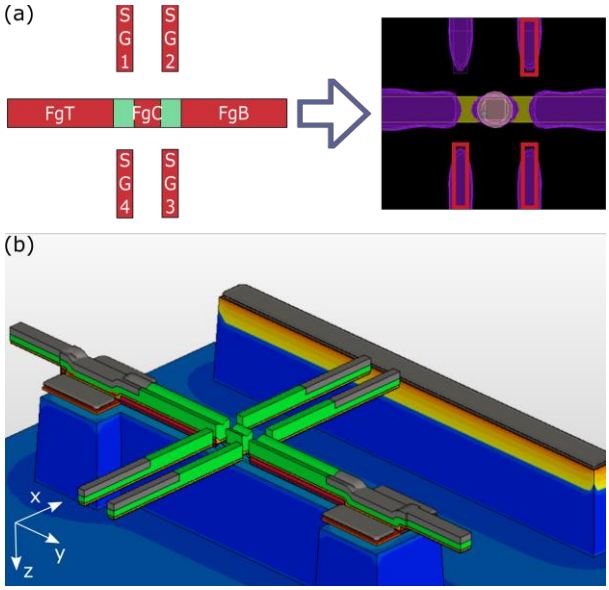

Figure 2. (a) Optical lithography simulation of the quantum dot device using STMicroelectronics' OFDEC software. Left: device layout focusing on the region where the quantum dot is expected to form. Right: simulated features printed onto the SOI wafer. (b) Quantum dot device simulated using the 3D TCAD Process modeling tool based on the layout used for MPW fabrication of the nanostructure.

IV. Controlling the Barrier Heights

The electrostatic profile of the quantum dot device was simulated using QTCAD [9]. More precisely, we used the QTCAD non-linear Poisson solver to compute the conduction-band edge, E_c, throughout the device. Convergence was achieved to within 1 mV at a temperature at which we expect the device to operate, i.e., $T = 1.4\,K$ [10, 11]. In Figure 3 (a), linecuts of E_c are plotted, taken along the transport direction and at 0.1 nm below the Si/SiO_2 interface situated between the channel and the front gates. Here, E_c was computed for the following bias configurations: the bias applied to the front gates, FgB and FgT, was $\varphi_T = \varphi_B = 1\,V$, the bias applied to FgC was $\varphi_C = 0.8\,V$, the back-gate bias was fixed at VB = 0 V, the bias applied to SG1 and SG4 was $\varphi_1 = \varphi_4 = 0\,V$, and the bias applied to SG2 and SG3, $\varphi_2 = \varphi_3$ was varied. In these plots, the Fermi level corresponds to 0 eV. At low temperatures, only regions with $E_c < 0$ eV contain occupied electron states. To the far left and right, E_c is very far below the Fermi level. These are the source and drain regions containing electron reservoirs. The bias applied to the front gates FgT and FgB allows these reservoirs to be extended toward the center of the device where the dot is formed. We can see from Figure 3 (a) that increasing the side gate voltage $\varphi_2 = \varphi_3$ lowers the dot-drain barrier.

For $\varphi_2 = \varphi_3 = 0$ V, this barrier has a height of 300 meV, which, for all intents and purposes, completely isolates quantum-dot electrons from the drain reservoir. We can however lower this barrier ($\varphi_2 = \varphi_3 = 8$ V) below the Fermi level allowing electrons to tunnel freely from the dot to the drain. The symmetric nature of the system would also allow us to lower the source-dot barrier by varying $\varphi_1 = \varphi_4$. Consequently, the side gates can be leveraged to modify the tunneling into and out of the dot.

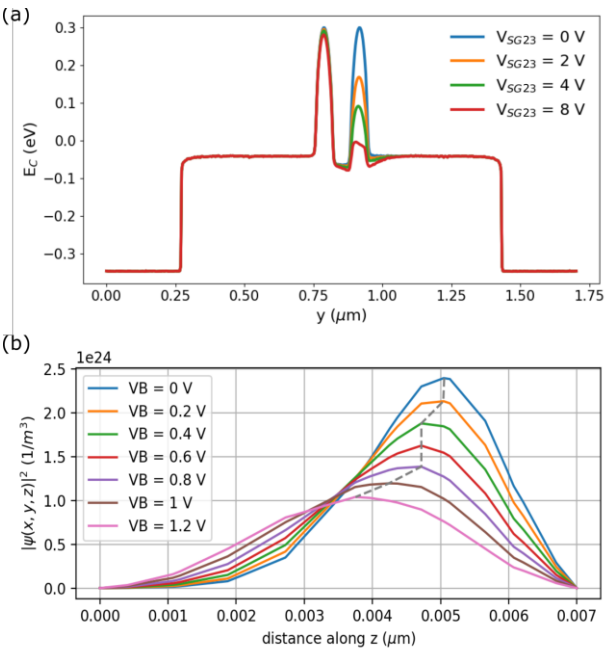

Figure 3. (a) QTCAD-simulated conduction band edge at a linecut taken at 0.1 nm below the top gate oxide into the conduction channel parallel to transport. A 2DEG at the Si/SiO_2 interface is observed, along with the ability to tune the potential barrier height by biasing the lateral gates. A voltage sweep is performed to SG2 and SG3 simultaneously with a grounded back gate. (b) QTCAD-simulated ground-state wavefunction along a linecut perpendicular to the conduction channel and at the center of the gate FgC. The grey dashed line tracks the maximal value of the wavefunction for different back-gate voltages. The ability to manipulate the wavefunction via the back gate is observed. Using the back gate, the electron can either be forced toward a Si/SiO_2 interface to maximize the valley splitting or moved away from the interfaces to protect the qubit from interface defects.

Moreover, we note that because the barrier heights can be continuously tuned from 0 to 300 meV, the system can be tuned from a regime where quantum dot electrons cannot be distinguished from reservoir electrons to one where there is no overlap between quantum dot and reservoir electrons. Correspondingly, we can envisage an operational scheme where the barriers are lowered to load electrons in (initialization) and out (readout) of the dot and the barriers are raised when qubit gates are performed on the quantum-dot-confined spin qubit.

V. Wavefunction Manipulation via the Back Gate

Using the QTCAD Schrodinger solver, we also analyzed certain quantum features of the device. For these simulations, we first set $\varphi_1 = \varphi_2 = \varphi_3 = \varphi_4 = 0\,V$ to isolate the quantum dot from the source and drain reservoirs. We then used the non-linear Poisson solver to compute the quantum dot confinement potential for different back gate biases. For each back gate bias, we solved the Schrodinger equation in a region below FgC to obtain the quantum dot orbital wavefunctions. The ground-state orbital is plotted in Figure 3 (b) along a linecut through the silicon channel (green region in Figure 1). The linecut was taken at the center of FgC starting from the silicon channel/BOX interface and ending at the Si/SiO_2 interface situated between the channel and the front gates. We observe that as the back gate bias, VB, increases, the ground state orbital is shifted toward the Si/BOX interface. In particular, when VB=1.2 V, the peak of the wavefunction is identified close to the center of the channel. Since the wavefunction is furthest from both interfaces in this configuration, it is less susceptible to interface defects. In contrast, when VB=0 V, the wave function is closest to the Si/SiO_2 interface between the channel and the front gates – the sharp confinement potential variation at this interface may then lead to a significant valley splitting [14]. Consequently, we may envision tuning the back gate between 0 V, to maximize valley splitting during qubit manipulation, and 1.2 V, to minimize sensitivity to interface defects and increase coherence between quantum-logic gates.

VI. Conclusion

In conclusion, we presented our work on a quantum dot device potentially suitable for quantum computing applications, based on STMicroelectonics' standard-process 28 nm UTBB FD-SOI planar technology. To optimize our design before the actual fabrication of the device, we developed a dedicated simulation process flow, aiming to reduce device fabrication risk and improve turnaround times. This flow involves a series of simulations, including optical, geometric, electrical, and quantum-mechanical property estimations, which are carried out using OFDEC, 3D TCAD Sentaurus Process and 3D QTCAD software tools, respectively. The first two simulation tools allowed us to define the critical dimensions of the device and the latter to evaluate its potential for quantum information processing. Finally, the simulation process flow presented in this paper can be also used for the realization of FD-SOI quantum dot devices based on smaller technology nodes, such as 22 nm, 18 nm and the soon-to-be-developed, 10 nm UTBB FD-SOI.

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