



What brings diamond compared to wide bandgap materials in power semiconductor devices?

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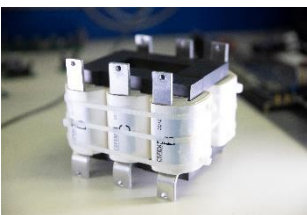
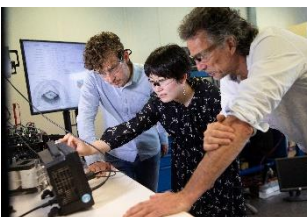
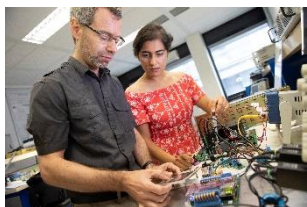
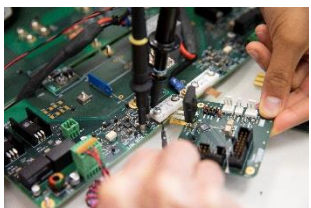
Submitted on 28 Sep 2023

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What brings diamond compared to wide bandgap materials in power semiconductor devices?

Session 4A: Diamond Power Devices I

**Invited speaker*

Sept 11th 2023

Nicolas ROUGER, CNRS Research scientist

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Outline

1. Power semiconductor devices

- A. Specificities and benchmarking
- B. Impact of WBG power devices vs. Silicon

2. Diamond for power electronics

- A. Unique properties of diamond
- B. Benefits & benchmark of diamond

3. What's next?



This project has received funding from the Clean Sky 2 Joint Undertaking (JU) under grant agreement No 101007868. The JU receives support from the European Union's Horizon 2020 research and innovation program and the Clean Sky 2 JU members other than the Union.

A close-up photograph of a power semiconductor device assembly. It shows a green printed circuit board (PCB) populated with various electronic components, including integrated circuits, resistors, and capacitors. The PCB is mounted on a copper heat sink, which is secured with several silver-colored screws. The assembly is part of a larger system, with other components visible in the background.

Part 1

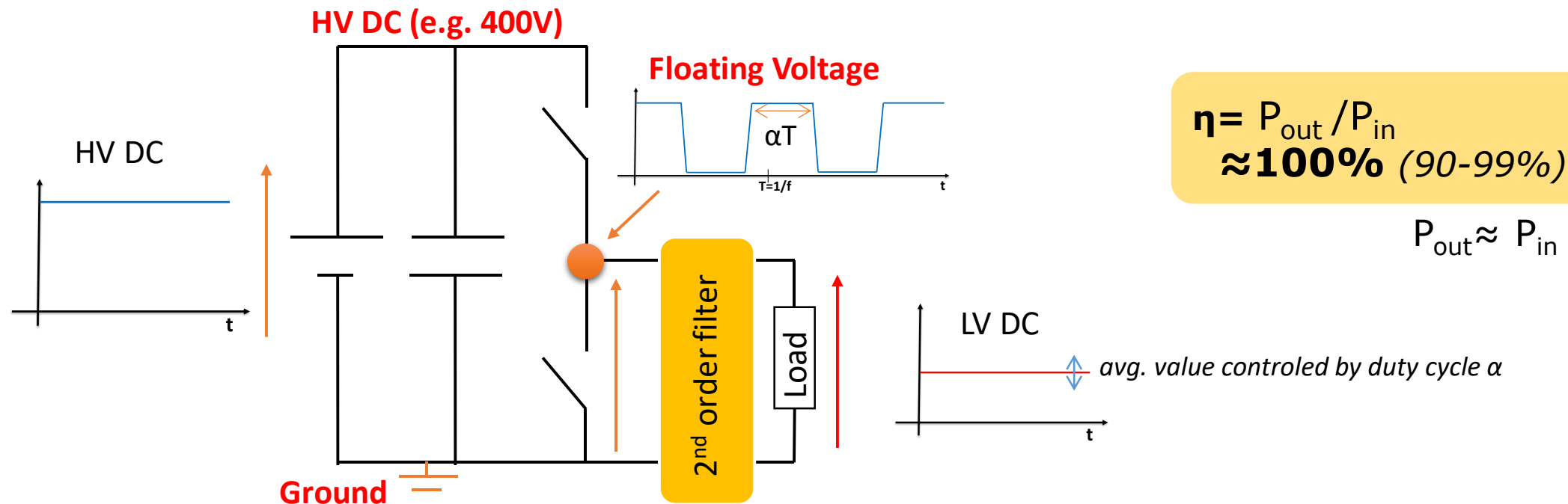
Power semiconductor devices

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Power electronics

e.g. Half bridge / Buck Converter (DC/DC)

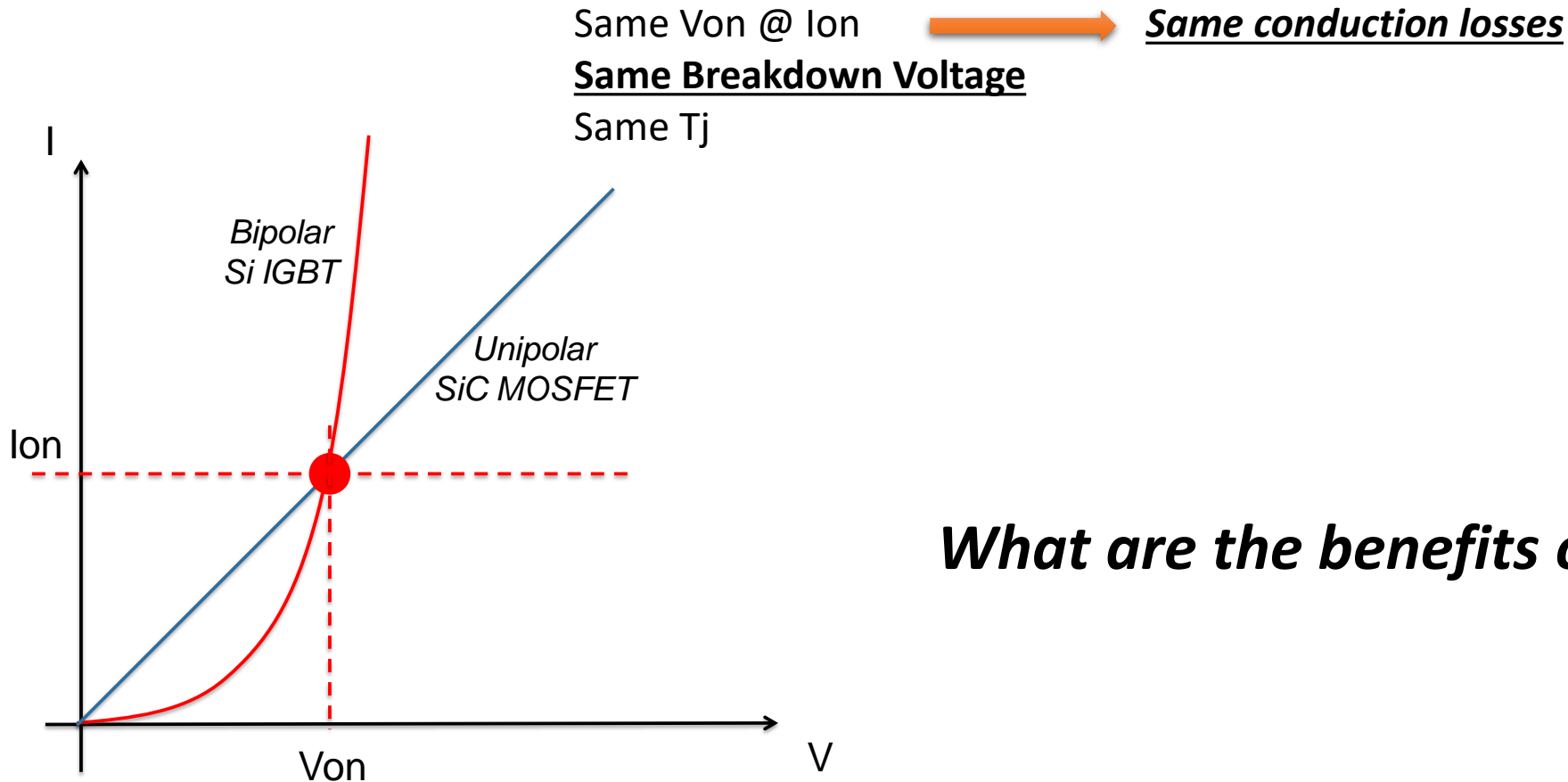
- Target 100 % efficiency
- Constraints on weight (volume), safety & reliability, cost, standards, adaptability to operating conditions, ...



Power semiconductor devices

How to compare / Benchmark?

e.g. Si vs. SiC (WBG)

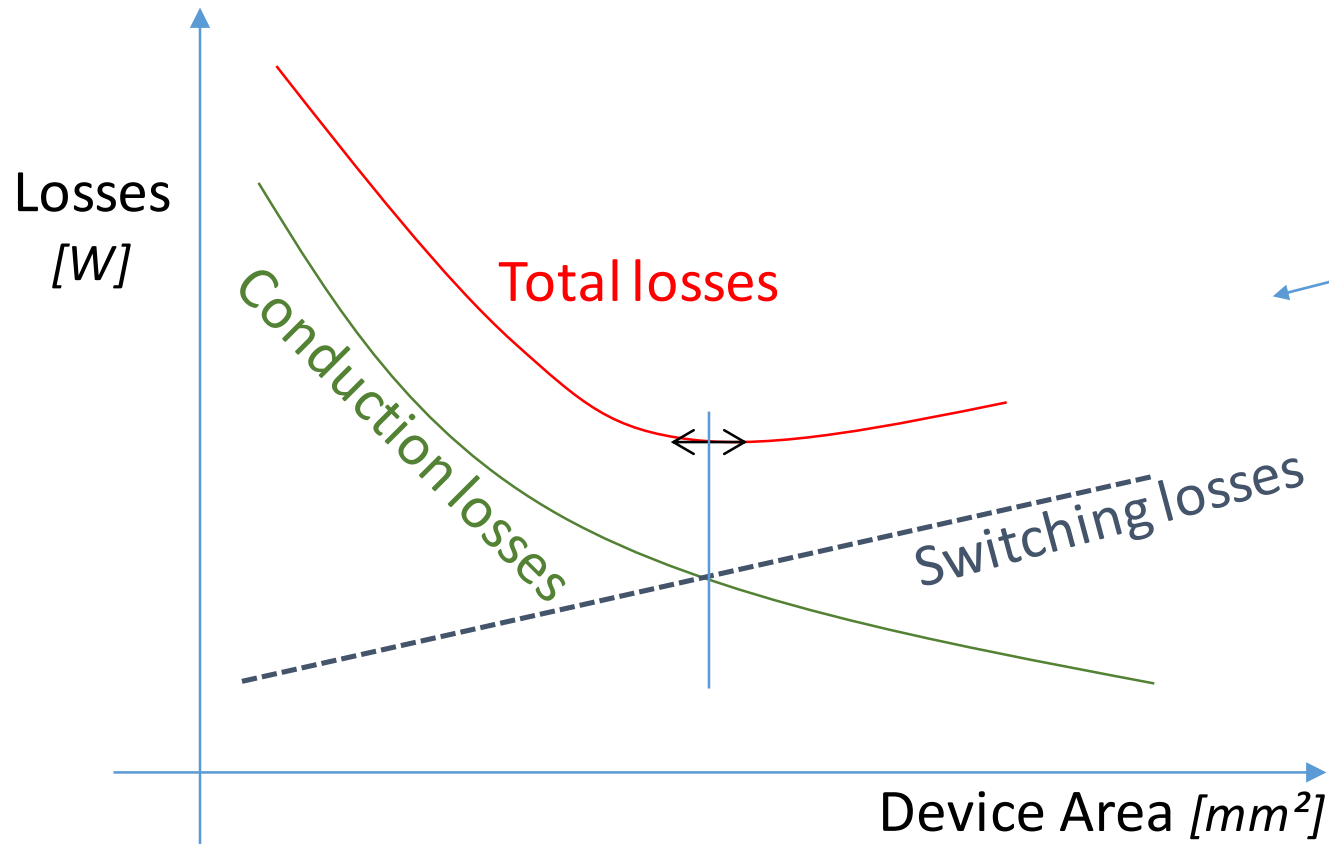


What are the benefits of (U)WBG vs. Si?

Power semiconductor devices

How to compare / Benchmark?

e.g. Carrier Lifetime Control and optimal area



Same specifications
Same technology
Same Tj
Same Carrier Lifetime



Trade off and optimization!
Multiple variables

A detailed, close-up photograph of a microchip or integrated circuit. The chip is a yellowish-brown color with a complex pattern of fine, dark lines representing the circuitry. Several circular pads are visible along the left edge, and a series of small, dark, rectangular components are arranged in a row along the bottom edge. The background is a solid black.

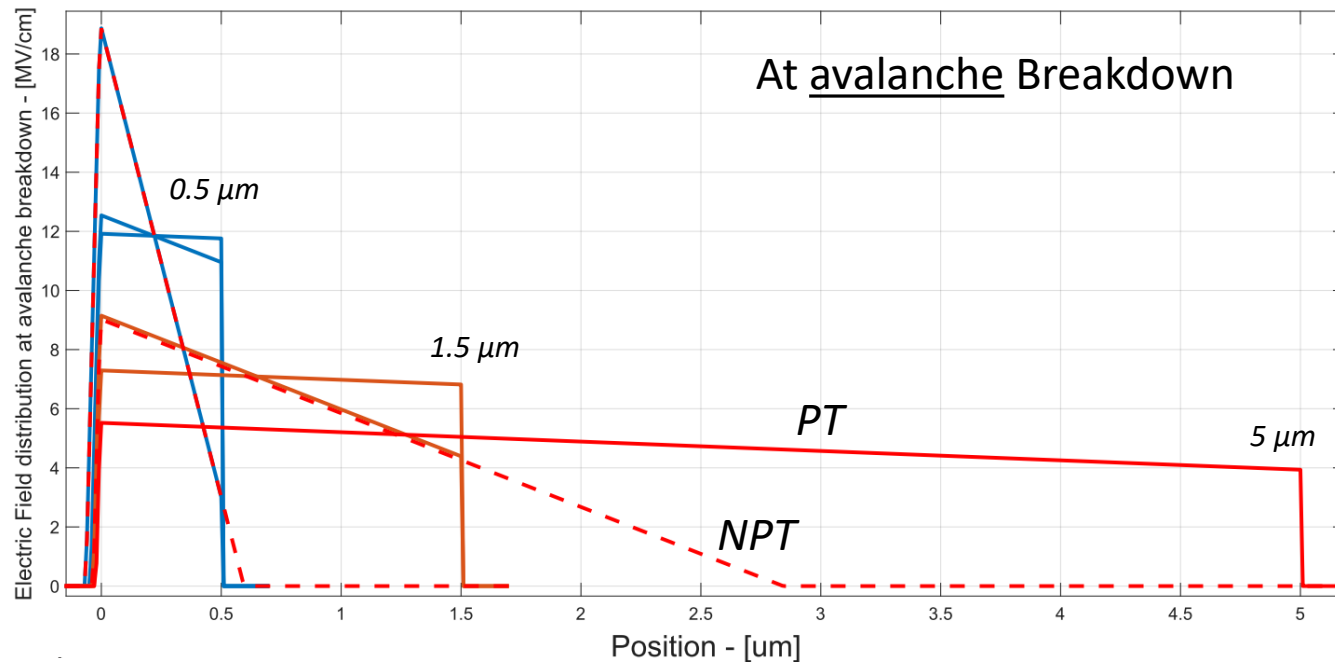
Part 2

Diamond for power electronics

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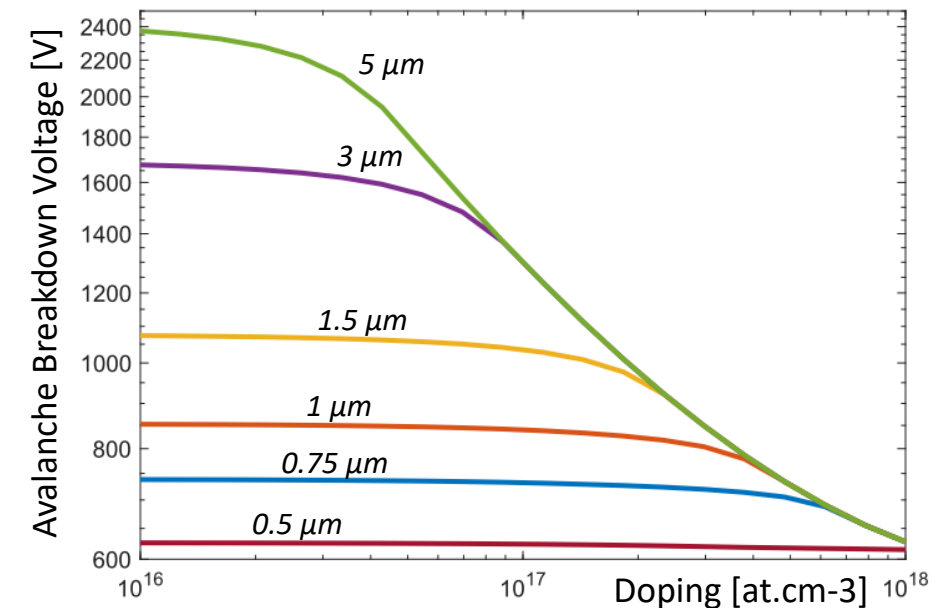
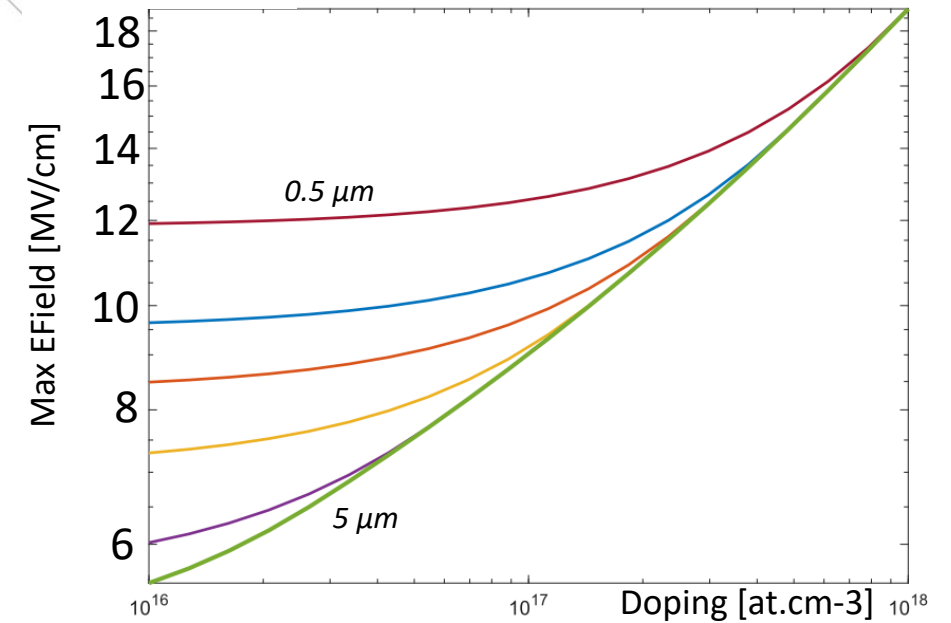
Benchmark: Diamond

Critical Electric Field of Diamond?

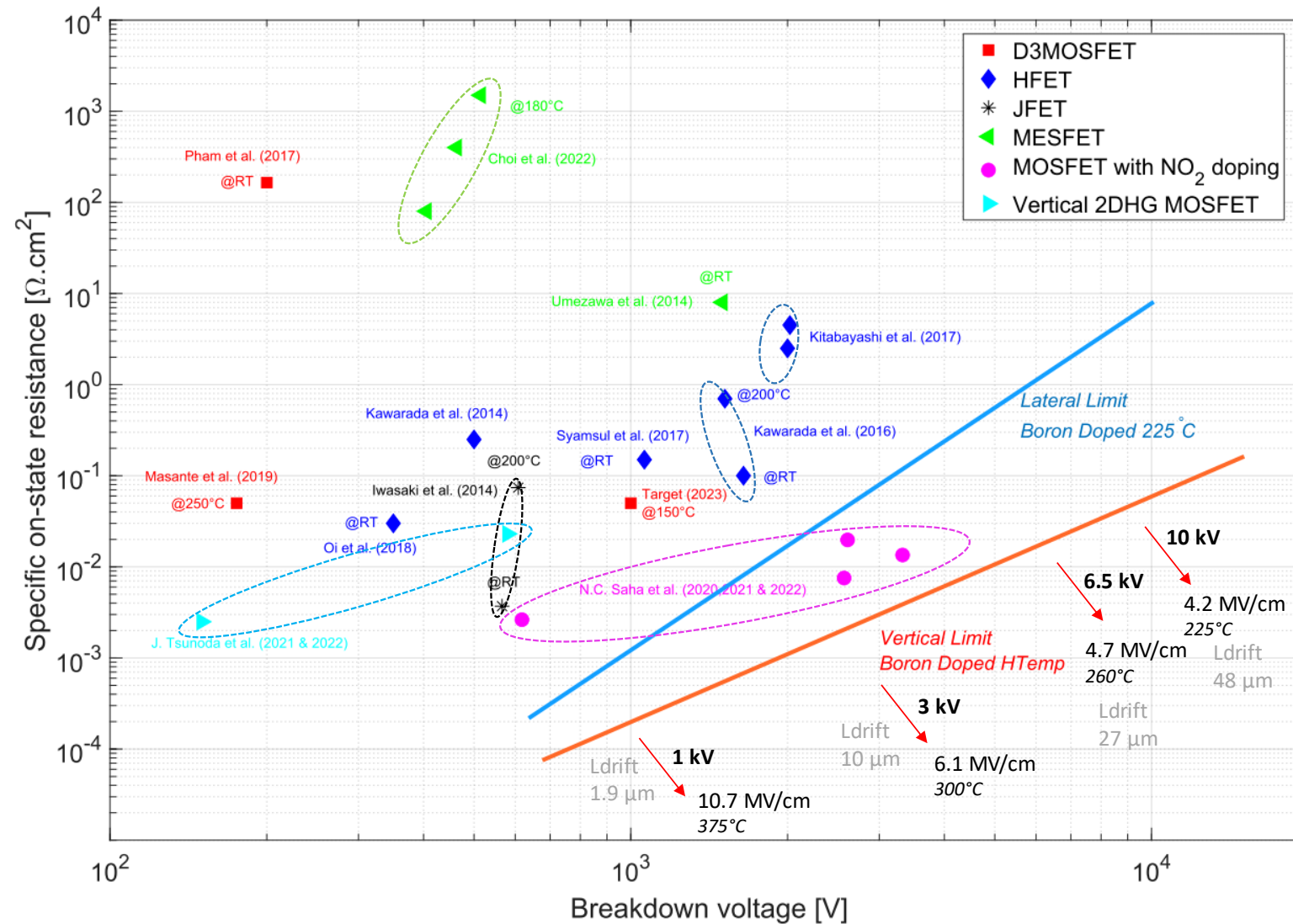


$$\alpha_p = a_p \exp\left(\frac{-b_p}{|E|}\right), \alpha_n = a_n \exp\left(\frac{-b_n}{|E|}\right)$$

[A. Hiraiwa, H. Kwarada, 2013, JAP 114 034506]



Benchmark: Diamond



Models for diamond limits:

1D Avalanche Breakdown & NPT

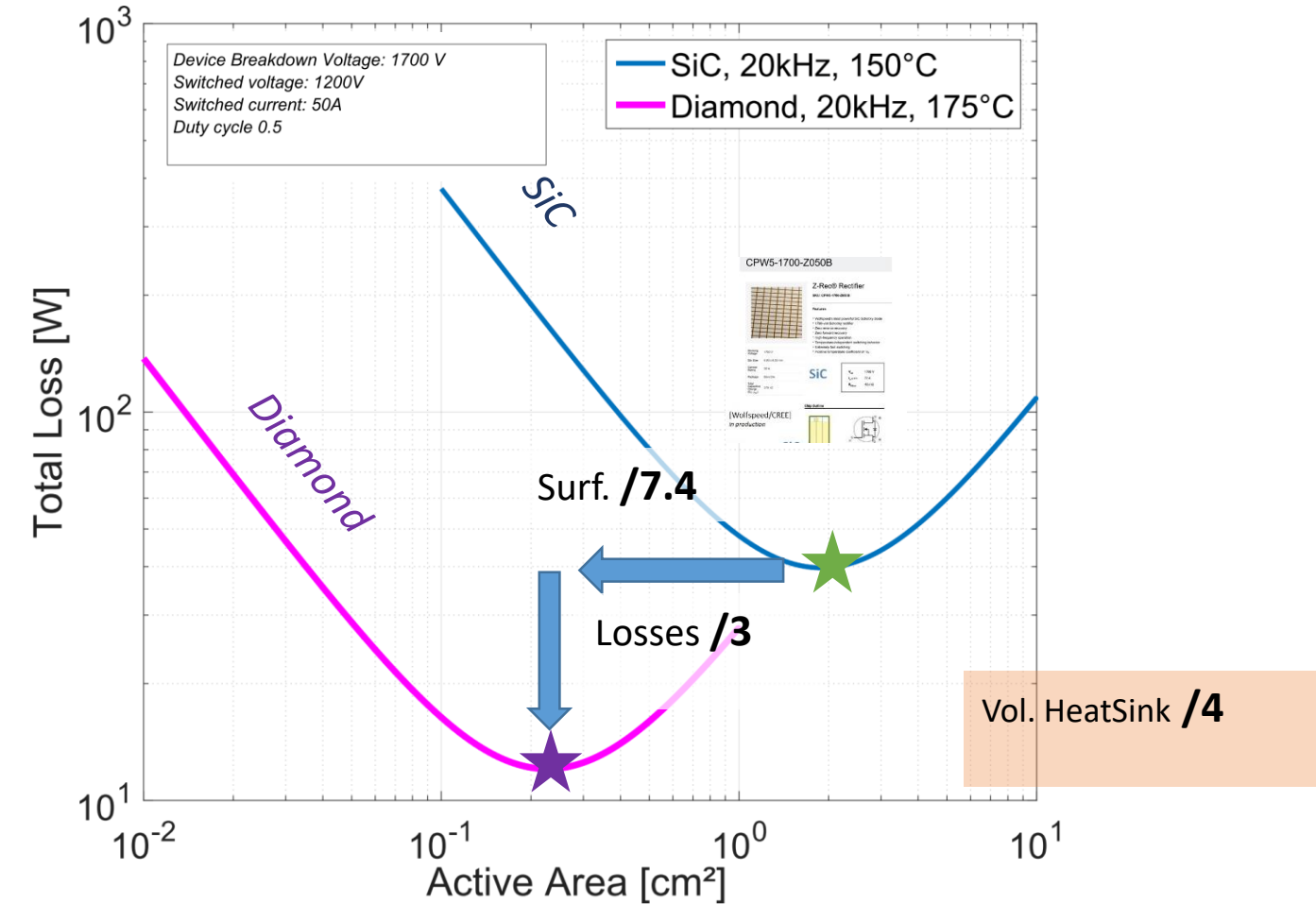
Inc. Ionization diamond
[B] Doped diamond

Drift region only

...

[M. Couret et al, 2023, Diamond & Related Materials Vol 135, 109 827,
10.1016/j.diamond.2023.109827]

Benchmark: Diamond vs. SiC



[N Donato, N. Rouger et al 2020 J. Phys. D: Appl. Phys. **53** 093001]

1D Avalanche Breakdown & NPT

Inc. Ionization diamond

[B] Doped diamond

Non linear Coss for Eon switching energy

$E_{off}=0$

Vertical architecture

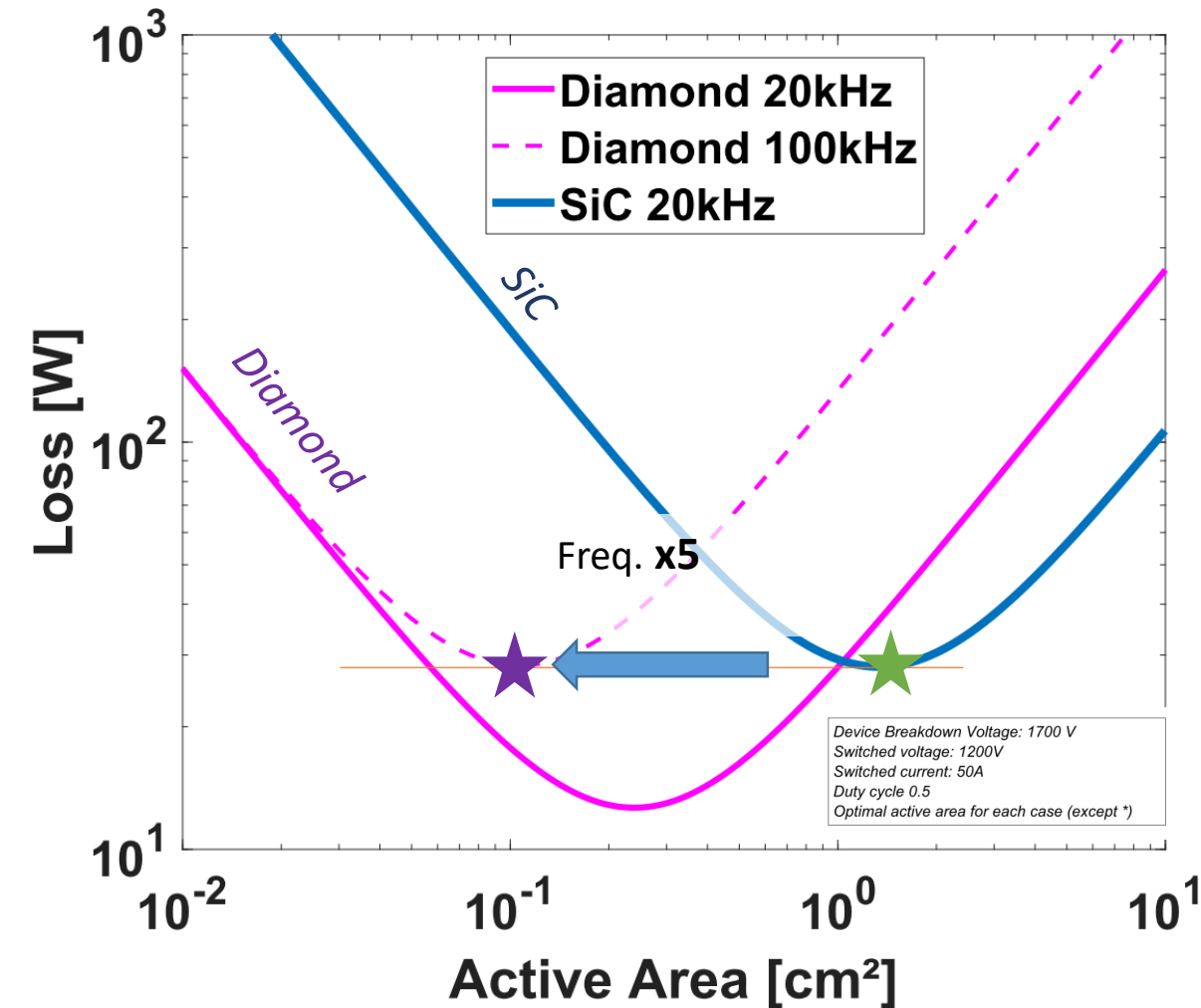
Drift region only

300K Ambient w/ natural convection

...

Fair but still to be discussed

Benchmark: Diamond vs. SiC

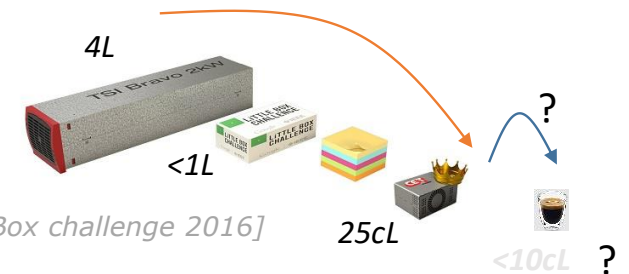


[N Donato, N. Rouger et al 2020 J. Phys. D: Appl. Phys. **53** 093001]

Other design:

If $P_{\text{Diam.}} = P_{\text{SiC}}$ then

f x5 => Passive Volume **/3 to 5**
 HeatSink Volume **-16% to -30%**



[IEEE/Google Little Box challenge 2016]

Same output power



(Losses / Area) x 10!

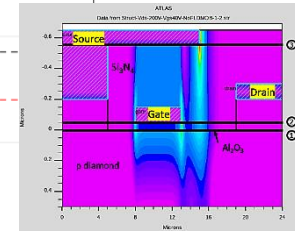
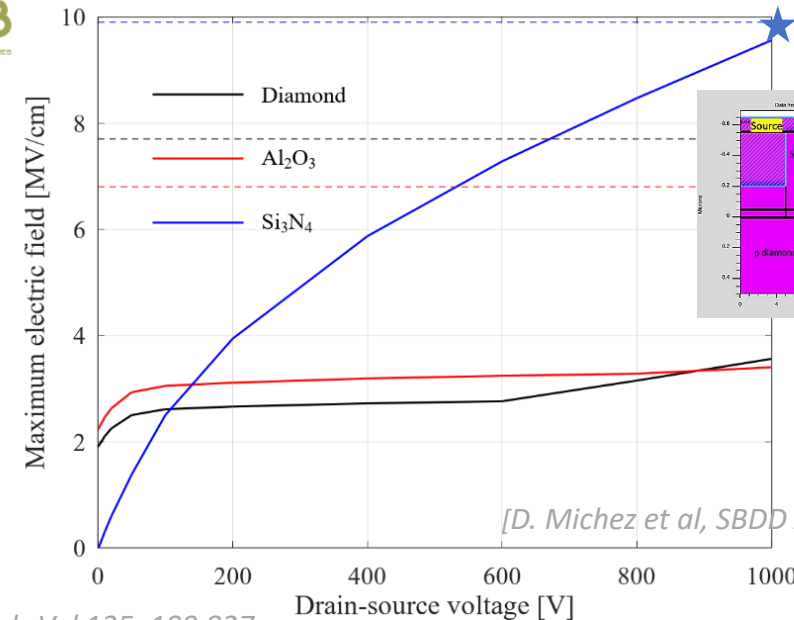
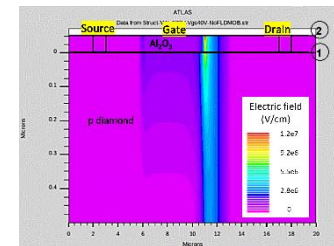
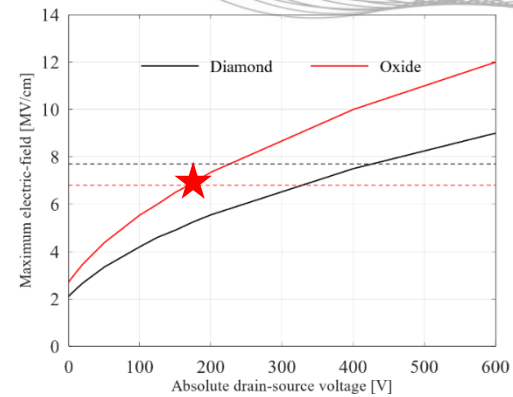
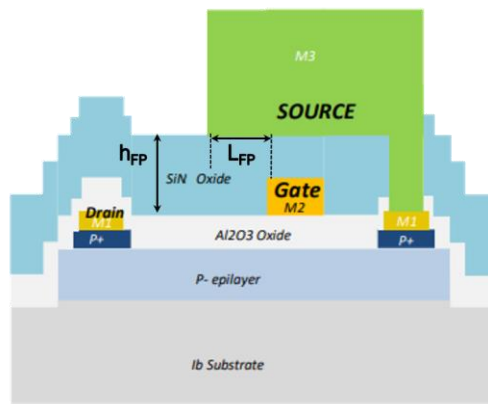
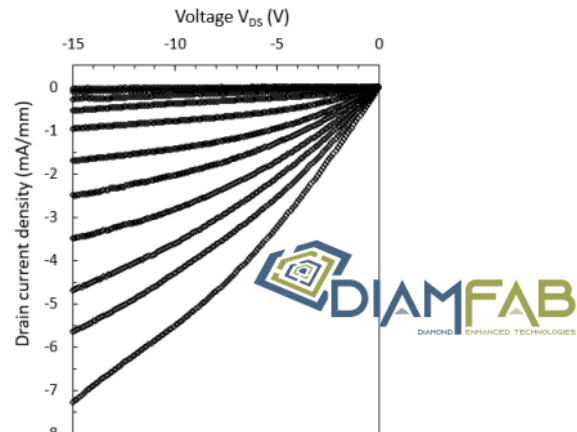
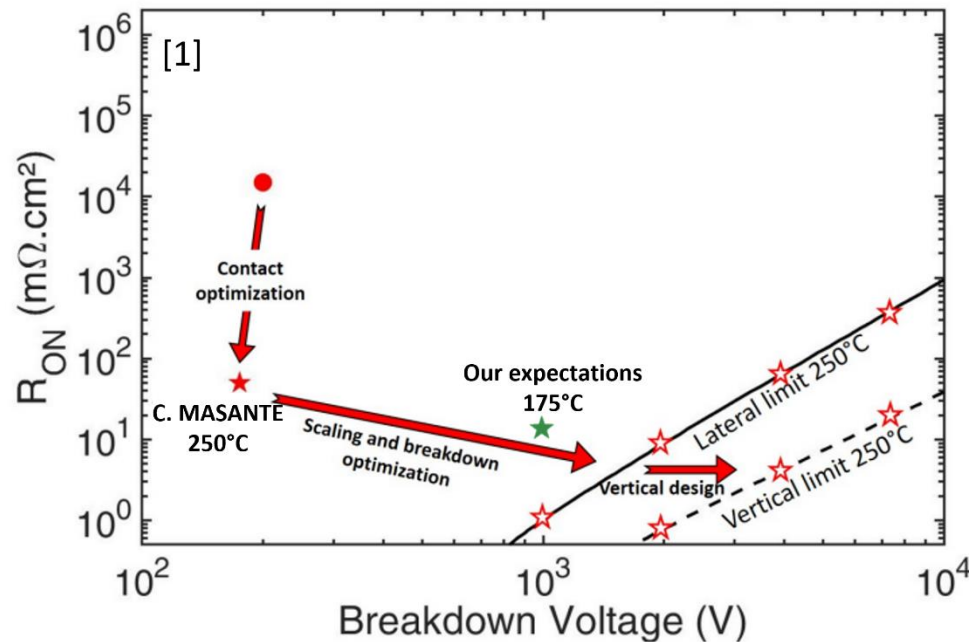


Part 3

What's next?

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Improved FOM *Lateral D3MOSFET* O-term



[M. Couret et al, 2023, Diamond & Related Materials Vol 135, 109 827, 10.1016/j.diamond.2023.109827]

[D. Michez et al, SBDD XXVII 2023]



Conclusion

Benefits of Diamond e.g. vs. SiC

- **7 times smaller** die, with **3 times less total losses**
- **4 times smaller heatsink** or **5 times higher switching frequency**

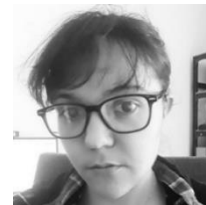


Challenges

- **Ecrit** for lightly doped and thick diamond?
- How to reach highest 1D **BV** with actual **3D** devices?
- **Large area** diamond devices with good FOM
- High quality & conductive substrate for **vertical** devices?
- **Switching losses** of diamond devices are unknown
- **Power loss density** P/S is expected to increase



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DCADE



2021-2023

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Dr. D. Eon



Pr. E. Gheeraert



D. Michez

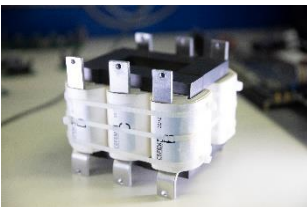
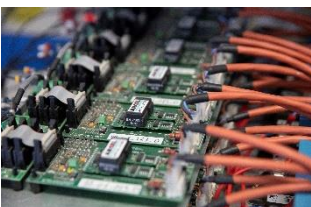
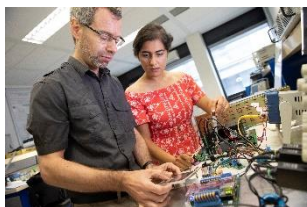


Dr. J. Letellier



Dr. K. Driche & Dr. G. Chicot





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