



HAL
open science

Recent developments and prospects of fully recessed MIS gate structures for GaN on Si power transistors

Pedro Fernandes Paes Pinto Rocha, Laura Vauche, Patricia Pimenta-Barros, Simon Ruel, René Escoffier, Julien Buckley

► To cite this version:

Pedro Fernandes Paes Pinto Rocha, Laura Vauche, Patricia Pimenta-Barros, Simon Ruel, René Escoffier, et al.. Recent developments and prospects of fully recessed MIS gate structures for GaN on Si power transistors. *Energies*, 2023, 16 (7), 10.3390/en16072978 . hal-04215264

HAL Id: hal-04215264

<https://hal.science/hal-04215264v1>

Submitted on 1 Apr 2024

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.



Distributed under a Creative Commons Attribution 4.0 International License

Perspective

Recent developments and prospects of fully recessed MIS gate structures for GaN on Si power transistors

Pedro Fernandes Paes Pinto Rocha ^{1,2}, Laura Vauche ¹, Patricia Pimenta-Barros¹, Simon Ruel¹, René Escoffier ¹, Julien Buckley^{1*}

¹ Univ. Grenoble Alpes, CEA, Leti, F-38000 Grenoble, France; pedro.fernandespaespintorocha@cea.fr (P.R.); laura.vauche@cea.fr (L.V.); patricia.pimenta-barros@cea.fr (P.B.); simon.ruel@cea.fr (S.R.); rene.escoffier@cea.fr (R.E.); julien.buckley@cea.fr (J.B.)

² Univ. Grenoble Alpes, CNRS, CEA/LETI-Minatec, Grenoble INP, Institute of Engineering and Management University Grenoble Alpes, LTM, Grenoble F-38054, France ; pedro.fernandespaespintorocha@cea.fr (P.R.)

* Correspondence: julien.buckley@cea.fr (J.B.)

Abstract: For High Electron Mobility Transistors (HEMTs) power transistors based on AlGaN/GaN heterojunction, p-GaN gate has been the gate topology commonly used to deplete the Two Dimensional Electron Gas (2-DEG) and achieve a Normally-OFF behavior. But fully recessed MIS gate GaN power transistors or MOSc-HEMTs have gained interest as Normally-OFF HEMTs thanks to the wider voltage swing and reduced gate leakage current when compared to p-GaN gate HEMTs. However the mandatory AlGaN barrier etching to deplete the 2-DEG combined with the nature of the dielectric/GaN interface generates etching related defects, traps and roughness. As a consequence, the threshold voltage (V_{TH}) can be unstable, and the electron mobility is reduced, which presents a challenge for the integration of a fully recessed MIS gate. Recent developments have been studied to solve this challenge. In this paper, we discuss developments in gate recess with low impact etching and Atomic Layer Etching (ALE) alongside surface treatments such as wet cleaning, thermal or plasma treatment, all in the scope of having a surface close to pristine. Finally, different interfacial layers, such as AlN, and alternative dielectrics investigated to optimize the dielectric/GaN interface are presented.

Keywords: MOSc-HEMT; GaN; MOS; Etching; Surface preparation; Insulator; Interface

Citation: To be added by editorial staff during production.

Academic Editor: Firstname Last-name

Received: date

Accepted: date

Published: date

Publisher's Note: MDPI stays neutral with regard to jurisdictional claims in published maps and institutional affiliations.



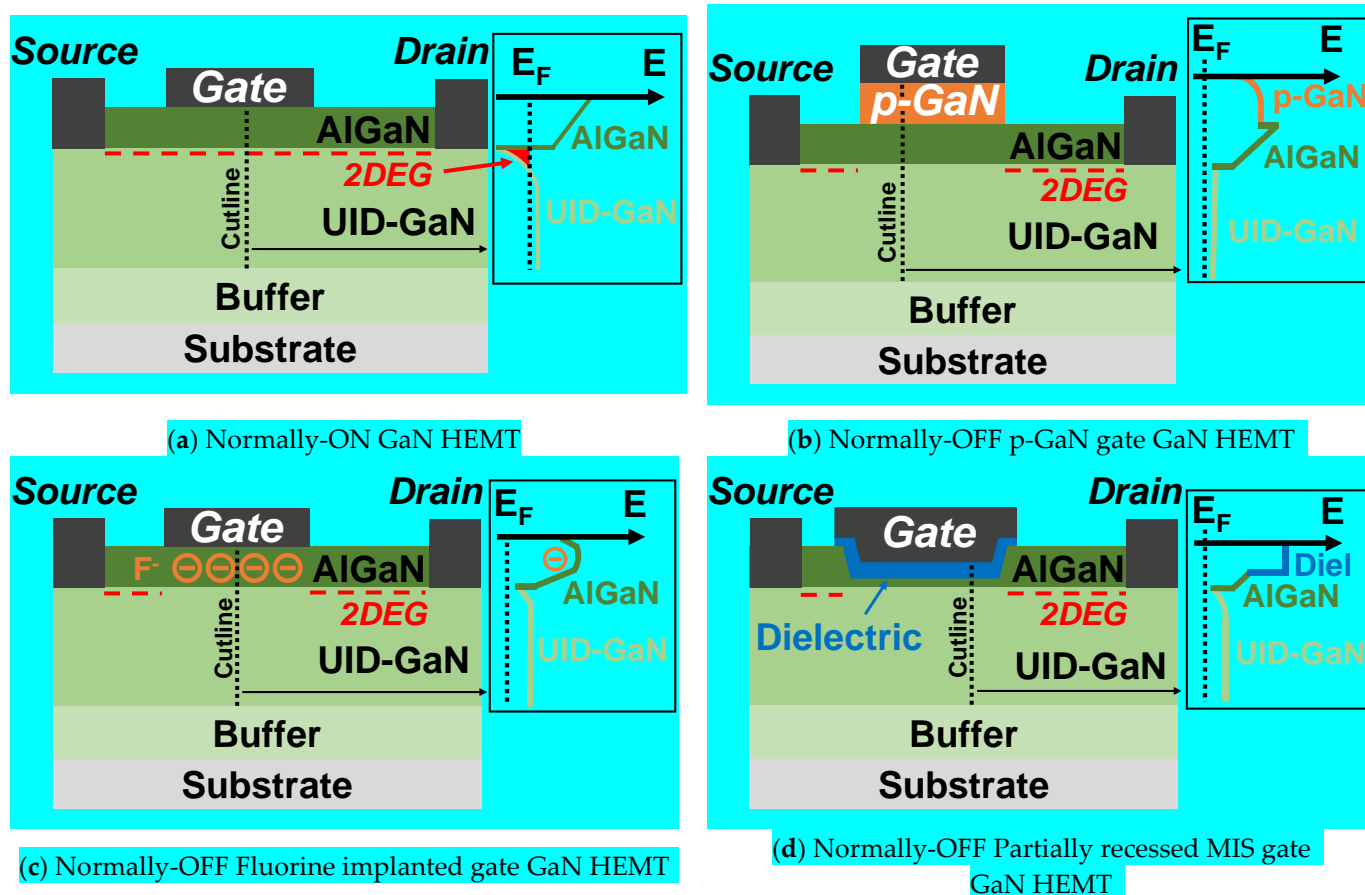
Copyright: © 2022 by the authors. Submitted for possible open access publication under the terms and conditions of the Creative Commons Attribution (CC BY) license (<https://creativecommons.org/licenses/by/4.0/>).

1. Introduction

The major challenge of power electronics today is dealing with the need for high conversion efficiency and reliability, and at the same time, the constant pursuit of cost and size reductions, with low environmental impacts. Replacing power devices made of Silicon semiconductor material by power devices made of wide bandgap semiconductor materials such as Gallium Nitride (GaN) allow to reach smaller size, cost reduction and higher switching speed at the power system level, thanks to better GaN intrinsic physical parameters. Noticeably, the AlGaN/GaN heterojunction allows to get a high mobile electron layer and to design GaN FETs such as HEMTs which offers high power density, and high switching frequency.

GaN transistors are faster and smaller than silicon MOSFETs thus leading to increased power density in chargers and adapters as well as high efficiency due to reduced conduction and switching losses. At the moment, the market of GaN power transistors with a positive threshold voltage (V_{TH}), or Normally-OFF, is completely dominated by p-GaN gate architecture (proposed by EPC, GaN Systems, Panasonic for instance). Typical Mg concentrations used in p-type GaN layer are around $1 \times 10^{19} \text{ cm}^{-3}$ [1], the Mg saturation being as high as $8.9 \times 10^{19} \text{ cm}^{-3}$ [2]. However, since acceptor levels from Mg are in the range of 150 to 200mV from the valence band, ionization of Mg is limited to a fraction of its concentration. However, the p-GaN gate architecture has intrinsic limits with respect to

its silicon power MOSFET counterparts. Because of the p-GaN gate topology, V_{TH} is generally limited to 1.5V and the typical recommended gate drive is in the range of 0V to 6V or -3V to 6V for high current hard switching applications. Metal-insulator-semiconductor Gate (MIS Gate) GaN transistors could give greater freedom in terms of gate driving voltage as a result of both increased threshold voltage and larger range in gate voltage swing. Alongside power applications, MIS Gate GaN transistors can be implemented for RF [3], gas sensing [4] and LiDAR [5]. Considering the benefits of a MIS Gate, the fully recessed MIS (Metal Insulator Semiconductor) gate stack has gained increasing interest during the last few years for the development of Normally-OFF lateral [6], pseudo-vertical [7] and vertical GaN on Si [8] power transistors. This structure is described in the literature by different names such as MOS-HEMT and MIS-FET which are also used to describe partially recessed MIS gates that allow to obtain a Normally-OFF transistor as well. In order to specifically describe the fully recessed MIS gate GaN HEMT, we chose to name it by MOS-channel-HEMT or MOSc-HEMT. Combining the benefits of a MIS gate, its interest comes from the fact that it allows to have a device with a positive threshold voltage by cutting the 2-DEG, low gate leakage current and high gate voltage swing. The MOSc-HEMT also enables to have a more stable V_{TH} than partially recessed MIS gate since the latter suffers from etching thickness variability affecting the V_{TH} [9]. The mentioned topologies as well such as the fluorine implanted gate and the cascode configuration are represented in Figure 1.



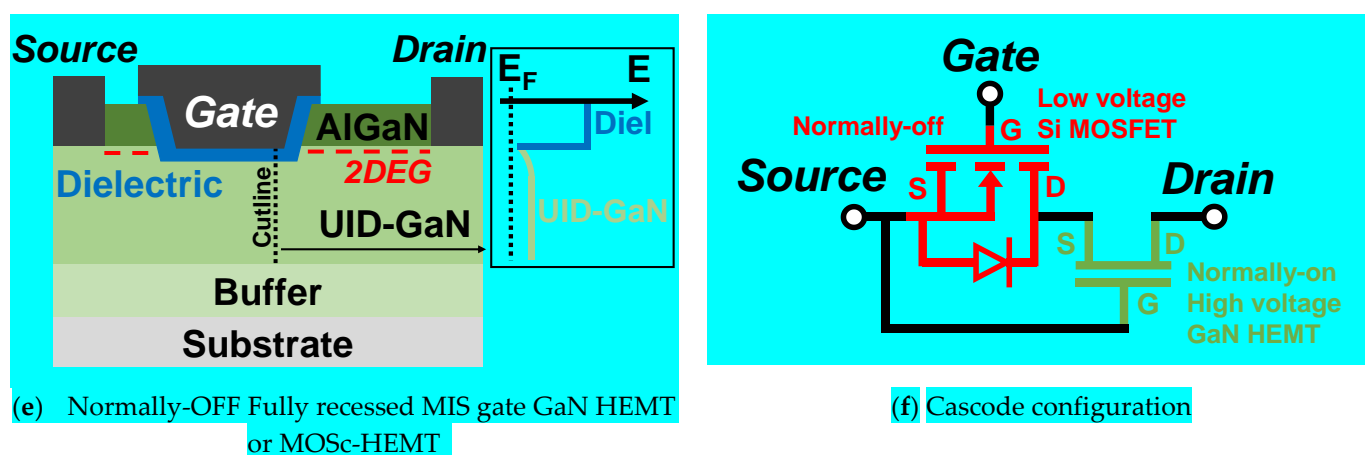


Figure 1. Structure for (a) Normally-ON GaN HEMT and different topologies of Normally-ON GaN HEMTs : (b) p-GaN gate; (c) Fluorine implanted gate; (d) Partially recessed MIS gate; (e) Fully recessed MIS gate or MOSc-HEMT; (f) Cascode configuration (schematic inspired by [10]). Energy band diagrams are represented alongside the structures.

To get the full benefits of the fully recessed MIS gate, it is required to optimize the insulator-semiconductor interface in order to achieve good mobility and low interface trapping states. It is equally essential to tune the insulator properties in view of limiting or controlling its charge. For this reason, several process steps have been studied showing both the impact of AlGaN/GaN recess, cleaning, and dielectric deposition. The different defects at the MIS gate are represented in Figure 2.

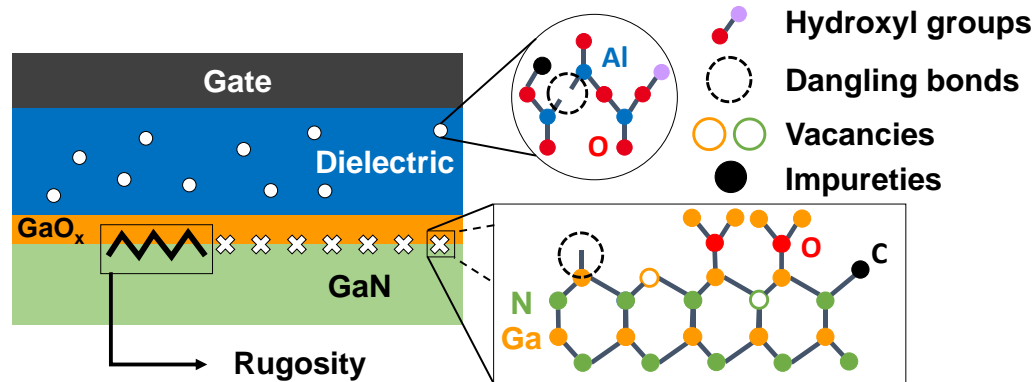


Figure 2. Different types of defects and impurities effectively or hypothetically encountered with fully recessed MIS gate.

Overall, these studies have been carried on either transistors or simple planar capacitors. In the case of transistors, parameters such as V_{TH} , its hysteresis (ΔV_{TH}) and channel mobility can be measured. But for simple planar capacitors, flat band voltage (V_{FB}), its hysteresis (ΔV_{FB}) and density of interface states (D_{it}) are usually studied to evaluate the properties of the dielectric/GaN interface. If the correspondence between results from transistors and planar capacitors can be established, with deeper recess depth, the impact of sidewalls is no longer negligible and needs to be taken into account. Moreover, planar capacitors will have an intentional n-doping in order to provide free carriers for positive voltage swing of C-V measurements, while transistors will have an unintentional doped (UID) GaN layer. Alongside electrical characterization, physical parameters such as roughness, presence of impurities and defects, and oxidation have been measured using different characterization techniques as AFM, XPS/HAXPES and ToF-SIMS. Studying the physical parameters allows to better understand the critical dielectric/GaN interface.

Hence, combining both electrical and physical characterization has been proven important to better investigate the MIS gate and improve it.

2. Manufacturing processes from gate recess to surface preparation

2.1 Gate recess by dry plasma etching

Etching is necessary to achieve a fully recessed gate structure in order to remove the passivation layers, the AlGaN barrier layer and a part of the GaN channel.

2.1.1. Reactive ion etching ICP-RIE

Reactive ion etching (RIE) is a form of dry plasma etching involving a mixture of different elements:

- Reactive and nonreactive ions,
- Reactive neutral species,
- Passivating species,
- Electrons,
- Photons.

The positively charged ions are guided towards the wafer surface through an applied negative bias on the wafer and their acceleration is normal to the wafer surface. Alongside the neutral species present in the plasma, the positive ions work in unison to etch the wafer surface.

For wide bandgap semiconductors, the application of high-density plasma in etching processes such as electron cyclotron resonance (ECR), inductively coupled plasma (ICP), and magnetron RIE was proven to achieve better etching characteristics than simple RIE. The reason for this enhancement can be explained by the higher plasma density, which is typically two orders of magnitude higher than RIE (10^{11} – 10^{12} cm⁻³ against 10^9 – 10^{10} cm⁻³). This increased plasma density leads to a higher efficiency in breaking bonds for these strongly bonded semiconductors and facilitates the removal by sputtering of etching by-products formed on the surface [11].

The use of inductively coupled plasma (ICP) reactors allows to control separately the plasma density (chemical part of the etching, controlled with inductance power) and the bombardment energy (physical part of the etching, controlled with bias voltage); unlike capacitance coupled plasma (CCP) reactors where the plasma density and bombardment energy are controlled together.

GaN is usually etched using fluorine-based or chlorine-based plasmas. ICP-RIE etching of GaN using these plasmas cannot be purely chemical at room temperature because of the formation of nonvolatile etching byproducts such as GaF_x (T_{eb}=1000°C) with fluorine-based chemistries (e.g. SF₆) or AlCl₃ (T_{eb}=183°C) and GaCl₃ (T_{eb}=201°C) with chlorine-based chemistries (e.g. Cl₂) [11]. Therefore, the physical bombardment should be sufficiently strong to remove these byproducts and to expose the surfaces for further etching, for instance using Ar or N₂ in combination with SF₆ [12] or Ar in combination with Cl₂ [13]. Addition of noble gases and energetic-ion sputtering in ICP also improves the etching both by initially breaking the stable Ga-N bond and by preferentially sputtering the nitrogen atoms, which results in a Ga-rich GaN surface [14]. XPS measurements of the GaN surfaces etched by SF₆ and Cl₂ indicate respectively the presence of F and Cl on the etched GaN surface [15]. Worse on-state characteristics were observed with SF₆ etching, assumed to be due to deterioration of the negative V_{TH} with F [15]. Moreover, since Cl based by-products are more volatile, the etching process is faster. Therefore, etching of GaN using chlorine-based plasma is preferred to fluorine-based plasma.

Gallium oxide can be present at the GaN surface or may form during the etching process since the etching chamber can contain small amounts of oxygen (chamber walls, mask layers on the wafer). BCl₃ is helpful for gallium oxide removal as BCl₂⁺ ions dissociated from BCl₃ are good Lewis acids with strong oxide affinity, leading to the formation

of BCl_xO_y (g) [16]. Therefore, etching of GaN is usually performed using Cl_2 and BCl_3 chlorine-based plasma. By increasing the bias power, the physical component of the etch process is enhanced, as confirmed by linear correlation between ICP bias power variation and AlGaIn, GaN and AlN etch rate [17].

The use of other chemicals such as SiCl_4 have been reported to tune the profile shape, for instance SiCl_4 passivates the sidewalls by formation of SiO_x and SiN_x , leading to a more vertical profile [18].

Continuous dry etching on GaN has fast etch rates, but the surface damage as shown in **Figure 3** (composition/roughness), the high variability and the non-uniformities at wafer and die level are, at present, the three main shortcomings [19,20].

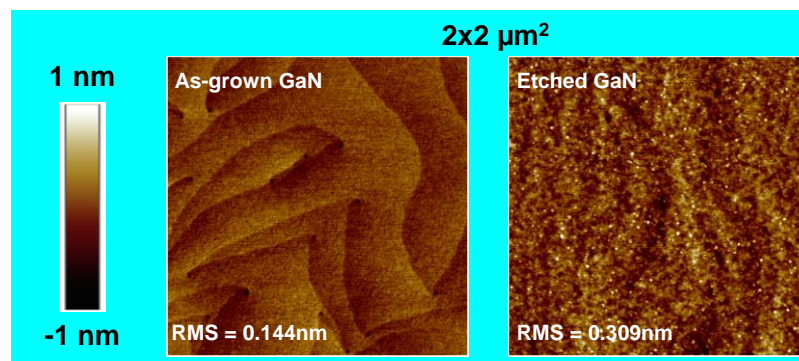


Figure 3: GaN surface before and after etching observed by AFM. The etching process is similar to the process used in [21]

2.1.2 Plasma induced damage

The device's performance can be seriously degraded due to the creation of plasma-induced damage, which occurs as a result of ion bombardment and exposure to ultraviolet (UV) photons during plasma assisted etching. Plasma-induced damage includes the following defects:

1. Lattice defects generated from energetic ions. These defects typically exhibit deep level states behavior and thus produce compensation, trapping or recombination in the material. Due to channeling of the low energy ions that strike the sample, and rapid diffusion of the defects created, the effects can be measured as deep as 1000 \AA from the surface, even though the projected range of the ions is only $<10 \text{ \AA}$ [22].
2. Atomic hydrogen unintentional passivation of dopants. The hydrogen may be a specific component of the plasma chemistry, or may be unintentionally present from residual water vapor in the chamber or from sources such as photoresist mask erosion. The effect of the hydrogen deactivation of the dopants is a strong function of substrate temperature, but may occur to depths of several thousand angstroms [22].
3. Polymeric film deposition through plasma chemistries involving CH_x species, or through reaction of photoresist masks with Cl_2 -based plasma [22].
4. Nonstoichiometric induced surfaces by selective removal of specific lattice elements. This can occur because of strong differences in the volatility of the respective etch products, leading to enrichment of the less volatile species, or by preferential sputtering of the lighter lattice element if there is a strong physical component to the etch mechanism. Typical depths of this nonstoichiometry are $<100 \text{ \AA}$ [22].

In the case of AlGaIn/GaN etching, various studies have shown that higher ICP bias power create ions with higher energy, ultimately leading to stronger ion bombardment damage [23], several GaN material damage or degradation of the devices performance [20,23–29]. The characterizations methods for dry plasma induced damage in AlGaIn/GaN materials and devices are reported in **Table 1**.

Table 1. Characterizations methods for dry plasma induced damage in AlGaIn/GaN materials or degradation of devices performances.

Characterization technique	Material damage or degradation of the device performance	Ref.
AFM	Roughness of AlGaIn surface	[30,31]
Photoluminescence	Increase of photoluminescence intensity ratio of YL/BE	[24]
Cathodoluminescence	Degradation of the AlGaIn Near Band Edge signal intensity	[31]
Depth Resolved Cathodoluminescence Spectroscopy (DRCLS)	V_N (@ $E_C - 0.9\text{eV}$) and C defects in the p-GaN layer	[32]
Electrochemical Impedance Spectroscopy	Decrease in built-in potential (V_{bi}) at the nGaIn/electrolyte Interface	[25,33]
Sheet resistance measurement (R_{sheet}) with 4-probe equipment on GaN/AlN/AlGaIn/GaN samples	Increase of 2DEG sheet resistance	[20,24,34–36]
Schottky diodes	Decrease of Schottky barrier height Φ_B	[25]
MOS capacitors or transistors	Increase of interface state density (D_{it})	[26–28,30,37]
	Lower electron mobility	[27,37]
	Increase of leakage current	[26]
	Lower threshold voltage	[23,37]

Reported electrical damage depth ranges from >10–20 nm [20,25] to 40 nm [38] or 50–60 nm [22,25]. From the AES electron spectrum of oxygen profile, surface damage was limited to the top few hundred angstroms [39].

One proposed explanation for the degradation of device performance is the introduction of donor levels, such as V_N , caused by dry-etching. These donor levels results in a n-GaN surface [32], which may contribute to the low V_{TH} since applying negative gate voltages is necessary to deplete the n-GaN surface donor layer and cut off the channel. As a matter of fact, under threshold conditions, some of these n-type defects become ionized and depleted, resulting the generation of positive ionized space charges. Therefore, the key factor for achieving normally-OFF operation in a fully dry-recessed MIS gate HEMT is the removal or recovery of the damaged layer (i.e. providing sufficient nitrogen to eliminate the V_N)[29].

Among the different approaches proposed to overcome the plasma induced damage issues are:

1. Reduction or elimination of the source of damage through use of etching methods without plasma or with low ICP bias power.
2. Recovery of the damaged layer.
3. Removal of the damaged layer.

The use of etching methods without plasma is a way to avoid damage. Photo-electrochemical (PEC) etching through photo-assisted anodic oxidation is interesting for nitride semiconductors since the high thermal and chemical stability hinders the use of typical wet chemical etching. The necessary amount of photo-induced holes is regulated by choosing the relevant wavelength λ and anodic bias [40]. The holes are generated at the anode present at the GaN/electrolyte interface, specifically where electrons are given off to the outside circuit. These holes then break down GaN into Ga^{3+} ions. The latter reacts with the electrolyte and results in the formation of Ga_2O_3 which dissolves in acid or base (H_3PO_4 and KOH [41] or $\text{H}_2\text{SO}_4/\text{H}_3\text{PO}_4$ mixture [42]). Finally, the etching depth is proportional to the total etching current [43].

The use of etching methods with low bias plasma is another way to reduce the damage.

In that matter, Atomic Layer Etching (ALE) is an interesting solution to reduce the dry-etching surface damage, which mitigates device performance and electron mobility,

and to accurately control the etching depth. ALE, with low etching rates, can be used directly to remove the AlGaIn/GaN layers (full ALE) or after conventional ICP-RIE etching with higher etching rate. The combination of ICP-RIE with ALE was reported to reduce etching damage, evaluated by the reduction of the sheet resistance R_{sheet} in **Figure 4**.

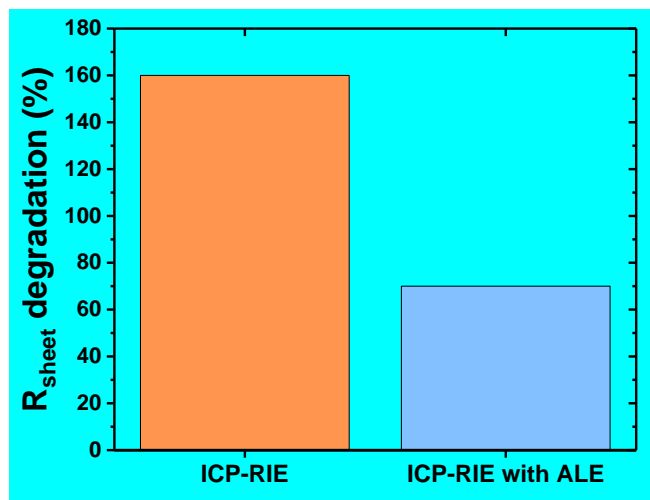


Figure 4: R_{sheet} measurements of the 2DEG after ICP-RIE etching or ICP-RIE with ALE etching [35]

However, it has also been reported that UV photon damage in ALE was larger than in RIE owing to the longer plasma irradiation time [31]. It has been found that the ALE photon-induced damage can be mitigated by a post etch anneal process at temperatures which are compatible with the overall thermal budget of a GaN power transistor process flow [44].

In a similar approach and more recently, multistep etching with decreasing bias and post-etching anneal has been proposed to reduce the damage [18,45].

Also, a neutral beam etching (NBE) system using the neutralization of negative ions has been proposed by Lin and co-workers in order to eliminate UV photon irradiation [46].

2.1.3. GaN atomic layer etching (ALE) or digital etching

The ALE mechanism consists of two sequential steps: surface modification (reaction A) and the removal of the modified surface (reaction B). The modification step creates a thin modified layer on surface with a specific thickness, which is easier to remove than the unmodified material. This modified layer has a distinct change in physical structure and/or in composition with a defined gradient.

The surface modification (reaction A) can occur through:

1. Chemisorption of species on the surface, which weakens the material bonds underneath (e.g. chlorination of GaN by Cl_2),
2. Deposition of a reactive layer on the surface,
3. Conversion of first layers into another material (e.g. oxidation of GaN),
4. Selective extraction of a specific species.

During the removal step (reaction B), the modified layer is removed while maintaining the integrity of the underlying substrate. This step allows the surface to be “reset” to a pristine or almost pristine state for the subsequent ALE cycle [20]. The ALE mechanism is represented in **Figure 5**:

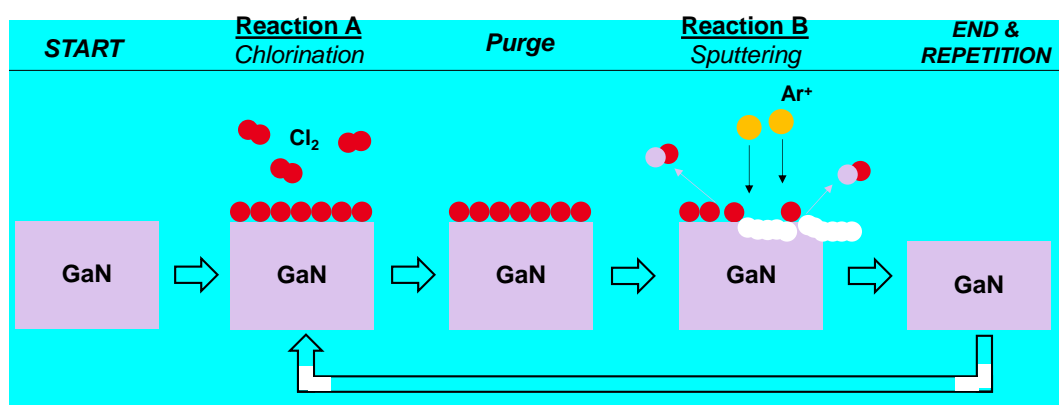


Figure 5: General concept of ALE with reaction A (chlorination of the GaN surface) and reaction B (removal of the modified surface with Ar plasma)

III-V and III-N materials are usually etched by directional ALE using a combination of chlorination and particle bombardment [20]. Chlorine mostly reacts with the surface and metallic Ga atoms to form Ga chlorides [14]. The removal of the chlorinated layer has been investigated by the bombardment of Ar or He ions [35,36]. Several teams have reported on Cl₂/Ar based ALE for GaN etching, achieving etch rates from 0.13 to 0.50 nm/cycle [35,36,44,47–50] and surfaces as smooth as the as-grown sample. The presumed etching by-products are GaCl₃(g) and N₂(g) [49].

Cl₂/Ar ALE parameters such as DC bias voltage during the Ar step, duration of each step, pressure during each step and gas ratio can be optimized in order to etch in the “ALE window” where there is no background etching during reaction A and only the modified layer by reaction A is removed by reaction B (no additional sputtering) [44,48,49]. A 2D fluid model is useful to determine the flux of reactive species, radicals and ions included, which arrive at the wafer surface. This flux can be calculated as a function of chlorine content, gas pressure and RF power, showing a strong correlation between the chemical nature of the etching process and the rise in atomic chlorine flux[51]. Ar bombardment leaves Ga atoms with dangling bonds, leading for a low energy bombardment of 100eV to a ~25Å amorphous layer enriched in Ga [52], for 400eV to a Ga-rich surface layer [53,54], for 1keV to Ga nanodroplets [55], for a high-energy bombardment of 2.5 keV to a metallic Ga layer [53,54]. Simultaneously, a portion of nitrogen is moved to interstitial position, forming split-interstitial defects [54]. This Ga-rich surface was associated with lower Ga 3d binding energy [55], increase in the downward band bending (nitrogen vacancies act as donors) and pinning of the surface Fermi level closer to the conduction band [56].

An alternative to chlorination for the surface modification step is the use of a bromine-based chemistry (HBr), allowing to reduce the Ar plasma power during the bombardment step [44].

An alternative to particle bombardment for the removal step is the thermal desorption of Ga chlorides at temperatures higher than 223 K [14].

Another ALE of III-V and III-N materials is a combination of oxidation of Al-GaN/GaN by oxygen based plasmas or by wet chemistries followed by removal of oxide by chlorine based plasma etching or wet etching, also called digital etching. This technique can also apply to remove unwanted native oxide/contamination, disordered gallium oxide/aluminum oxide residue. The oxidation step can be achieved by exposure to a low power O₂ plasma [19,57–63], to N₂O plasma [64] or to wet solutions such as H₂SO₄/H₂O₂ [65]. Increased GaN surface roughness has been reported, attributed to the locally improved oxidation around the dislocations. The pinholes, which are likely caused by dislocations, were significantly enlarged as the recess depth increases [66]. Removal of the oxide layer can be achieved using a low-power BCl₃ oxide etch step [67–69], which resembles a self-limiting process, due to the fact that BCl₃ etches the oxidized GaN layer much faster

than unoxidized regions. This difference in etch rate is explained by B_xCl_y deposited layer on unoxidized GaN. After etching, this deposited layer can be easily removed by stripping process [69]. Removal of the oxide layer can also be achieved by submerging the wafer into a wet HCl acid bath [19,20,57–59,61,64,65,70]. Thanks to the high oxidation selectivity ratio of GaN and AlGaN [71–74], TMAH and KOH are reported for selective etching of oxidized AlGaN and AlN while GaN plays the role of etch stop layer [73–75]. GaN cap layer can be used as a recess mask [71].

In conclusion, etching of AlGaN/GaN is mandatory in order to obtain a recessed gate architecture. However, traditional ICP-RIE processes create damage, which can alter the electrical performance. The following challenges arise:

1. Proper characterization of the damage, correlation with electrical damage (which depends on the target device),
2. Developments of damage-free or reduced damage etching processes, compatible with an industrial process (wafer size, throughput),
3. Process integration and choice of mask that enable the use of damage-free or reduced damage etching processes,
4. Adapted stripping that removes masks and etching residues.

Cyclic processes such as ALE show good repeatability and etch depth control with lower electrical degradation than ICP-RIE processes, enabling to reduce the damage. Other approaches include recovery or removal of the damaged layer, which can be performed by various GaN surface treatments.

2.2. Cleaning or surface preparation by wet, thermal or plasma treatments

The surfaces to clean are the GaN gate bottom, which is a polar (0001) Ga-face c-plane and the gate cavity AlGaN and GaN sidewalls. If the gate cavity had 90° sidewall angles, they could be non-polar m-planes and a-planes, depending on the orientation, due to the Wurtzite GaN crystal structure (hexagonal symmetry).

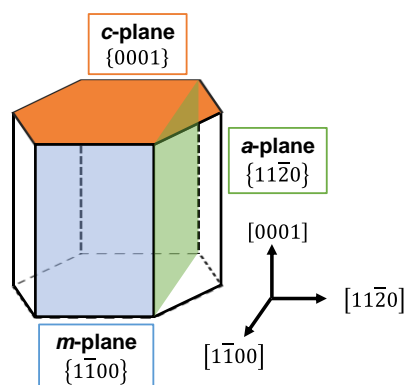


Figure 6. Different planes from the Wurtzite GaN crystal structure (hexagonal symmetry).

The contamination layer of air-exposed GaN is usually $\sim 2\text{--}5\text{nm}$ thick. About half of this contamination consists of transparent inorganic and organic species. The rest is presumed to be native oxide [76]. Wurtzite GaN surfaces are very active towards the adsorption of oxygen. The presence of dangling bonds at the GaN surface makes the surface reactive to a wide range of impurities, leading to higher impurity concentration on GaN than on Si [77].

GaN surface preparation aims at:

- Reducing the surface contamination (particulate, metallic, and chemical: native oxides, carbon and other),
- Not damaging the crystal structure nor introducing additional defect states,
- Removing the etch-induced damage,
- Smoothing the GaN surface,

- Improving the nucleation of the dielectric layer (for instance Atomic Layer Deposited or ALD Al₂O₃). 333
334

Ex-situ cleaning includes solvents, various acid and bases, as well as UV/O₃. In-situ cleaning includes room temperature or high temperature plasma, sputtering and vacuum or gas annealing [76]. A summary of all the treatments discussed in this paper can be found in **Table 2**. 335
336
337
338

Table 2: GaN surface treatments and their impact on contamination removal, etch-induced damage removal. The abbreviation “Y” and “N” are for “Yes” and “No” respectively. 339
340

Surface treatment	Anisotropic etching (Y/N)	Oxide removal (Y/N)	Carbon removal (Y/N)	Dry etching damage removal (Y/N)	Impact on roughness and incorporation of impurities	Impact on device
TMAH	Y [78–80]			Y (sidewall [81]) N (planar [26])	Removal of F [82] Removal of plasma damage [83]	Positive V _{TH} shift [84] Improved mobility [83]
KOH	Y [85,86]					
NaOH				Y [37]		Positive V _{TH} shift [37]
NH ₄ OH		Y [21,87–91]	Y [90] N [87,88,92]	Y (100°C [23])		Positive V _{TH} shift [23,91]
HCl		Y [21,89,93–95]	N [89,96,97]	Y (70°C [98])	Incorporation of Cl [21,94,99] Detrimental impact on ALD nucleation [100]	Large hysteresis [100]
HF		Y [97,101]	Y [102] N [96,97]		Incorporation of F [97]	
H ₂ O ₂ :H ₂ SO ₄		Y [97] N [96]	Y [96,97,102]		Smoothing [97,102]	Reduction of hysteresis [100,102]
H ₃ PO ₄	Y [21,103]	Y [21]	Y [21]	Y [21]	Incorporation of P [21,103]	
(NH ₄) ₂ S		Y [21]	N [97,102]		Incorporation of S [104]	Reduction of hysteresis [105]
UV/O ₃		N [106]	Y [107]			
O ₂ plasma			Y [99]		Removal of Cl [99]	
N ₂ annealing				Y [38,45]	Removal of Cl [99]	
NH ₃ annealing		Y [108,109]				
H ₂ S annealing					Incorporation of S [110]	Negative V _{TH} shift [110]
Ar plasma						Reduction of hysteresis [111,112]
NH ₃ plasma		Y [87]	Y [87]			Reduction of hysteresis [113]
N ₂ plasma			Y [88,114,115]	Y [23,24]	Incorporation of N [88,115]	
H ₂ plasma		Y [116]	Y [116]		Formation of Ga droplets [116]	

Various wet cleaning sequences have been reported in the literature. After oxygen removing wet treatments, such as HF, the presence of a Ga-O bonds indicates the presence of a native oxide. It suggests a reoxidation (estimated to 0.5Å) forming a GaO_x layer during surface exposure to ambient air prior to XPS measurement or during wet treatments (HF and/or DI water rinse) [101]. This further confirms the strong oxygen affinity of a clean GaN surface. The presence of a GaO_x layer is problematic, with increased hysteresis and 341
342
343
344
345
346

interface states [117–119]. In-situ $\text{NH}_3/\text{Ar}/\text{N}_2$ plasma sequence has been reported for the removal of the surface native oxide [120] and formation of a nitrated inter-layer (NIL) prior to the gate dielectric deposition as seen in **Figure 7**. This treatment is sometimes labelled as remote plasma pretreatment (RPP). The NH_3 -Ar plasma is used as a cleaning step to remove the native oxide. The subsequent N_2 plasma allows to nitride the surface (Ga dangling bonds passivated and possible V_N compensated), resulting in a NIL on the III-N surface [121,117,122]. Other plasma sequences such as H_2/NH_3 cycles [123], a sequence of NH_3 and N_2 [124] or N_2/H_2 [125] have been reported before ALD of AlN , SiN_x or epitaxy, leading to a decrease in hysteresis, a reduction of the ON resistance but also a decrease in V_TH [124].

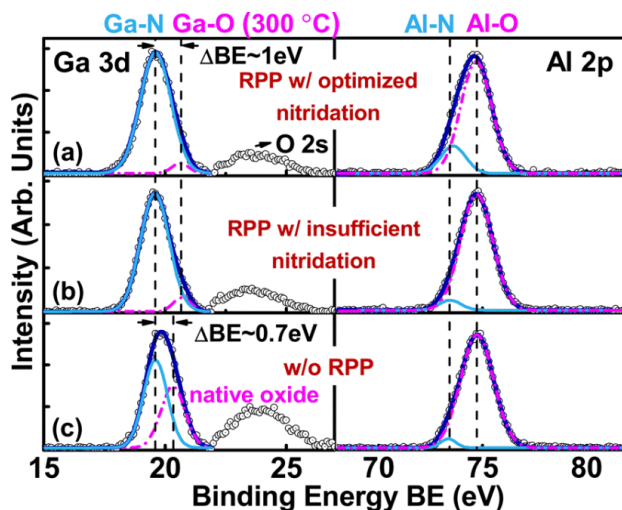


Figure 7. XPS measurements of Ga3d and Al2p spectra from $\text{Al}_2\text{O}_3/\text{GaN}$ interfaces (a) with optimized RPP, (b) with RPP having insufficient nitridation and (c) without RPP (© 2013 IEEE. Reprinted, with permission, from [116])

Thus, it seems that a combination or a sequence of different treatments is the most suitable in order to achieve all the goals of the surface preparation [126]. Also, for a same surface preparation process, the surface states depend on previous processing, such as dry etching conditions, and therefore the surface preparation should be adapted to the specificities of the material and overall process flow. For instance it was found that the Ga oxidation states at $\text{Al}_2\text{O}_3/\text{GaN}$ interface were higher for etched samples than for non-etched samples [91] or that increased trapping occurred for etched GaN [127]. The higher oxidation state when reduced with the appropriate wet cleaning sequences was proven to increase V_TH (**Figure 8**)

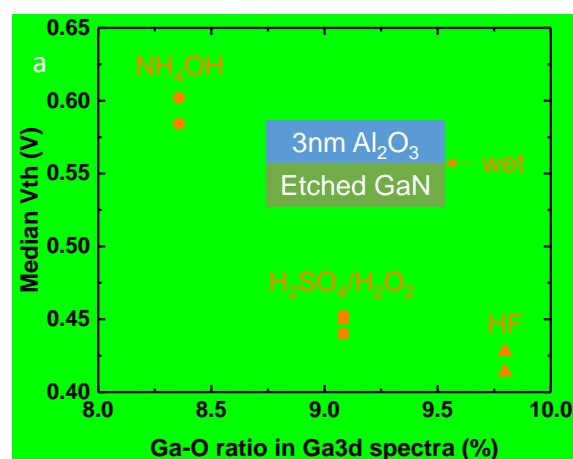


Figure 8. Trend of V_{TH} with gallium oxidation after different wet treatment on etched GaN (from [91])

In addition, as stated in introduction, there is still a limited understanding of the impact of the gate cavity morphology, since most of the studies reported here focus on planar structures formed on c-plane (corresponding to the bottom of the gate). We have seen that anisotropic GaN etchants such as tetramethylammonium hydroxide (TMAH), potassium hydroxide (KOH) or H_3PO_4 impact trench sidewall morphology [78,85,86,128]. For instance TMAH etches any plane of GaN, except for the (0001) c-plane, while it etches m-plane at a considerably lower rate than other semi-polar planes allowing for instance to achieve rough a-plane oriented sidewall (composed of microscopic m-faces) and smooth m-plane oriented ones [78,79]. In the few studies carried out on different non-polar planes, it is clear that GaN crystallographic orientation impacts the effect of surface treatments on electrical characteristics [79,112,129–131] or that sidewall formation has a significant impact on device performance (in comparison with a planar etched structure) [127]. As a consequence, it is crucial to improve the understanding of how the GaN crystal orientation and 3D gate cavity with sidewalls formation impacts recessed gate devices' performance.

Finally, selective area regrowth faces some similar challenges with the deposition of a dielectric in a recessed GaN cavity (such as in MOSc-HEMTs): negative impact of the dry etching [98], exposure to air, difference between trench bottom and sidewalls, incorporation and activation of the Mg dopant. Therefore, similar characterization techniques can be applied to study these impacts [132]. But regrown GaN is still promising to recover dry etching plasma induced damage [133,134], and can be combined with in-situ dielectric deposition which allows an increase in electron mobility (OG-FET device reported in [135]).

3. Interface and dielectric materials

3.1 Interface

Since the growth of a thick native gallium oxide, similar to SiO_2 from Si, is difficult [136], the deposition of a dielectric layer has been necessary to form a MIS gate. However, due to the defective interfacial GaO_x and the lattice mismatch at the dielectric/GaN interface, this interface needs to be controlled to have the desired device properties.

In the case of GaO_x , reducing the low-quality interfacial oxide was presented in the previous section with wet cleaning and plasma treatments, notably with the NIL plasma treatment. This technique is important since as stated before GaO_x is not reduced with HF [101] nor after dielectric deposition such as Al_2O_3 [137]. Another solution is to create a high-quality interfacial gallium oxide. Oxidation by exposing the surface to ozone was found beneficial for AlGaIn/GaN devices with reduced hysteresis [138]. More specifically, oxidation by O_2 plasma combined with a high temperature anneal under N_2 and prior SiN_x deposition by Low-Pressure Chemical Vapor Deposition (LPCVD) was studied [139–141]. The result is a GaON layer formed at the interface between SiN_x and the recessed GaN surface. With the GaON layer, a V_{TH} of 1.15V and a reduced hysteresis of 0.2V is reported [139]. Reduced hole injection under negative stress is also observed, the high valence band offset between GaON and GaN explaining this improvement [140,141]. GaON can also be formed with a N_2O plasma [142–144], reducing the damage from the LPCVD SiN_x deposition process [143] and increasing electron mobility [144]. With a non-recessed gate structure, an AlGaON layer formed by controlled oxidation with N_2O plasma through a thin Al_2O_3 layer was reported in [145,146]. An increased V_{TH} was observed with a small hysteresis correlated to the oxidation step [145].

A thin interfacial AlN can be directly deposited before the dielectric to improve the interface quality due to its lower lattice mismatch with GaN with respect to Al_2O_3 [147]. Moreover, AlN is known to form a passive oxide layer, when exposed to air. For this rea-

son, AlN deposition is typically followed by in-situ dielectric deposition without air exposure. When applied on both GaN's c-plane (polar surface) and m-plane (non-polar surface) before ALD Al₂O₃, AlN reduces the V_{FB} hysteresis and the interface states, especially at the non-polar surface [130]. Specifically for MOSc-HEMT, a reduction of V_{TH} hysteresis from 800mV to 65mV is obtained with a 2nm PEALD AlN interfacial layer at the Al₂O₃/GaN interface, as well as a lower density of interface states [148]. By combining the NIL process and the AlN deposition, the improvement in terms of hysteresis is similar but a lower density of interface states is observed and a greater separation between defects on Al₂O₃ and GaN is obtained [119,149]. With an AlSiO dielectric, AlN improves the electron mobility by confining the electrons at the interface [150] and allows to reduce Ga diffusion into the dielectric after high temperature Post-Deposition Annealing (PDA) at 950°C [151].

In conclusion, two ways of treating the interfacial GaO_x are possible; either reducing it or improving/growing the interfacial oxide with fewer defects. Specific AlN interfacial layer deposition before thicker dielectric deposition leads to increased mobility, lower hysteresis and lower density of states. Since the direct deposition of oxides on GaN maintains the interfacial GaO_x, combining its removal with an AlN layer represents a promising solution to keep a low oxidation state at the interface, improve electron mobility and reduce V_{TH} hysteresis.

3.2 Dielectric

Another essential aspect of the MIS gate is its dielectric. The considered properties are [152]:

- Larger band gap than GaN in another to have a conduction offset higher than 1 eV,
- Layer without grain boundaries,
- High relative permittivity and high breakdown voltage.

A summary of dielectrics, their band lineup with GaN and their dielectric constant are represented in Figure 9. As the high-κ dielectric band gap tends to decrease with the dielectric constant, there is a limitation in the choice of candidates. Frequently used dielectrics are SiO₂, SiN_x and Al₂O₃. Annealing after deposition or after metallization is equally important to improve the dielectric/GaN stack.

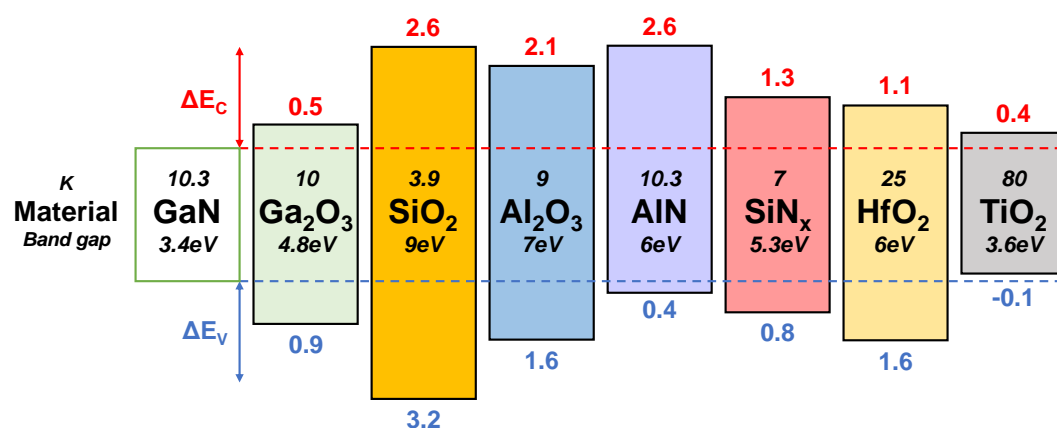


Figure 9. Band lineups of different dielectrics with GaN alongside their respective dielectric constant (Refs [153–156]).

SiO₂ has a high gap (~9 eV) but a low relative permittivity (~3.9) [157,158]. Its large gap strongly reduces leakage current, and its thermal stability allows the use of high thermal budgets (>800°C). However, Ga diffusion into SiO₂ can lead to increased leakage current as well as reduced breakdown voltage [132]. A negative shift of V_{FB} at high PDA temperature (800°C) was also reported and attributed to the formation of V_o after hydrogen reduction with interfacial GaO_x [133].

SiN_x has a lower gap (~5.5 eV) and a higher relative permittivity (~7.5) [157,158]. The V_N passivation with SiN_x leads to a lower reported density of interface states [134,135]. However, because of its small gap, gate leakage may be in certain cases too high [136].

Al₂O₃ has a high gap (~7 eV) and relative permittivity (8–10) [157,158]. Regarding the interface, D_{it} values ranging from 10¹¹ to 10¹³ cm⁻²·eV⁻¹ are found in the literature depending on the deposition and treatment before or after Al₂O₃ formation [159–161]. However, amorphous Al₂O₃ has a lower thermal stability than SiN_x and SiO₂. Crystallization typically occurs at about 800°C [160] on as-grown GaN and a beginning of crystallization can be observed at 600°C on etched GaN [162]. When PDA is applied, usually between 400°C and 800°C, a general increase of V_{TH}/V_{FB} is reported [163–166], V_{TH} hysteresis is reduced [167] and electron mobility is increased [137,163,166]. These improvements can be related to the reduction of positive charges in both GaO_x [152,166] and Al₂O₃ [165], or to the reduction of interface states [164,167,168].

With the respective limitation of commonly used dielectrics, one approach is to develop ternary alloys to benefit from their specific properties.

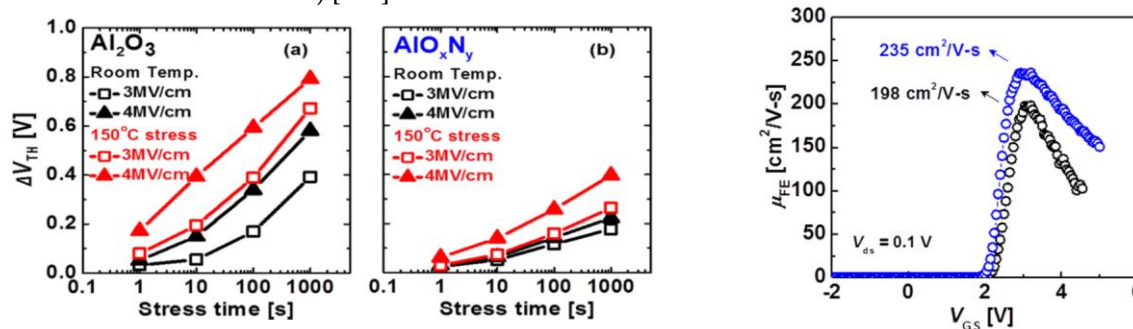
3.2.1 Al₂O₃ and AlN alloys for improved thermal stability and lower electron trapping: AlON

AlON is an example of such an alloy, consisting of a mixture between Al₂O₃ and AlN, and having many advantages compared to Al₂O₃ and AlN. It can be deposited by different techniques:

- Sputtering of an Al source with a flow of O₂ and N₂ [169],
- Nitriding ALD Al₂O₃ with N₂ plasma [170,171],
- ALD with Trimethylaluminium (TMA) and N₂/O₂ precursors [172],
- ALD nanolaminates of Al₂O₃ and AlN [173,174],
- Oxidation of ALD AlN with O₃ [175,176].

In terms of advantages, the introduction of nitrogen into the Al₂O₃ matrix reduces current leakage by both passivating V_O defects [177] and increasing the electron barrier height between AlON and GaN [171], although AlON's band gap was reported to be smaller than Al₂O₃ [169,175]. The passivation of these defects could explain the reduction in hysteresis and electron injection reported for AlON in the literature [169,171,173,175,177,178]. Nozaki and co-workers indeed reported a reduction in electron injection with increasing nitrogen concentration while Kang and co-workers reported a reduced V_{TH} instability under positive bias stress (Figure 10.a). Furthermore, the presence of nitrogen induces the presence of negative fixed charges allowing V_{FB} to increase [170,173]. With a fully recessed MIS gate HEMT, a similar V_{TH} of ~2.25 V is found for AlON and Al₂O₃ [171]. According to an ab-initio study by Choi and co-workers, the introduction of nitrogen into crystalline Al₂O₃ induces negative fixed charges for n-type doped GaN [179]. However, according to Guo and co-workers, these nitrogen defects are absent in the amorphous Al₂O₃ gap. Thus the negative charges introduced by these defects are also absent [180].

Regarding the interface, AlON reduces interface states mostly for defect energy level from the conduction band or E_C-E_T higher than 0.35 eV, possibly through the reduction of GaO_x at the interface [169,171,173,178]. With a better interface than Al₂O₃/GaN, Field Effect mobility (μ_{FE}) for MOSc-HEMT with AlON increases by ~19% up to 235 cm²·V⁻¹·s⁻¹ (Figure 10.b) [171].



(a)

(b)

Figure 10. For both Al₂O₃ and AlON deposited in a MOSc-HEMT : (a) V_{TH} shift with positive bias stress at room temperature and at 150°C (b) field effect mobility extracted for a V_{DS} at 0.1V [171](© IOP Publishing. Reproduced with permission. All rights reserved).

However, while AlON has better immunity to electron injection, Hosoi and co-workers [181] reported a hole injection which could be problematic in the case of negative stress. These hole traps would be explained by the existence of defects in the N2p orbital near the AlON's valence band [182].

With the incorporation of nitrogen, AlON also benefits from a higher thermal stability up to 800°C in PDA [169]. As such, the high temperature PDA or Post-Metallization Annealing (PMA) allows to increase the V_{FB} and reduce its hysteresis [170,178]. However, few studies reported the impact of different PDA temperatures.

3.2.2. Al₂O₃ and SiO₂ alloys for improved thermal stability and lower electron trapping: AlSiO

As well as AlON, AlSiO is a ternary alloy of Al₂O₃ and SiO₂, combining the higher relative permittivity of Al₂O₃ (~9) with the higher band gap of SiO₂ (~9eV). It can be deposited by different techniques:

- Sputtering a silicon doped aluminum target [183,184],
- MOCVD [185–187],
- ALD nanolaminates of Al₂O₃ and SiO₂ [151,188–191].

By increasing the silicon concentration, the conduction band offset between AlSiO and GaN increases, reducing the leakage current [188,189]. The incorporation of silicon reduces the hysteresis [184–187] with Sayed and co-workers reporting a reduction in hysteresis for MOCVD AlSiO with increasing silicon percentage up to 46% [187]. However, they also describes a negative hysteresis for a percentage equal to 76%, possibly originating from mobile charges. Concerning V_{FB} , the impact of silicon content differs in the literature. Komatsu and co-workers reported an increase in V_{FB} for a silicon content of 29% [184], Gutpa and co-workers reported a reduction in V_{FB} [186], and Kikuta and co-workers reported a small correlation between V_{FB} and silicon content [188]. These differences could be due to the introduction of either positive or negative charges, or the different deposition methods used. More recently, Smith and co-workers reported an increase of V_{TH} with increasing Si content, this effect magnified with AlN interfacial layer [150]. Furthermore, by ab-initio simulation, Chokawa and co-workers described a lower formation energy of V_O defects when the silicon concentration increases [192]. Unlike V_O defects that would be electrically active (V_O^{2+}) in Al₂O₃ [193], these vacancies surrounded by silicon are electrically inactive. However, the transition energy (2+/0) for V_O defects is approximately at 2.8~3.5 eV from the alumina's valence band (1.9~2.6 eV from GaN's valence band if the valence band off-set is considered to be 0.9 eV) [193,194]. In the case of n-doped and UID GaN, V_O defects would already have a neutral charge state. For p-doped GaN, this defect can be a source of hole leakage [194].

Finally, regarding the interface between AlSiO and GaN (0001) (or Ga-Face), the absence of dangling bonds is observed by ab-initio simulation and explained by oxygen migration from the dielectric to the interface [195]. Thus, a low D_{it} is observed when compared to Al₂O₃/GaN (0001) interface [185,186]. In the case of p-MOSFET, the extracted μ_{FE} was found to be around 27.7–36.2 cm².V⁻¹.s⁻¹ [191]. Similar to AlON, the incorporation of Si increases the thermal stability with respect to Al₂O₃ [185,190].

A study of PDA on AlSiO with Si content of 22% was carried out by Kikuta and co-workers by annealing from 650 °C to 1050 °C under N₂ for 10min [190]. A reduction in hysteresis and in V_{FB} drift under positive stress for a PDA higher than 650 °C was observed (**Figure 11**). For a PDA above 850 °C, a plateau on the I-V characteristic related to electron trapping is reduced. Contrary to Al₂O₃, AlSiO presents no sign of crystallization for a PDA at 850°C. However, the same group observed the onset of crystallization for AlSiO at the interface for a PDA at 950 °C. The proposed solution to reduce this crystallization was the

deposition of a thin SiO₂ layer at the AlSiO/GaN interface. Moreover, the SiO₂ interfacial layer improves μ_{FE} by 50% (i.e. 27.7–36.2 cm²·V⁻¹·s⁻¹), and is explained by the possible reduction of border traps [191].

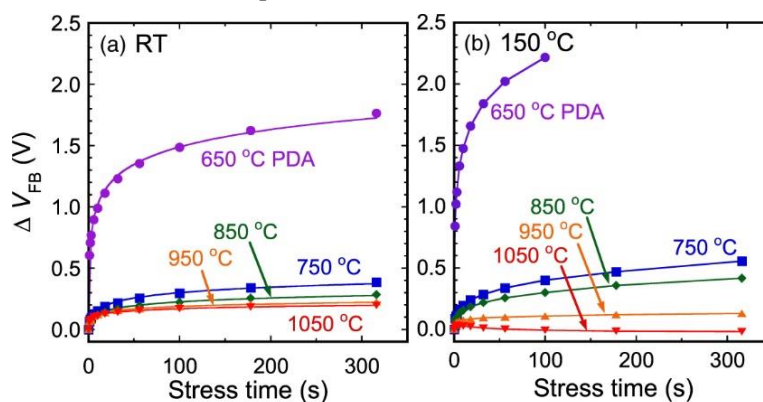


Figure 11. V_{FB} shift under positive bias stress at both room temperature and 150°C for AlSiO (21%Si)/n-GaN MOSCAPs under different PDA temperatures [190] (© The Japan Society of Applied Physics. Reproduced by permission of IOP Publishing Ltd. All rights reserved).

3.2.3 HfO₂ and SiO₂ alloys for improved mobility: HfSiO_x

Another interesting approach is the use of HfSiO_x by mixing HfO₂ and SiO₂ by ALD [69,196–199]. As AlSiO, HfSiO_x is deposited by alternating ALD HfO₂ and ALD SiO₂. Hf and Si composition is controlled by adjusting the ratio of HfO₂ and SiO₂ ALD cycles [198,199]. HfO₂ has a higher relative permittivity but suffers from low thermal stability. In the same way with AlSiO, the introduction of Si increases the thermal stability. In that matter, non-crystallized film after a PDA at 900°C for 5min is reported with a silicon content of 43% [199]. Reported values of relative permittivity are in the order of 13–18 with a high band gap around 6.5 eV, close to reported ALD Al₂O₃ band gap of 6.8 eV [196,199,200]. Compared to HfO₂, HfSiO_x leads to lower hysteresis possibly associated to fewer electron traps, but a lower V_{FB}/V_{TH} induced by possible positive charges is also reported [197,198]. For an ALE fully recessed MIS gate HEMT, a positive V_{TH} of 2.1V was reported [196].

In terms of interface quality with GaN or AlGaN, HfSiO_x has lower D_{it} than HfO₂ and Al₂O₃ (around 5×10^{11} cm⁻²·eV⁻¹ at $E_C - E_T \approx 0.3$ eV), possibly because of the high temperature PDA applied (i.e. 800°C). This highlights the higher interface quality of GaN with HfSiO_x than with HfO₂ and Al₂O₃ [196,198,199]. Combined with the high relative permittivity, transconductance is increased compared to Al₂O₃ in AlGaN/GaN HEMTs [199]. With an ALE fully recessed MIS gate HEMT, a μ_{FE} of around 406 cm²·V⁻¹·s⁻¹ is obtained [196].

3.2.4 Al₂O₃ and TiO₂ alloy for V_{TH} engineering: AlTiO

Finally, the use of AlTiO, a ternary alloy of Al₂O₃ and TiO₂ obtained through the deposition of ALD Al₂O₃ and TiO₂ nanolaminates offers an interesting solution to increase V_{TH} [201,202]. Combining Al₂O₃ with TiO₂ lead to finding a trade-off between TiO₂ high relative permittivity but small band gap (6.0 and 3.5eV respectively) with Al₂O₃ lower relative permittivity and higher band gap (~9 and ~7eV respectively) [157,158]. The obtained band gap and relative permittivity are in the order of 5–6 eV and ~22 respectively [201,202]. However, the major gain with AlTiO consists in the increase of V_{FB}/V_{TH} . Indeed, on the one hand, Nguyen and Suzuki reported that with a decreasing Al content from 100% to 35%, a reduction of positives charges at the AlTiO/AlGaN interface is observed and explained by the reduction of O-Ga and O-Al at the surface by Ti [202]. Combined with partially recessed AlGaN barrier, further reduction of interfacial charges is obtained as shown in **Figure 12.a**, leading to a V_{TH} of 1.7V with an Al content of 73% and a remaining AlGaN barrier of 4 nm [203]. Nonetheless, gate voltage of -6V is reported to induce a V_{TH}

negative shift of -0.5V [203]. On the other hand, Gupta and co-workers reported a Normally-OFF HEMT with a partially recessed AlGaN barrier (8nm) and an AlTiO layer after PDA [201]. With increasing Al content from 10% to 52%, an increase in V_{TH} is observed, allowing a V_{TH} of 0.5V. Compared to Al_2O_3 and TiO_2 on HEMTs, higher V_{TH} is obtained with a Ti content of 50% as represented in **Figure 12.b**. The increase of V_{TH} with Al content is explained and confirmed by the formation of p-type doping with deep acceptors states close to AlTiO's valence band [204]. These states are formed by Al replacing Ti in TiO_2 . Hence with higher Al content up to 52%, more p-doping is obtained. Concerning hysteresis, a low hysteresis of 40mV for V_{DS} of 15 V was reported. Finally, by combining both results, it seems that an intermediate Al content is the optimal content to have the highest V_{TH} .

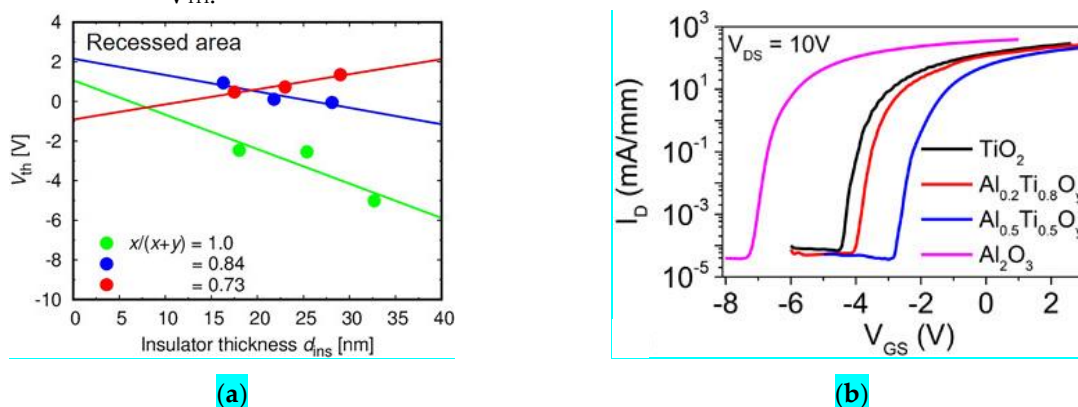


Figure 12. (a) V_{TH} in function of Al_xTi_yO thickness in partially recessed MIS Gate for different Al content. Increasing Ti content up to 27% combined with partial AlGaN recess reduce positive charges at the interface (Reprinted from [203], with the permission of AIP Publishing); (b) I_D - V_{GS} transfer characteristic for Al_2O_3 , TiO_2 , $Al_{0.2}Ti_{0.8}O_y$ and $Al_{0.5}Ti_{0.5}O_y$ on HEMTs. Decreasing Ti content up to 52% increase V_{TH} in comparison to Al_2O_3 , TiO_2 and $Al_{0.2}Ti_{0.8}O_y$ (Reprinted from [204], with the permission of AIP Publishing).

3.2.5 Summary

In conclusion, many dielectric candidates exist for MOSc-HEMT, from standard Al_2O_3 to alternative solution such as ternary alloys. Their implementation is beneficial for both electrical (i.e. hysteresis and V_{TH}) and material properties (i.e. crystallization temperature). For high thermal stability, AlON, AlSiO and $HfSiO_x$ are interesting, allowing higher thermal budget in the fabrication process. Better interface and less defects are also commonly reported for those dielectrics. Finally, AlTiO offers an interesting approach to increase the threshold voltage. Since AlTiO in a fully recessed gate is not yet reported, it would be reasonable to verify the possible V_{TH} obtained from this gate stack. A summary of the MOSCAPs discussed in this section is represented in **Table 3**:

Table 3. Summary of mentioned MOSCAPs.

Dielectric	Substrate Wet cleaning	Deposition technique	Annealing	V_{FB} (V)	ΔV_{FB} (mV)	D_{it} ($cm^{-2}eV^{-1}$)	Ref.
6nm Al_2O_3	n-GaN ($Si:5 \times 10^{18} cm^{-3}$) NH_4OH	ALD	PMA 400°C N_2/H_2 15min	~1.1	0	10^{12} ($E_C - E_T = 0.5 eV$)	[170]
5nm ALON (6.2% N)		PEALD		~1.4	40	10^{13} ($E_C - E_T = 0.5 eV$)	
11.5 nm ALON	AlGaN/GaN Acetone cleaning	PEALD nanolaminates	PDA 600°C N_2 30s PMA 400°C N_2/H_2 3min	+1.5 compared to Al_2O_3	/	$10^{13}-10^{11}$ ($E_C - E_T = 0.42-0.54 eV$)	[173]
10.5nm ALON (~8% N)	AlGaN/GaN 5min of 5% HCl	ALD	PDA 800°C N_2 3min PMA 600°C N_2 3min	/	/	/	[175]
25nm Al_2O_3	n-GaN ($2 \times 10^{17} cm^{-3}$)	MOCVD	/	-1.2	10(after 10min at +4V)	4.9×10^{12} ($E_C - E_T = 0.15$ to 2 eV)	[185]

25nm AlSiO (~44% Si)				-2.4	3 (after 10min at +4V)	6.4x10 ¹¹ (Ec -E _T = 0.15 to 2 eV)	
25nm Al ₂ O ₃				0.28	/	5.3x10 ¹² (Ec -E _T = 0.15 eV)	[186]
25nm AlSiO (28% Si)	n-GaN (2x10 ¹⁷ cm ⁻³)	MOCVD	/	-4.3	/	1.9x10 ¹² (Ec -E _T = 0.15 eV)	
24nm AlSiO (~46% Si)	N-face n-GaN (2.5x10 ¹⁷ cm ⁻³)	MOCVD	/	/	45	/	[187]
20nm Al ₂ O ₃	n-GaN (Si:1x10 ¹⁷ cm ⁻³)	PEALD	PDA 650°C N ₂ 1hr	-0.5	/	5.8x10 ¹¹ (Ec -E _T = 0.7 eV)	[188]
20nm AlSiO (21% Si)	1% HF	PEALD nanolaminates	PMA 400°C N ₂ 5min	-0.3	/	7.8x10 ¹¹ (Ec -E _T = 0.7 eV)	
40nm AlSiO (22% Si)	n-GaN (Si:1x10 ¹⁷ cm ⁻³) 1% HF	PEALD nanolaminates	PDA 950°C N ₂ 10min	Negative shift compared to ideal curve	/	/	[190]
20nm HfO ₂	Etched GaN HCl	ALD	/	/	200	2.5x10 ¹³ (Ec -E _T = 0.37 eV)	[197]
20nm HfSiO _x	Etched GaN HCl	ALD nanolaminates	/	/	150	1.6x10 ¹² (Ec -E _T = 0.37 eV)	
25.7nm HfO ₂	n-GaN (1.3x10 ¹⁸ cm ⁻³)	PEALD	PDA 800°C N ₂ 5min	2.05	600	6x10 ¹³ -4x10 ¹¹ (Ec -E _T =0.12-0.58 eV)	[198]
23nm HfSiO _x (43% Si)	Piranha + buffered HF	PEALD nanolaminates		0.63	70	8x10 ¹¹ -2x10 ¹¹ (Ec -E _T =0.15-0.6 eV)	

4. Conclusions

The fully recessed MIS gate GaN HEMT (or MOSc-HEMT) is a promising solution for Normally-OFF GaN-based power devices thanks to its positive threshold voltage, reduced leakage current and higher allowed gate-voltage swing. Its development can be challenging due to the impact of different process steps of the transistor. The main effect is the low and unstable V_{TH} , and the reduced mobility at the gate channel. In addition, the necessary etching of the AlGaN barrier introduces a GaN surface far from pristine.

The main challenges are a proper characterization of the induced damage and a process integration compatible with industrial requirements. Among the current developments, ALE represents a useful tool to mitigate the damage caused by ICP-RIE. Its controlled etching process associated to the removal of the damaged layer can reduce the roughness and increase the electron mobility. In similar fashion, recent work on selective area growth shows promising results but shares the same issues related to the dry etching step.

In addition to the etched surface, the GaN surface has a tendency to both contain more impurities than semiconductors such as silicon and has a difficult to remove native gallium oxide (i.e. GaO_x). This surface condition presents a challenge and specifically during air-break transitions. A recovery towards a more pristine GaN surface is possible through optimized etching (low impact etching and ALE) combined with specific surface treatments, from wet cleanings (e.g. HF or NH₄OH) to plasma treatment (e.g. Remote Plasma Pretreatment).

Interface layer, such as AlN, seems mandatory to increase the electron mobility as well as to protect the recessed surface from oxidation during dielectric deposition. The choice of the dielectric is also important, both to optimize the dielectric/GaN interface and be suitable with the integration process of the fully recessed MIS gate transistors. Al₂O₃ is frequently used thanks to its high band gap and high relative permittivity. However, unstable V_{TH} , low electron mobility and low thermal stability can limit its integration. Ternary alloys such as AlON, AlSiO and HfSiO_x could improve the above mentioned electrical properties as well as the thermal stability. As such, for AlON and AlSiO associated

622

623

624

625

626

627

628

629

630

631

632

633

634

635

636

637

638

639

640

641

642

643

644

645

646

647

648

649

650

with high temperature annealing, immunity to electron trapping increases, hence opening a path to lower V_{TH} instability. Moreover, the possible introduction of negative charges in AlON could increase V_{TH} . Another alternative is HfSiO_x which allows to increase the electron mobility thanks to both its good interface quality with GaN and its high relative permittivity. Combining HfSiO_x with AlN interfacial layer could possibly further increase the electron mobility. Specifically for V_{TH} engineering, the implementation of an AlTiO gate dielectric with an intermediary Ti content in fully recessed MIS Gate should further increase the V_{TH} thanks to its apparent p-type behavior. However, from the reviewed literature on MOSc-HEMT, the process having the highest V_{TH} is still in [166] with ICP-RIE and digital etching using Al₂O₃ with a PDA at 400°C.

To summarize, the combination of different process steps from etching to dielectric deposition need to be well controlled in order to fit the desired final device properties. Such developments are also important in the case of Vertical GaN MOS trench-gate transistors. A summary of the mentioned MOSc-HEMTs is reported in **Table 3**. Finally, a better understanding of gate-trench sidewall quality is needed in order to fully quantify their impact on device properties.

651
652
653
654
655
656
657
658
659
660
661
662
663
664
665
666
667

Table 3. Summary of mentioned fully recessed MIS gate HEMTs.

668

Substrate	Etching	Surface preparation	Interfacial layer	Dielectric	Annealing after deposition	V_{TH} (V)	ΔV_{TH} (mV)	Mobility μ_{FE} ($cm^2 \cdot V^{-1} \cdot s^{-1}$)	D_{it} ($cm^{-2} \cdot eV^{-1}$)	Ref.
Si/GaN/AlN/AlGaIn	ICP-RIE: Cl based	NH ₄ OH 0.6% 75°C	/	Al ₂ O ₃	/	0.6 ^a	/	/	/	[91]
Sapphire/GaN/Al _{0.26} Ga _{0.74} N	ICP-RIE	TMAH 5% 90°C 1hr	/	Al ₂ O ₃	Ohmic contact : 30s 800°C N ₂	3.5 ^b	/	/	/	[83]
Si/Al(GaN)/GaN/AlN/Al _{0.2} Ga _{0.8} N/ GaN/AlN/Al _{0.26} Ga _{0.74} /GaN	ALE: Oxidation + KOH	/	/	Al ₂ O ₃	PDA : 10min 400°C O ₂	0.4 ^a	200	396	/	[74]
Si/AlN/AlGaIn/GaN/Al _{0.2} Ga _{0.8} N	Selective Area Growth	UV treatment + acid solution	/	Al ₂ O ₃	PDA under N ₂	~0.5 ^c	~0	/	/	[133]
Si/GaN/AlN/AlGaIn	Selective Area Growth	HF/H ₂ SO ₄ /HCl	/	Al ₂ O ₃	Ohmic contact : 30s 850°C N ₂	2.6 ^b	/	80	Lowest = 9x10 ¹² Highest = 1x10 ¹³	[134]
Sapphire/GaN/AlN/ Al _{0.25} Ga _{0.75} N/GaN	ICP-RIE: BCl ₃ /Cl ₂	NH ₃ :H ₂ O + Oxidation through thin Al ₂ O ₃ + HCl wet etch	/	Al ₂ O ₃	PMA : 5min 450°C O ₂	2.8 ^a	300	48	/	[63]
Si/GaN/AlN/Al _{0.25} Ga _{0.75} N/GaN	ICP-RIE + digital etching	/	ICP/RF 5/10W + O ₂ plasma + NH ₃ anneal- ing: GaON	SiN _x	Ohmic contact : 30s 850°C N ₂	1.15 ^a	200	150	Lowest = 3x10 ¹² Highest = 1x10 ¹³	[139]
Sapphire/GaN/ Al _{0.23} Ga _{0.77} N/GaN	Wet etching	/	PECVD RF 200W N ₂ O: GaON	SiN _x	Ohmic contact : 30s 870°C N ₂	1.2 ^a	/	/	Lowest = ~3x10 ¹² Highest = 1x10 ¹³	[143]
SiC/GaN/AlN/Al _{0.25} Ga _{0.75} N	ICP-RIE: BCl ₃ /Cl ₂	/	PECVD 300W : N ₂ O	Al ₂ O ₃	Ohmic contact : 30s 840°C	1.5 ^b	/	658	Lowest = 1.5x10 ¹¹ Highest = 8x10 ¹²	[144]
Si/GaN/AlN/Al _{0.25} Ga _{0.75} N	Digital etching: O ₂ plasma + HCl	RPP	AlN	Al ₂ O ₃	PDA : 500°C O ₂	0.3 ^a	900	165	10 ¹¹ ~ 10 ¹²	[149]
Si/GaN/AlN/AlGaIn	ICP-RIE : BCl ₃ /Cl ₂ Digital etching: O ₂ plasma + HCl	/	/	Al ₂ O ₃	PDA : 10min 400°C N ₂	5.2 ^a	400	70	/	[166]
Si/GaN/AlN/AlGaIn	ICP-RIE: BCl ₃ /Cl ₂	/	/	AlON	PDA : 10min 500°C N ₂ PMA : 10min 400°C N ₂ /H ₂	2.25 ^c	180	235	Lowest = 3.5x10 ¹¹ Highest = 1x10 ¹³	[171]
Si/GaN/Al _{0.25} Ga _{0.75} N	ICP-RIE: SF ₆ BCl ₃ /Cl ₂	/	AlN	Al _{0.23} Si _{0.77} O	PDA	~0.5 ^c	/	1000 (μ_{eff})	/	[150]
Si/GaN/AlN/Al _{0.25} Ga _{0.75} N	ALE: O ₂ + BCl ₃ plasma	/	/	HfSiO _x	/	2.1 ^b	/	426	Lowest = 3x10 ¹¹ Highest = 6 x10 ¹²	[196]

V_{TH} extracted by: ^a normalized fixed I_{DS} current; ^b linear extrapolation; ^c extraction technique not mentioned

669

670

Author Contributions: Conceptualization, P.R., L.V., R.E. and J.B.; methodology, P.R. and L.V.; investigation, P.R., L.V. and J.B.; writing—original draft preparation, P.R., L.V., P.B., S.R., R.E. and J.B.; writing—review and editing, P.R., L.V., P.B., S.R., R.E. and J.B.; visualization, P.R.; supervision, JB; All authors have read and agreed to the published version of the manuscript.

Data Availability Statement: Not applicable.

Funding: This work was partially supported by the French Renatech network and by the French Public Authorities within the frame of the PSCP French national program “G-Mobility”: DOS0134974

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Efthymiou, L.; Longobardi, G.; Camuso, G.; Chien, T.; Chen, M.; Udrea, F. On the Physical Operation and Optimization of the P-GaN Gate in Normally-off GaN HEMT Devices. *Appl. Phys. Lett.* **2017**, *110*, 123502, doi:10.1063/1.4978690.
2. Hu, Y.; Hernández-Gutiérrez, C.A.; Solís-Cisneros, H.I.; Santana, G.; Kudriatsev, Y.; Camas-Anzueto, J.L.; López-López, M. Blue Luminescence Origin and Mg Acceptor Saturation in Highly Doped Zinc-Blende GaN with Mg. *Journal of Alloys and Compounds* **2022**, *897*, 163133, doi:10.1016/j.jallcom.2021.163133.
3. Lossy, R.; Gargouri, H.; Arens, M.; Würfl, J. Gallium Nitride MIS-HEMT Using Atomic Layer Deposited Al₂O₃ as Gate Dielectric. *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films* **2013**, *31*, 01A140, doi:10.1116/1.4771655.
4. Ahn, J.; Kim, D.; Park, K.-H.; Yoo, G.; Heo, J. Pt-Decorated Graphene Gate AlGaIn/GaN MIS-HEMT for Ultrahigh Sensitive Hydrogen Gas Detection. *IEEE Transactions on Electron Devices* **2021**, *68*, 1255–1261, doi:10.1109/TED.2021.3053515.
5. LMG1020 5-V, 7-A, 5-A Low-Side GaN and MOSFET Driver For 1-Ns Pulse Width Applications; Texas Instrument, 2018; p. 26;.
6. Le Royer, C.; Mohamad, B.; Biscarrat, J.; Vauche, L.; Escoffier, R.; Buckley, J.; Bécu, S.; Riat, R.; Gillot, C.; Charles, M.; et al. Normally-OFF 650V GaN-on-Si MOSc-HEMT Transistor: Benefits of the Fully Recessed Gate Architecture. In Proceedings of the 2022 IEEE 34th International Symposium on Power Semiconductor Devices and ICs (ISPSD); May 2022; pp. 49–52.
7. Zhu, R.; Jiang, H.; Tang, C.W.; Lau, K.M. High-Performance GaN Vertical Trench MOSFETs Grown on Si Substrate. In Proceedings of the 2022 Compound Semiconductor Week (CSW); June 2022; pp. 1–2.
8. Khadar, R.A.; Liu, C.; Soleimanzadeh, R.; Matioli, E. Fully Vertical GaN-on-Si Power MOSFETs. *IEEE Electron Device Letters* **2019**, *40*, 443–446, doi:10.1109/LED.2019.2894177.
9. Amano, H.; Baines, Y.; Beam, E.; Borga, M.; Bouchet, T.; Chalker, P.R.; Charles, M.; Chen, K.J.; Chowdhury, N.; Chu, R.; et al. The 2018 GaN Power Electronics Roadmap. *J. Phys. D: Appl. Phys.* **2018**, *51*, 163001, doi:10.1088/1361-6463/aaaf9d.
10. He, J.; Cheng, W.-C.; Wang, Q.; Cheng, K.; Yu, H.; Chai, Y. Recent Advances in GaN - Based Power HEMT Devices. *Advanced electronic materials* **2021**, *7*, 2001045, doi:10.1002/aelm.202001045.
11. Pearton, S.J.; Douglas, E.A.; Shul, R.J.; Ren, F. Plasma Etching of Wide Bandgap and Ultrawide Bandgap Semiconductors. *Journal of Vacuum Science & Technology A* **2020**, *38*, 020802, doi:10.1116/1.5131343.
12. Sreenidhi, T.; Baskar, K.; DasGupta, A.; DasGupta, N. Reactive Ion Etching of GaN in SF₆ + Ar and SF₆ + N₂ Plasma. *Semiconductor Science and Technology* **2008**, *23*, 125019, doi:10.1088/0268-1242/23/12/125019.
13. Shah, A.P.; Azizur Rahman, A.; Bhattacharya, A. Temperature-Dependence of Cl₂/Ar ICP-RIE of Polar, Semipolar, and Nonpolar GaN and AlN Following BCl₃/Ar Breakthrough Plasma. *Journal of Vacuum Science & Technology A* **2020**, *38*, 013001, doi:10.1116/1.5123787.
14. Lai, Y.-H.; Yeh, C.-T.; Hwang, J.-M.; Hwang, H.-L.; Chen, C.-T.; Hung, W.-H. Sputtering and Etching of GaN Surfaces. *The Journal of Physical Chemistry B* **2001**, *105*, 10029–10036, doi:10.1021/jp011728k.
15. Kambayashi, H.; Satoh, Y.; Ootomo, S.; Kokawa, T.; Nomura, T.; Kato, S.; Chow, T.P. Over 100A Operation Normally-off AlGaIn/GaN Hybrid MOS-HFET on Si Substrate with High-Breakdown Voltage. *Solid-State Electronics* **2010**, *54*, 660–664, doi:10.1016/j.sse.2010.01.001.

16. Liu, Z.; Wang, Y.; Xia, X.; Yang, H.; Li, J.; Gu, C. Fabrication of GaN Hexagonal Cones by Inductively Coupled Plasma Reactive Ion Etching. *Journal of Vacuum Science & Technology B, Nanotechnology and Microelectronics: Materials, Processing, Measurement, and Phenomena* **2016**, *34*, 041226, doi:10.1116/1.4954986. 716-718
17. Constant, A.; Baele, J.; Coppens, P.; Pestel, F.D.; Moens, P.; Tack, M. Recessing Process for Au-Free Ohmic Contacts Formation on AlGaIn/GaN Heterostructures with AlN Spacer. In Proceedings of the 2017 International Conference on Compound Semiconductor Manufacturing Technology (CS MANTECH); 2017. 719-721
18. Yamada, S.; Sakurai, H.; Osada, Y.; Furuta, K.; Nakamura, T.; Kamimura, R.; Narita, T.; Suda, J.; Kachi, T. Formation of Highly Vertical Trenches with Rounded Corners via Inductively Coupled Plasma Reactive Ion Etching for Vertical GaN Power Devices. *Appl. Phys. Lett.* **2021**, *118*, 102101, doi:10.1063/5.0040920. 722-724
19. Buttari, D.; Heikman, S.; Keller, S.; Mishra, U.K. Digital Etching for Highly Reproducible Low Damage Gate Recessing on AlGaIn/GaN HEMTs. In Proceedings of the Proceedings. IEEE Lester Eastman Conference on High Performance Devices; 2002. 725-727
20. Kanarik, K.J.; Lill, T.; Hudson, E.A.; Sriraman, S.; Tan, S.; Marks, J.; Vahedi, V.; Gottscho, R.A. Overview of Atomic Layer Etching in the Semiconductor Industry. *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films* **2015**, *33*, 020802, doi:10.1116/1.4913379. 728-730
21. Benrabah, S.; Legallais, M.; Besson, P.; Ruel, S.; Vauche, L.; Pelissier, B.; Thieuleux, C.; Salem, B.; Charles, M. H₃PO₄-Based Wet Chemical Etching for Recovery of Dry-Etched GaN Surfaces. *Applied Surface Science* **2022**, *582*, 152309, doi:10.1016/j.apsusc.2021.152309. 731-733
22. Cao, X.A.; Cho, H.; Pearton, S.J.; Dang, G.T.; Zhang, A.P.; Ren, F.; Shul, R.J.; Zhang, L.; Hickman, R.; Van Hove, J.M. Depth and Thermal Stability of Dry Etch Damage in GaN Schottky Diodes. *Applied Physics Letters* **1999**, *75*, 232–234, doi:10.1063/1.124332. 734-736
23. Wang, Q.; Jiang, Y.; Zhang, J.; Kawaharada, K.; Li, L.; Wang, D.; Ao, J.-P. Effects of Recess Process and Surface Treatment on the Threshold Voltage of GaN MOSFETs Fabricated on a AlGaIn/GaN Heterostructure. *Semiconductor Science and Technology* **2015**, *30*, 065004, doi:10.1088/0268-1242/30/6/065004. 737-739
24. Lee, J.-M.; Chang, K.-M.; Kim, S.-W.; Huh, C.; Lee, I.-H.; Park, S.-J. Dry Etch Damage in N-Type GaN and Its Recovery by Treatment with an N₂ Plasma. *JOURNAL OF APPLIED PHYSICS* **2000**, *87*, 5. 740-741
25. Yamada, S.; Takeda, K.; Toguchi, M.; Sakurai, H.; Nakamura, T.; Suda, J.; Kachi, T.; Sato, T. Depth Profiling of Surface Damage in N-Type GaN Induced by Inductively Coupled Plasma Reactive Ion Etching Using Photo-Electrochemical Techniques. *Appl. Phys. Express* **2020**, *13*, 106505, doi:10.35848/1882-0786/abb787. 742-744
26. Tokuda, H.; Harada, S.; Asubar, J.T.; Kuzuhara, M. Influence of Reactive-Ion-Etching Depth on Interface Properties in Al₂O₃/n-GaN MOS Diodes. *Japanese Journal of Applied Physics* **2019**, *58*, 106503, doi:10.7567/1347-4065/ab3d11. 745-746
27. Jiang, Y.; Wang, Q.P.; Tamai, K.; Miyashita, T.; Motoyama, S.; Wang, D.J.; Ao, J.P.; Ohno, Y. GaN MOSFET with Boron Trichloride-Based Dry Recess Process. *Journal of Physics: Conference Series* **2013**, *441*, 012025, doi:10.1088/1742-6596/441/1/012025. 747-749
28. Yatabe, Z.; Asubar, J.T.; Hashizume, T. Insulated Gate and Surface Passivation Structures for GaN-Based Power Transistors. *Journal of Physics D: Applied Physics* **2016**, *49*, 393001, doi:10.1088/0022-3727/49/39/393001. 750-751
29. Takashima, S.; Li, Z.; Chow, T.P. Sidewall Dominated Characteristics on Fin-Gate AlGaIn/GaN MOS-Channel-HEMTs. *IEEE Transactions on Electron Devices* **2013**, *60*, 3025–3031, doi:10.1109/TED.2013.2278185. 752-753
30. Yatabe, Z.; Hori, Y.; Kim, S.; Hashizume, T. Effects of Cl₂-Based Inductively Coupled Plasma Etching of AlGaIn on Interface Properties of Al₂O₃/AlGaIn/GaN Heterostructures. *Applied Physics Express* **2013**, *6*, 016502, doi:10.7567/APEX.6.016502. 754-755
31. Fukumizu, H.; Sekine, M.; Hori, M.; Kanomaru, K.; Kikuchi, T. Atomic Layer Etching of AlGaIn Using Cl₂ and Ar Gas Chemistry and UV Damage Evaluation. *Journal of Vacuum Science & Technology A* **2019**, *37*, 021002, doi:10.1116/1.5063795. 756-757

32. Foster, G.M.; Koehler, A.; Ebrish, M.; Gallagher, J.; Anderson, T.; Noesges, B.; Brillson, L.; Gunning, B.; Hobart, K.D.; Kub, F. Recovery from Plasma Etching-Induced Nitrogen Vacancies in p-Type Gallium Nitride Using UV/O₃ Treatments. *Appl. Phys. Lett.* **2020**, *117*, 082103, doi:10.1063/5.0021153. 758–760
33. Pernel, C.; Berthou, W.; Suman, S.; Ruel, S.; Vauche, L. Electrochemical Short Loop to Assess the Impact of Plasma and Surface Treatments on N-GaN.; Berlin, Germany., October 9 2022. 761–762
34. Lehmann, J.; Leroux, C.; Reibold, G.; Charles, M.; Torres, A.; Morvan, E.; Baines, Y.; Ghibaudo, G.; Bano, E. Novel Sheet Resistance Measurement on AlGaIn/GaN HEMT Wafer Adapted from Four-Point Probe Technique. In Proceedings of the Proceedings of the 2015 International Conference on Microelectronic Test Structures; Tempe, AZ, USA, March 2015; pp. 163–168. 763–766
35. Pimenta-Barros, P.; Chauvet, N.; Roux, F.L.; Burtin, P.; Tan, S.; Barnola, S.; Ruel, S.; Vauche, L.; Torres, A.; Plissonnier, M.; et al. GaN Damage Evaluation after Conventional Plasma Etching and Anisotropic Atomic Layer Etching. In Proceedings of the 41st International Symposium on Dry Process (DPS2019); Hiroshima, Japan, 2019; Vol. 41st, pp. 43–44. 767–769
36. Ruel, S.; Pimenta-Barros, P.; Roux, F.L.; Chauvet, N.; Massardier, M.; Thoueille, P.; Tan, S.; Shin, D.; Gaucher, F.; Posseme, N. Atomic Layer Etching of GaN Using Cl₂ and He or Ar Plasma. *Journal of Vacuum Science & Technology A* **2021**, *39*, 022601, doi:10.1116/6.0000830. 770–772
37. Tang, K.; Huang, W.; Chow, T.P. GaN MOS Capacitors and FETs on Plasma-Etched GaN Surfaces. *Journal of Electronic Materials* **2009**, *38*, 523–528, doi:10.1007/s11664-008-0617-y. 773–774
38. Cao, X.A.; Pearton, S.J.; Zhang, A.P.; Dang, G.T.; Ren, F.; Shul, R.J.; Zhang, L.; Hickman, R.; Hove, J.M.V. Electrical Effects of Plasma Damage in P-GaN. *APPLIED PHYSICS LETTERS* **1999**, *75*, 4. 775–776
39. Lin, M.E.; Fan, Z.F.; Ma, Z.; Allen, L.H.; Morkoç, H. Reactive Ion Etching of GaN Using BCl₃. *Appl. Phys. Lett.* **1994**, *64*, 887–888. 777–778
40. Sato, T.; Toguchi, M.; Komatsu, Y.; Uemura, K. Low-Damage Etching for AlGaIn/GaN HEMTs Using Photo-Electrochemical Reactions. *IEEE Transactions on Semiconductor Manufacturing* **2019**, 1–1, doi:10.1109/TSM.2019.2934727. 779–780
41. Heffernan, C.; Lynch, R.P.; Buckley, D.N. A Study of the Photoelectrochemical Etching of N-GaN in H₃PO₄ and KOH Electrolytes. *ECS Journal of Solid State Science and Technology* **2020**, *9*, 015003, doi:10.1149/2.0082001JSS. 781–782
42. Fariza, A.; Ji, X.; Gao, Y.; Ran, J.; Wang, J.; Wei, T. Role of Energy-Band Offset in Photo-Electrochemical Etching Mechanism of p-GaN Heterostructures. *Journal of Applied Physics* **2021**, *129*, 165701, doi:10.1063/5.0046560. 783–784
43. Horikiri, F.; Ohta, H.; Asai, N.; Narita, Y.; Yoshida, T.; Mishima, T. Excellent Potential of Photo-Electrochemical Etching for Fabricating High-Aspect-Ratio Deep Trenches in Gallium Nitride. *Applied Physics Express* **2018**, *11*, 091001, doi:10.7567/APEX.11.091001. 785–787
44. Thayne, I.; Li, X.; Millar, D.; Fu, Y.-C.; Peralagu, U. Plasma Processing of III-V Materials for Energy Efficient Electronics Applications.; Engelmann, S.U., Wise, R.S., Engelmann, S.U., Wise, R.S., Eds.; San Jose, California, United States, March 21 2017; p. 101490R. 788–790
45. Yamada, S. Reduction of Plasma-Induced Damage in n-Type GaN by Multistep-Bias Etching in Inductively Coupled Plasma Reactive Ion Etching. *Appl. Phys. Express* **2019**, *6*. 791–792
46. Lin, Y.-K.; Noda, S.; Lo, H.-C.; Liu, S.-C.; Wu, C.-H.; Wong, Y.-Y.; Luc, Q.H.; Chang, P.-C.; Hsu, H.-T.; Samukawa, S.; et al. AlGaIn/GaN HEMTs With Damage-Free Neutral Beam Etched Gate Recess for High-Performance Millimeter-Wave Applications. *IEEE Electron Device Letters* **2016**, *37*, 1395–1398, doi:10.1109/LED.2016.2609938. 793–795
47. Kauppinen, C.; Khan, S.A.; Sundqvist, J.; Suyatin, D.B.; Suihkonen, S.; Kauppinen, E.I.; Sopanen, M. Atomic Layer Etching of Gallium Nitride (0001). *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films* **2017**, *35*, 060603, doi:10.1116/1.4993996. 796–798

48. Ohba, T.; Yang, W.; Tan, S.; Kanarik, K.J.; Nojiri, K. Atomic Layer Etching of GaN and AlGa_N Using Directional Plasma-Enhanced Approach. *Japanese Journal of Applied Physics* **2017**, *56*, 06HB06, doi:10.7567/JJAP.56.06HB06. 799
800
49. Kanarik, K.J.; Tan, S.; Yang, W.; Kim, T.; Lill, T.; Kabansky, A.; Hudson, E.A.; Ohba, T.; Nojiri, K.; Yu, J.; et al. Predicting Synergy in Atomic Layer Etching. *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films* **2017**, *35*, 05C302, doi:10.1116/1.4979019. 801
802
803
50. Aroulanda, S.; Patard, O.; Altuntas, P.; Michel, N.; Pereira, J.; Lacam, C.; Gamarra, P.; Delage, S.L.; Defrance, N.; de Jaeger, J.-C.; et al. Cl₂/Ar Based Atomic Layer Etching of AlGa_N Layers. *Journal of Vacuum Science & Technology A* **2019**, *37*, 041001, doi:10.1116/1.5090106. 804
805
806
51. Despiau-Pujo, E.; Chabert, P.; Bansropun, S.; Thénot, D.; Plouhinec, P.; Cassette, S. Simulations of Radical and Ion Fluxes on a Wafer in a Cl₂/Ar Inductively Coupled Plasma Discharge: Confrontation with GaAs and GaN Etch Experiments. *Journal of Vacuum Science & Technology B, Nanotechnology and Microelectronics: Materials, Processing, Measurement, and Phenomena* **2010**, *28*, 693–701, doi:10.1116/1.3437492. 807
808
809
810
52. Despiau-Pujo, E.; Chabert, P. MD Simulations of GaN Sputtering by Ar⁺ Ions: Ion-Induced Damage and near-Surface Modification under Continuous Bombardment. *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films* **2010**, *28*, 1105–1110, doi:10.1116/1.3460904. 811
812
813
53. Deenapanray, P.N.K.; Petravić, M.; Kim, K.-J.; Kim, B.; Li, G. Compositional Changes on GaN Surfaces under Low-Energy Ion Bombardment Studied by Synchrotron-Based Spectroscopies. *Applied Physics Letters* **2003**, *83*, 4948–4950, doi:10.1063/1.1626792. 814
815
816
54. Petravic, M.; Deenapanray, P.N.K.; Coleman, V.A.; Kim, K.; Kim, B.; Li, G. Core-Level Photoemission and near-Edge x-Ray Absorption Fine-Structure Studies of GaN Surface under Low-Energy Ion Bombardment. *Journal of Applied Physics* **2004**, *95*, 5487–5493, doi:10.1063/1.1707232. 817
818
819
55. Venugopal, V.; Upadhyaya, K.; Kumar, K.; Shivaprasad, S.M. Ion Induced Compositional Changes and Nanodroplet Formation on GaN Surface. *Applied Surface Science* **2014**, *315*, 440–444, doi:10.1016/j.apsusc.2014.02.042. 820
821
56. Petravic, M.; Coleman, V.A.; Kim, K.-J.; Kim, B.; Li, G. Defect Acceptor and Donor in Ion-Bombarded GaN. *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films* **2005**, *23*, 1340–1345, doi:10.1116/1.1991869. 822
823
57. Hua, M.; Liu, C.; Yang, S.; Liu, S.; Fu, K.; Dong, Z.; Cai, Y.; Zhang, B.; Chen, K.J. GaN-Based Metal-Insulator-Semiconductor High-Electron-Mobility Transistors Using Low-Pressure Chemical Vapor Deposition SiN_x as Gate Dielectric. *IEEE Electron Device Letters* **2015**, *36*, 448–450, doi:10.1109/LED.2015.2409878. 824
825
826
58. Hua, M.; Zhang, Z.; Qian, Q.; Wei, J.; Bao, Q.; Tang, G.; Chen, K.J. High-Performance Fully-Recessed Enhancement- Mode GaN MIS-FETs with Crystalline Oxide Interlayer. In Proceedings of the Proceedings of The 29th International Symposium on Power Semiconductor Devices & ICs, Sapporo; 2017. 827
828
829
59. Hua, M.; Zhang, Z.; Wei, J.; Lei, J.; Tang, G.; Fu, K.; Cai, Y.; Zhang, B.; Chen, K.J. Integration of LPCVD-SiN_x Gate Dielectric with Recessed-Gate E-Mode GaN MIS-FETs: Toward High Performance, High Stability and Long TDDb Lifetime. In Proceedings of the IEDM16; 2016. 830
831
832
60. Le Roux, F.; Possémé, N.; Burtin, P.; Barnola, S.; Torres, A. XPS Study of a Selective GaN Etching Process Using Self-Limiting Cyclic Approach for Power Devices Application. *Microelectronic Engineering* **2020**, *228*, 111328, doi:10.1016/j.mee.2020.111328. 833
834
61. Zhou, Q.; Zhang, A.; Zhu, R.; Shi, Y.; Wang, Z.; Liu, L.; Chen, B.; Jin, Y.; Chen, W.; Zhang, B. Threshold Voltage Modulation by Interface Charge Engineering for High Performance Normally-off GaN MOSFETs with High Faulty Turn-on Immunity. In Proceedings of the Proceedings of the 2016 28th International Symposium on Power Semiconductor Devices and ICs (ISPSD); Prague, Czech Republic, June 2016. 835
836
837
838
62. Wu, J.; Lei, S.; Cheng, W.-C.; Sokolovskij, R.; Wang, Q.; Xia, G. (Maggie); Yu, H. Oxygen-Based Digital Etching of AlGa_N/GaN Structures with AlN as Etch-Stop Layers. *Journal of Vacuum Science & Technology A* **2019**, *37*, 060401, doi:10.1116/1.5115427. 839
840

63. Zhu, J.; Jing, S.; Ma, X.; Liu, S.; Wang, P.; Zhang, Y.; Zhu, Q.; Mi, M.; Hou, B.; Yang, L.; et al. Improvement of Electron Transport Property and On-Resistance in Normally-OFF Al₂O₃/AlGa_N/Ga_N MOS-HEMTs Using Post-Etch Surface Treatment. *IEEE Trans. Electron Devices* **2020**, *67*, 3541–3547, doi:10.1109/TED.2020.3007564. 841–843
64. Chiu, H.-C.; Chang, Y.-S.; Li, B.-H.; Wang, H.-C.; Kao, H.-L.; Chien, F.-T.; Hu, C.-W.; Xuan, R. High Uniformity Normally-OFF p-GaN Gate HEMT Using Self-Terminated Digital Etching Technique. *IEEE Transactions on Electron Devices* **2018**, *65*, 4820–4825, doi:10.1109/TED.2018.2871689. 844–846
65. Shih, P.-C.; Engel, Z.; Ahmad, H.; Doolittle, W.A.; Palacios, T. Wet-Based Digital Etching on GaN and AlGa_N. *Appl. Phys. Lett.* **2022**, *120*, 022101, doi:10.1063/5.0074443. 847–848
66. Zhou, Q.; Chen, B.; Jin, Y.; Huang, S.; Wei, K.; Liu, X.; Bao, X.; Mou, J.; Zhang, B. High-Performance Enhancement-Mode Al₂O₃/AlGa_N/Ga_N-on-Si MISFETs With 626 MW/Cm² Figure of Merit. *IEEE Transactions on Electron Devices* **2015**, *62*, 776–781, doi:10.1109/TED.2014.2385062. 849–851
67. Burnham, S.D.; Boutros, K.; Hashimoto, P.; Butler, C.; Wong, D.W.S.; Hu, M.; Micovic, M. Gate-Recessed Normally-off Ga_N-on-Si HEMT Using a New O₂-BCl₃ Digital Etching Technique. *physica status solidi (c)* **2010**, *7*, 2010–2012, doi:10.1002/pssc.200983644. 852–854
68. Mikhailovich, S.V.; Pavlov, A.Yu.; Tomosh, K.N.; Fedorov, Yu.V. Low-Energy Defectless Dry Etching of the AlGa_N/Al_N/Ga_N HEMT Barrier Layer. *Technical Physics Letters* **2018**, *44*, 435–437, doi:10.1134/S1063785018050218. 855–856
69. Hu, Q.; Li, S.; Li, T.; Wang, X.; Li, X.; Wu, Y. Channel Engineering of Normally-OFF AlGa_N/Ga_N MOS-HEMTs by Atomic Layer Etching and High-κ Dielectric. *IEEE Electron Device Letters* **2018**, *39*, 1377–1380, doi:10.1109/LED.2018.2856934. 857–858
70. Zhou, Q.; Yang, Y.; Hu, K.; Zhu, R.; Chen, W.; Zhang, B. Device Technologies of Ga_N-on-Si for Power Electronics: Enhancement-Mode Hybrid MOS-HFET and Lateral Diode. *IEEE Transactions on Industrial Electronics* **2017**, *64*, 8971–8979, doi:10.1109/TIE.2017.2652373. 859–861
71. Wang, H.; Wang, J.; Li, M.; Cao, Q.; Yu, M.; He, Y.; Wu, W. 823-MA/Mm Drain Current Density and 945-MW/Cm² Baliga's Figure-of-Merit Enhancement-Mode Ga_N MISFETs With a Novel PEALD-Al_N/LPCVD-Si₃N₄ Dual-Gate Dielectric. *IEEE Electron Device Letters* **2018**, *39*, 1888–1891, doi:10.1109/LED.2018.2879543. 862–864
72. Gao, J.; Jin, Y.; Xie, B.; Wen, C.P.; Hao, Y.; Wang, M. Ga_N Lateral Schottky Diodes with High Baliga's Figure-of-Merit Utilizing Self-Terminated, Low Damage Anode Recessing Technology. In Proceedings of the 2018 76th Device Research Conference (DRC); 2018; pp. 1–2. 865–867
73. Lin, S.; Wang, M.; Sang, F.; Tao, M.; Wen, C.P.; Xie, B.; Yu, M.; Wang, J.; Hao, Y.; Wu, W.; et al. A Ga_N HEMT Structure Allowing Self-Terminated, Plasma-Free Etching for High-Uniformity, High-Mobility Enhancement-Mode Devices. *IEEE Electron Device Letters* **2016**, *37*, 377–380, doi:10.1109/LED.2016.2533422. 868–870
74. Tao, M.; Liu, S.; Xie, B.; Wen, C.P.; Wang, J.; Hao, Y.; Wu, W.; Cheng, K.; Shen, B.; Wang, M. Characterization of 880 V Normally Off Ga_N MOSHEMT on Silicon Substrate Fabricated With a Plasma-Free, Self-Terminated Gate Recess Process. *IEEE Trans. Electron Devices* **2018**, *65*, 1453–1457, doi:10.1109/TED.2018.2808345. 871–873
75. Jo, Y.-W.; Son, D.-H.; Won, C.-H.; Lee, J.-H. Normally-Off AlGa_N/Ga_N-Based MOSHEMT by Using One-Step TMAH Wet Etching. **2016**, *5*. 874–875
76. Eller, B.S.; Yang, J.; Nemanich, R.J. Electronic Surface and Dielectric Interface States on Ga_N and AlGa_N. *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films* **2013**, *31*, 050807, doi:10.1116/1.4807904. 876–877
77. Zywiets, T.K.; Neugebauer, J.; Scheffler, M. The Adsorption of Oxygen at Ga_N Surfaces. *Applied Physics Letters* **1999**, *74*, 1695–1697, doi:10.1063/1.123658. 878–879
78. Khadar, R.A.; Liu, C.; Soleimanzadeh, R.; Matioli, E. Fully-Vertical Ga_N-on-Si Power MOSFETs. In Proceedings of the 2018 IEEE International Electron Devices Meeting (IEDM); June 2017; pp. 1–2. 880–881

79. Hirai, H.; Miura, Y.; Nakajima, A.; Harada, S.; Yamaguchi, H. Crystal-Orientation-Dependent Flatband Voltage of Non-Polar GaN MOS Interfaces Investigated Using Trench Sidewall Capacitors. *Appl. Phys. Lett.* **2021**, *119*, 071601, doi:10.1063/5.0060415.
80. Kodama, M.; Sugimoto, M.; Hayashi, E.; Soejima, N.; Ishiguro, O.; Kanechika, M.; Itoh, K.; Ueda, H.; Uesugi, T.; Kachi, T. GaN-Based Trench Gate Metal Oxide Semiconductor Field-Effect Transistor Fabricated with Novel Wet Etching. *Applied Physics Express* **2008**, *1*, 021104, doi:10.1143/APEX.1.021104.
81. Ji, D.; Li, W.; Agarwal, A.; Chan, S.H.; Haller, J.; Bisi, D.; Labrecque, M.; Gupta, C.; Cruse, B.; Lal, R.; et al. Improved Dynamic R_{ON} of GaN Vertical Trench MOSFETs (OG-FETs) Using TMAH Wet Etch. *IEEE Electron Device Letters* **2018**, *39*, 1030–1033, doi:10.1109/LED.2018.2843335.
82. Lu, B.; Sun, M.; Palacios, T. An Etch-Stop Barrier Structure for GaN High-Electron-Mobility Transistors. *IEEE Electron Device Letters* **2013**, *34*, 369–371, doi:10.1109/LED.2012.2237374.
83. Im, K.-S. Mobility Fluctuations in a Normally-Off GaN MOSFET Using Tetramethylammonium Hydroxide Wet Etching. *IEEE Electron Device Lett.* **2021**, *42*, 18–21, doi:10.1109/LED.2020.3035712.
84. Reddy, M.S.P.; Park, W.-S.; Im, K.-S.; Lee, J.-H. Dual-Surface Modification of AlGaIn/GaN HEMTs Using TMAH and Piranha Solutions for Enhancing Current and 1/f-Noise Characteristics. *IEEE Journal of the Electron Devices Society* **2018**, *6*, 791–796, doi:10.1109/JEDS.2018.2849444.
85. Stocker, D.A.; Schubert, E.F.; Redwing, J.M. Crystallographic Wet Chemical Etching of GaN. *Appl. Phys. Lett.* **1998**, *73*, 2654–2656, doi:10.1063/1.122543.
86. Wong, M.S.; Lee, C.; Myers, D.J.; Hwang, D.; Kearns, J.A.; Li, T.; Speck, J.S.; Nakamura, S.; DenBaars, S.P. Size-Independent Peak Efficiency of III-Nitride Micro-Light-Emitting-Diodes Using Chemical Treatment and Sidewall Passivation. *Applied Physics Express* **2019**, *12*, 097004, doi:10.7567/1882-0786/ab3949.
87. Yang, J.; Eller, B.S.; Nemanich, R.J. Surface Band Bending and Band Alignment of Plasma Enhanced Atomic Layer Deposited Dielectrics on Ga- and N-Face Gallium Nitride. *Journal of Applied Physics* **2014**, *116*, 123702, doi:10.1063/1.4895985.
88. Meunier, R.; Torres, A.; Charles, M.; Morvan, E.; Petit-Etienne, C.; Renault, O.; Billon, T. XPS Analysis of AlGaIn/GaN Surface after Chemical and N-Containing Plasma Treatments. *ECS Transactions* **2012**, *50*, 451–460, doi:10.1149/05003.0451ecst.
89. Sohal, R.; Dudek, P.; Hilt, O. Comparative Study of NH_4OH and HCl Etching Behaviours on AlGaIn Surfaces. *Applied Surface Science* **2010**, *256*, 2210–2214, doi:10.1016/j.apsusc.2009.09.075.
90. Zhernokletov, D.M.; Negara, M.A.; Long, R.D.; Aloni, S.; Nordlund, D.; McIntyre, P.C. Interface Trap Density Reduction for Al_2O_3 /GaN (0001) Interfaces by Oxidizing Surface Preparation Prior to Atomic Layer Deposition. *ACS Applied Materials & Interfaces* **2015**, *7*, 12774–12780, doi:10.1021/acsami.5b01600.
91. Vauche, L.; Chanuel, A.; Martinez, E.; Roure, M.-C.; Le Royer, C.; Bécu, S.; Gwoziecki, R.; Plissonnier, M. Study of an Al_2O_3 /GaN Interface for Normally Off MOS-Channel High-Electron-Mobility Transistors Using XPS Characterization: The Impact of Wet Surface Treatment on Threshold Voltage V_{TH} . *ACS Appl. Electron. Mater.* **2021**, *3*, 1170–1177, doi:10.1021/acsaelm.0c01023.
92. Jackson, C.M.; Arehart, A.R.; Grassman, T.J.; McSkimming, B.; Speck, J.S.; Ringel, S.A. Impact of Surface Treatment on Interface States of ALD Al_2O_3 /GaN Interfaces. *ECS Journal of Solid State Science and Technology* **2017**, *6*, P489–P494.
93. King, S.W.; Barnak, J.P.; Bremser, M.D.; Tracy, K.M.; Ronning, C.; Davis, R.F.; Nemanich, R.J. Cleaning of AlN and GaN Surfaces. *Journal of Applied Physics* **1998**, *84*, 5248–5260.
94. Uhlrich, J.J.; Grabow, L.C.; Mavrikakis, M.; Kuech, T.F. Practical Surface Treatments and Surface Chemistry of N-Type and p-Type GaN. *Journal of Electronic Materials* **2008**, *37*, 439–447, doi:10.1007/s11664-007-0348-5.
95. Okada, H.; Shinohara, M.; Kondo, Y.; Sekiguchi, H.; Yamane, K.; Wakahara, A. Investigation of HCl -Based Surface Treatment for GaN Devices. In Proceedings of the AIP Conf. Proc.; 2016; Vol. 1709, pp. 020011, 1–5.

96. Rosenberg, S.G.; Pennachio, D.J.; Wagenbach, C.; Johnson, S.D.; Nepal, N.; Kozen, A.C.; Woodward, J.M.; Robinson, Z.; Joress, H.; Ludwig, K.F.; et al. Low Temperature Surface Preparation of GaN Substrates for Atomic Layer Epitaxial Growth: Assessment of Ex Situ Preparations. *Journal of Vacuum Science & Technology A* **2019**, *37*, 020908, doi:10.1116/1.5080090. 923–925
97. English, C.R.; Wheeler, V.D.; Garces, N.Y.; Nepal, N.; Nath, A.; Hite, J.K.; Mastro, M.A.; Eddy, C.R. Impact of Surface Treatments on High- κ Dielectric Integration with Ga-Polar and N-Polar GaN. *Journal of Vacuum Science & Technology B, Nanotechnology and Microelectronics: Materials, Processing, Measurement, and Phenomena* **2014**, *32*, 03D106, doi:10.1116/1.4831875. 926–928
98. Yamamoto, A.; Kanatani, K.; Makino, S.; Kuzuhara, M. Metalorganic Vapor Phase Epitaxial Growth of AlGaIn Directly on Reactive-Ion Etching-Treated GaN Surfaces to Prepare AlGaIn/GaN Heterostructures with High Electron Mobility ($\sim 1500 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$): Impacts of Reactive-Ion Etching-Damaged Layer Removal. *Japanese Journal of Applied Physics* **2018**, *57*, 125501, doi:10.7567/JJAP.57.125501. 929–932
99. Auzelle, T.; Ullrich, F.; Hietzschold, S.; Brackmann, S.; Hillebrandt, S.; Kowalsky, W.; Mankel, E.; Lovrincic, R.; Fernández-Garrido, S. Electronic Properties of Air-Exposed GaN(11-00) and (0001) Surfaces after Several Device Processing Compatible Cleaning Steps. *Applied Surface Science* **2019**, *495*, 143514, doi:10.1016/j.apsusc.2019.07.256. 933–935
100. Nepal, N.; Garces, N.Y.; Meyer, D.J.; Hite, J.K.; Mastro, M.A.; Eddy, Jr., Charles R. Assessment of GaN Surface Pretreatment for Atomic Layer Deposited High- κ Dielectrics. *Applied Physics Express* **2011**, *4*, 055802, doi:10.1143/APEX.4.055802. 936–937
101. Duan, T.L.; Pan, J.S.; Ang, D.S. Investigation of Surface Band Bending of Ga-Face GaN by Angle-Resolved X-Ray Photoelectron Spectroscopy. *ECS Journal of Solid State Science and Technology* **2016**, *5*, P514–P517, doi:10.1149/2.0261609jss. 938–939
102. Hossain, T.; Wei, D.; Edgar, J.H.; Garces, N.Y.; Nepal, N.; Hite, J.K.; Mastro, M.A.; Eddy, C.R.; Meyer, H.M. Effect of GaN Surface Treatment on Al₂O₃/n-GaN MOS Capacitors. *Journal of Vacuum Science & Technology B, Nanotechnology and Microelectronics: Materials, Processing, Measurement, and Phenomena* **2015**, *33*, 061201, doi:10.1116/1.4931793. 940–942
103. Reiner, M.; Reiss, M.; Brünig, T.; Knuuttila, L.; Pietschnig, R.; Ostermaier, C. Chemical Understanding and Utility of H₃PO₄ Etching of Group-III-Nitrides: Chemical Understanding and Utility of H₃PO₄ Etching of Group-III-Nitrides. *Phys. Status Solidi B* **2015**, *252*, 1121–1126, doi:10.1002/pssb.201451504. 943–945
104. Lim, D.; Jung, W.S.; Choi, M.S.; Gil, Y.; Choi, C. The Effects of (NH₄)₂S_x Treatment on n-GaN MOS Device with Nano-Laminated ALD HfAlO_x and Ru Gate Stack. *Microelectronic Engineering* **2015**, *147*, 210–214, doi:10.1016/j.mee.2015.04.068. 946–947
105. Han, H.H.; Lim, D.; Sergeevich, A.S.; Jeon, Y.-R.; Lee, J.H.; Son, S.K.; Choi, C. Suppressed Charge Trapping Characteristics of (NH₄)₂S_x Passivated GaN MOS Device with Atomic Layer Deposited HfAlO_x Gate Dielectric. *Microelectronic Engineering* **2017**, *178*, 240–244, doi:10.1016/j.mee.2017.05.027. 948–950
106. Kim, K.; Jang, J. Improving Ni/GaN Schottky Diode Performance through Interfacial Passivation Layer Formed via Ultraviolet/Ozone Treatment. *Current Applied Physics* **2020**, *20*, 293–297, doi:10.1016/j.cap.2019.11.017. 951–952
107. Kim, K.; Ryu, J.H.; Kim, J.; Cho, S.J.; Liu, D.; Park, J.; Lee, I.-K.; Moody, B.; Zhou, W.; Albrecht, J.; et al. Band-Bending of Ga-Polar GaN Interfaced with Al₂O₃ through Ultraviolet/Ozone Treatment. *ACS Applied Materials & Interfaces* **2017**, *9*, 17576–17585, doi:10.1021/acsami.7b01549. 953–955
108. Li, Y.; Xiu, X.; Xiong, Z.; Hua, X.; Xie, Z.; Chen, P.; Liu, B.; Tao, T.; Zhang, R.; Zheng, Y. Single-Crystal GaN Layer Converted from β -Ga₂O₃ Films and Its Application for Free-Standing GaN. *CryEngComm* **2019**, *21*, 1224–1230, doi:10.1039/c8ce01336e. 956–957
109. Chen, D.-Y.; Persson, A.R.; Wen, K.-H.; Sommer, D.; Grünenpütt, J.; Blanck, H.; Thorsell, M.; Kordina, O.; Darakchieva, V.; Persson, P.O.Å.; et al. Impact of in Situ NH₃ Pre-Treatment of LPCVD SiN Passivation on GaN HEMT Performance. *Semicond. Sci. Technol.* **2022**, *37*, 035011, doi:10.1088/1361-6641/ac4b17. 958–960
110. Ho, Y.J.; Jin, H.S.; Ha, M.-W.; Park, T.J. Sulfur Incorporation at Interface Between Atomic-Layer-Deposited Al₂O₃ Thin Film and AlGaIn/GaN Heterostructure. *Electronic Materials Letters* **2019**, *15*, 179–185. 961–962

111. Cho, S.J.; Roberts, J.W.; Guiney, I.; Li, X.; Ternent, G.; Floros, K.; Humphreys, C.J.; Chalker, P.R.; Thayne, I.G. A Study of the Impact of In-Situ Argon Plasma Treatment before Atomic Layer Deposition of Al₂O₃ on GaN Based Metal Oxide Semiconductor Capacitor. *Microelectronic Engineering* **2015**, *147*, 277–280, doi:10.1016/j.mee.2015.04.067.
112. Wu, X.; Luo, W.; Liu, L.; Guo, L.; Liang, R.; Xu, J.; Wang, J. Effects of Argon Plasma Pretreatment on Polar and Nonpolar GaN/Al₂O₃ Interface. In Proceedings of the 2016 5th International Symposium on Next-Generation Electronics (ISNE); Hsinchu, Taiwan, May 2016; pp. 1–2.
113. Jung, W.S.; Lim, D.; Han, H.; Sokolov, A.S.; Jeon, Y.-R.; Choi, C. Influence of In-Situ NH₃ Plasma Passivation on the Electrical Characteristics of Ga-Face n-GaN MOS Capacitor with Atomic Layer Deposited HfO₂. *Solid-State Electronics* **2018**, *149*, 52–56, doi:10.1016/j.sse.2018.08.009.
114. Chen, P.-Y.; Posadas, A.B.; Kwon, S.; Wang, Q.; Kim, M.J.; Demkov, A.A.; Ekerdt, J.G. Cubic Crystalline Erbium Oxide Growth on GaN(0001) by Atomic Layer Deposition. *Journal of Applied Physics* **2017**, *122*, 215302, doi:10.1063/1.4999342.
115. Qin, X.; Dong, H.; Brennan, B.; Azacatl, A.; Kim, J.; Wallace, R.M. Impact of N₂ and Forming Gas Plasma Exposure on the Growth and Interfacial Characteristics of Al₂O₃ on AlGaIn. *Applied Physics Letters* **2013**, *103*, 221604, doi:10.1063/1.4833836.
116. Hashizume, T.; Ootomo, S.; Inagaki, T.; Hasegawa, H. Surface Passivation of GaN and GaN/AlGaIn Heterostructures by Dielectric Films and Its Application to Insulated-Gate Heterostructure Transistors. *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures* **2003**, *21*, 1828, doi:10.1116/1.1585077.
117. Yang, S.; Tang, Z.; Wong, K.-Y.; Lin, Y.-S.; Liu, C.; Lu, Y.; Huang, S.; Chen, K.J. High-Quality Interface in Al₂O₃/GaN/GaN/AlGaIn/GaN MIS Structures With In Situ Pre-Gate Plasma Nitridation. *IEEE Electron Device Letters* **2013**, *34*, 1497–1499, doi:10.1109/LED.2013.2286090.
118. Ozaki, S.; Ohki, T.; Kanamura, M.; Imada, T.; Nakamura, N.; Okamoto, N.; Miyajima, T.; Kikkawa, T. Effect of Oxidant Source on Threshold Voltage Shift of AlGaIn / GaN MIS-HEMTs Using ALD-Al₂O₃ Gate Insulator Films.; Boston MA, 2011.
119. Liu, S.; Yang, S.; Tang, Z.; Jiang, Q.; Liu, C.; Wang, M.; Shen, B.; Chen, K.J. Interface/Border Trap Characterization of Al₂O₃/AlN/GaN Metal-Oxide-Semiconductor Structures with an AlN Interfacial Layer. *Appl. Phys. Lett.* **2015**, *106*, 051605, doi:10.1063/1.4907861.
120. Zhang, Z.; Li, W.; Fu, K.; Yu, G.; Zhang, X.; Zhao, Y.; Sun, S.; Song, L.; Deng, X.; Xing, Z.; et al. AlGaIn/GaN MIS-HEMTs of Very-Low V_{th} Hysteresis and Current Collapse With In-Situ Pre-Deposition Plasma Nitridation and LPCVD-Si₃N₄ Gate Insulator. *IEEE Electron Device Letters* **2017**, *38*, 236–239, doi:10.1109/LED.2016.2636136.
121. Yang, S.; Tang, Z.; Wong, K.-Y.; Lin, Y.-S.; Lu, Y.; Huang, S.; Chen, K.J. Mapping of Interface Traps in High-Performance Al₂O₃/AlGaIn/GaN MIS-Heterostructures Using Frequency- and Temperature-Dependent C-V Techniques. In Proceedings of the Electron Devices Meeting (IEDM), 2013 IEEE International; Washington, DC, USA, 2013.
122. Yang, S.; Liu, S.; Liu, C.; Hua, M.; Chen, K.J. Gate Stack Engineering for GaN Lateral Power Transistors. *Semiconductor Science and Technology* **2016**, *31*, 024001, doi:10.1088/0268-1242/31/2/024001.
123. Tzou, A.-J.; Chu, K.-H.; Lin, I.-F.; Østregren, E.; Fang, Y.-S.; Wu, X.-P.; Wu, B.-W.; Shen, C.-H.; Shieh, J.-M.; Yeh, W.-K.; et al. AlN Surface Passivation of GaN-Based High Electron Mobility Transistors by Plasma-Enhanced Atomic Layer Deposition. *Nanoscale Research Letters* **2017**, *12*, doi:10.1186/s11671-017-2082-0.
124. Guo, F.; Huang, S.; Wang, X.; Luan, T.; Shi, W.; Deng, K.; Fan, J.; Yin, H.; Shi, J.; Mu, F.; et al. Suppression of Interface States between Nitride-Based Gate Dielectrics and Ultrathin-Barrier AlGaIn/GaN Heterostructure with in Situ Remote Plasma Pretreatments. *Appl. Phys. Lett.* **2021**, *118*, 093503, doi:10.1063/5.0041421.
125. Amalraj, F.W.; Dhasiyan, A.K.; Lu, Y.; Shimizu, N.; Oda, O.; Ishikawa, K.; Kondo, H.; Sekine, M.; Ikarashi, N.; Hori, M. Effect of N₂/H₂ Plasma on GaN Substrate Cleaning for Homoepitaxial GaN Growth by Radical-Enhanced Metalorganic Chemical Vapor Deposition (REMOCVD). *AIP Advances* **2018**, *8*, 115116, doi:10.1063/1.5050819.

126. Horng, R.-H.; Tseng, M.-C.; Wu, D.-S. Surface Treatments on the Characteristics of Metal–Oxide Semiconductor Capacitors. *Crystals* **2019**, *9*, 1, doi:10.3390/cryst9010001. 1004
1005
127. Mukherjee, K.; De Santi, C.; You, S.; Geens, K.; Borga, M.; Decoutere, S.; Bakeroot, B.; Diehle, P.; Altmann, F.; Meneghesso, G.; et al. Study and Characterization of GaN MOS Capacitors: Planar vs Trench Topographies. *Appl. Phys. Lett.* **2022**, *120*, 143501, doi:10.1063/5.0087245. 1006
1007
1008
128. Yang, C.; Luo, X.; Zhang, A.; Deng, S.; Ouyang, D.; Peng, F.; Wei, J.; Zhang, B.; Li, Z. AlGaIn/GaN MIS-HEMT With AlN Interface Protection Layer and Trench Termination Structure. *IEEE Transactions on Electron Devices* **2018**, 1–5, doi:10.1109/TED.2018.2868104. 1009
1010
1011
129. Wei, D.; Hossain, T.; Nepal, N.; Garces, N.Y.; Hite, J.K.; Meyer, H.M.; Eddy, C.R.; Edgar, J.H. Comparison of the Physical, Chemical and Electrical Properties of ALD Al₂O₃ on c- and m- Plane GaN: Comparison of the Physical, Chemical and Electrical Properties of ALD Al₂O₃ on c- and m- Plane GaN. *physica status solidi (c)* **2014**, *11*, 898–901, doi:10.1002/pssc.201300677. 1012
1013
1014
1015
130. Wu, X.; Liang, R.; Guo, L.; Liu, L.; Xiao, L.; Shen, S.; Xu, J.; Wang, J. Improved Interface Properties of GaN Metal-Oxide-Semiconductor Device with Non-Polar Plane and AlN Passivation Layer. *Appl. Phys. Lett.* **2016**, *109*, 232101, doi:10.1063/1.4971352. 1016
1017
1018
131. Ando, Y.; Nagamatsu, K.; Deki, M.; Taoka, N.; Tanaka, A.; Nitta, S.; Honda, Y.; Nakamura, T.; Amano, H. Electrical Properties of GaN Metal-Insulator-Semiconductor Field-Effect Transistors with Al₂O₃/GaN Interfaces Formed on Vicinal Ga-Polar and Nonpolar Surfaces. *Applied Physics Letters* **2020**, *7*. 1019
1020
1021
132. Fu, H.; Fu, K.; Yang, C.; Liu, H.; Hatch, K.A.; Peri, P.; Herath Mudiyansele, D.; Li, B.; Kim, T.-H.; Alugubelli, S.R.; et al. Selective Area Regrowth and Doping for Vertical Gallium Nitride Power Devices: Materials Challenges and Recent Progress. *Materials Today* **2021**, *49*, 296–323, doi:10.1016/j.mattod.2021.04.011. 1022
1023
1024
133. Tajima, J.; Hikosaka, T.; Kuraguchi, M.; Nunoue, S. Improvement of Electrical Characteristics in Regrown AlGaIn/GaN MOSFETs by Suppression of the Residual Interface Charge. *Journal of Crystal Growth* **2019**, *509*, 129–132, doi:10.1016/j.jcrysgro.2018.10.051. 1025
1026
1027
134. He, L.; Li, L.; Yang, F.; Zheng, Y.; Zhang, J.; Que, T.; Liu, Z.; Zhang, J.; Wu, Q.; Liu, Y. Correlating Device Behaviors with Semiconductor Lattice Damage at MOS Interface by Comparing Plasma-Etching and Regrown Recessed-Gate Al₂O₃/GaN MOS-FETs. *Applied Surface Science* **2021**, *546*, 148710, doi:10.1016/j.apsusc.2020.148710. 1028
1029
1030
135. Ji, D.; Gupta, C.; Chan, S.H.; Agarwal, A.; Li, W.; Keller, S.; Mishra, U.K.; Chowdhury, S. Demonstrating >1.4 KV OG-FET Performance with a Novel Double Field-Plated Geometry and the Successful Scaling of Large-Area Devices.; San Francisco, CA, USA, 2017; p. 9.4.1-9.4.4. 1031
1032
1033
136. Yamada, T.; Ito, J.; Asahara, R.; Watanabe, K.; Nozaki, M.; Nakazawa, S.; Anda, Y.; Ishida, M.; Ueda, T.; Yoshigoe, A.; et al. Comprehensive Study on Initial Thermal Oxidation of GaN(0001) Surface and Subsequent Oxide Growth in Dry Oxygen Ambient. *Journal of Applied Physics* **2017**, *121*, 035303, doi:10.1063/1.4974458. 1034
1035
1036
137. Duan, T.L.; Pan, J.S.; Ang, D.S. Effect of Post-Deposition Annealing on the Interface Electronic Structures of Al₂O₃-Capped GaN and GaN/AlGaIn/GaN Heterostructure. *ECS J. Solid State Sci. Technol.* **2015**, *4*, P364–P368, doi:10.1149/2.0081509jss. 1037
1038
138. Tokuda, H.; Asubar, J.T.; Kuzuhara, M. AlGaIn/GaN Metal–Insulator–Semiconductor High-Electron Mobility Transistors with High on/off Current Ratio of over 5×10^{10} Achieved by Ozone Pretreatment and Using Ozone Oxidant for Al₂O₃ Gate Insulator. *Jpn. J. Appl. Phys.* **2016**, *55*, 120305, doi:10.7567/JJAP.55.120305. 1039
1040
1041
139. Hua, M.; Wei, J.; Tang, G.; Zhang, Z.; Qian, Q.; Cai, X.; Wang, N.; Chen, K.J. Normally-Off LPCVD-Si_x/GaN MIS-FET With Crystalline Oxidation Interlayer. *IEEE Electron Device Lett.* **2017**, *38*, 929–932, doi:10.1109/LED.2017.2707473. 1042
1043
140. Hua, M.; Cai, X.; Yang, S.; Zhang, Z.; Zheng, Z.; Wei, J.; Wang, N.; Chen, K.J. Suppressed Hole-Induced Degradation in E-Mode GaN MIS-FETs with Crystalline GaOxN_{1-x} Channel.; San Francisco, CA, USA, 2018; p. 30.3.1-30.3.4. 1044
1045

141. Cai, X.; Hua, M.; Zhang, Z.; Yang, S.; Zheng, Z.; Cai, Y.; Chen, K.J.; Wang, N. Atomic-Scale Identification of Crystalline GaON Nanophase for Enhanced GaN MIS-FET Channel. *Appl. Phys. Lett.* **2019**, *114*, 053109, doi:10.1063/1.5078767. 1046
1047
142. Qin, X.; Dong, H.; Kim, J.; Wallace, R.M. A Crystalline Oxide Passivation for Al₂O₃/AlGaIn/GaN. *Appl. Phys. Lett.* **2014**, *105*, 141604, doi:10.1063/1.4897641. 1048
1049
143. Li, M.; Wang, J.; Wang, H.; Cao, Q.; Liu, J.; Huang, C. Improved Performance of Fully-Recessed Normally-off LPCVD SiN/GaN MISFET Using N₂O Plasma Pretreatment. *Solid-State Electronics* **2019**, *156*, 58–61, doi:10.1016/j.sse.2019.03.067. 1050
1051
144. He, Y.; He, Q.; Mi, M.; Zhang, M.; Wang, C.; Yang, L.; Ma, X.; Hao, Y. High Breakdown Electric Field MIS-Free Fully Recessed-Gate Normally Off AlGaIn/GaN HEMT With N₂O Plasma Treatment. *IEEE J. Emerg. Sel. Topics Power Electron.* **2021**, *9*, 2163–2170, doi:10.1109/JESTPE.2019.2940594. 1052
1053
1054
145. Zhu, J.; Ma, M.; Zhu, Q.; Hou, B.; Chen, L.; Yang, L.; Zhou, X.; Ma, X.; Hao, Y. High Performance Normally-Off Al₂O₃/AlGaIn/GaN MOS-HEMTs Using Diffusion-Controlled Interface Oxidation Technique.; IEEE: Xi'an, China, 2018; pp. 135–139. 1055
1056
1057
146. Zhu, J.; Zhang, Y.; Ma, X.; Liu, S.; Jing, S.; Zhu, Q.; Mi, M.; Hou, B.; Yang, L.; Uren, M.J.; et al. Interface Property and Band Offset Investigation of GaN Based MOS Heterostructures with Diffusion-Controlled Interface Oxidation Technique. *Semicond. Sci. Technol.* **2020**, *7*. 1058
1059
1060
147. Zoroddu, A.; Bernardini, F.; Ruggerone, P.; Fiorentini, V. First-Principles Prediction of Structure, Energetics, Formation Enthalpy, Elastic Constants, Polarization, and Piezoelectric Constants of AlN, GaN, and InN: Comparison of Local and Gradient-Corrected Density-Functional Theory. *Phys. Rev. B* **2001**, *64*, 045208, doi:10.1103/PhysRevB.64.045208. 1061
1062
1063
148. Hsieh, T.-E.; Chang, E.Y.; Song, Y.-Z.; Lin, Y.-C.; Wang, H.-C.; Liu, S.-C.; Salahuddin, S.; Hu, C.C. Gate Recessed Quasi-Normally OFF Al₂O₃/AlGaIn/GaN MIS-HEMT With Low Threshold Voltage Hysteresis Using PEALD AlN Interfacial Passivation Layer. *IEEE ELECTRON DEVICE LETTERS* **2014**, *35*, 3. 1064
1065
1066
149. Liu, S.; Yang, S.; Tang, Z.; Jiang, Q.; Liu, C.; Wang, M.; Chen, K.J. Al₂O₃/AlN/GaN MOS-Channel-HEMTs With an AlN Interfacial Layer. *IEEE Electron Device Lett.* **2014**, *35*, 723–725, doi:10.1109/LED.2014.2322379. 1067
1068
150. Smith, M.; Kajiwara, Y.; Ono, H.; Huang, P.-C.; Kato, D.; Mukai, A.; Shindome, A.; Kuraguchi, M. High Mobility in GaN MOSFETs with AlSiO Gate Dielectric and AlN Mobility Enhancement Layer. In Proceedings of the 2021 IEEE 8th Workshop on Wide Bandgap Power Devices and Applications (WiPDA); IEEE: Redondo Beach, CA, USA, November 7 2021; pp. 283–287. 1069
1070
1071
1072
151. Ito, K.; Tomita, K.; Kikuta, D.; Horita, M.; Narita, T. Improvement of Channel Mobility in AlSiO/GaN MOSFETs Using Thin Interfacial Layers to Reduce Border Traps.; Makuhari, Japan, 2022; p. 2. 1073
1074
152. Asubar, J.T.; Yatabe, Z.; Gregusova, D.; Hashizume, T. Controlling Surface/Interface States in GaN-Based Transistors: Surface Model, Insulated Gate, and Surface Passivation. *Journal of Applied Physics* **2021**, *129*, 121102, doi:10.1063/5.0039564. 1075
1076
153. Bernardini, F.; Fiorentini, V.; Vanderbilt, D. Polarization-Based Calculation of the Dielectric Tensor of Polar Crystals. *Phys. Rev. Lett.* **1997**, *79*, 3958–3961, doi:10.1103/PhysRevLett.79.3958. 1077
1078
154. Passlack, M.; Hunt, N.E.J.; Schubert, E.F.; Zydzik, G.J.; Hong, M.; Mannaerts, J.P.; Opila, R.L.; Fischer, R.J. Dielectric Properties of Electron - beam Deposited Ga₂O₃ Films. *Appl. Phys. Lett.* **1994**, *64*, 2715–2717, doi:10.1063/1.111452. 1079
1080
155. Robertson, J.; Falabretti, B. Band Offsets of High K Gate Oxides on III-V Semiconductors. *Journal of Applied Physics* **2006**, *100*, 014111, doi:10.1063/1.2213170. 1081
1082
156. Mitrovic, I.Z.; Das, P.; Jones, L.; Gibbon, J.; Dhanak, V.R.; Mahapatra, R.; Partida Manzanera, T.; Roberts, J.W.; Potter, R.J.; Chalker, P.R.; et al. (Invited) Band Line-up of High-k Oxides on GaN. *ECS Trans.* **2020**, *97*, 67–81, doi:10.1149/09701.0067ecst. 1083
1084
157. Robertson, J. Band Offsets of Wide-Band-Gap Oxides and Implications for Future Electronic Devices. *J. Vac. Sci. Technol. B* **2000**, *18*, 1785, doi:10.1116/1.591472. 1085
1086
158. Robertson, J. High Dielectric Constant Oxides. *Eur. Phys. J. Appl. Phys.* **2004**, *28*, 265–291, doi:10.1051/epjap:2004206. 1087

159. Ostermaier, C.; Lee, H.-C.; Hyun, S.-Y.; Ahn, S.-I.; Kim, K.-W.; Cho, H.-I.; Ha, J.-B.; Lee, J.-H. Interface Characterization of ALD Deposited Al₂O₃ on GaN by CV Method. *phys. stat. sol. (c)* **2008**, *5*, 1992–1994, doi:10.1002/pssc.200778663. 1088
1089
160. Hori, Y.; Mizue, C.; Hashizume, T. Process Conditions for Improvement of Electrical Properties of Al₂O₃/n-GaN Structures Prepared by Atomic Layer Deposition. *Jpn. J. Appl. Phys.* **2010**, *49*, 080201, doi:10.1143/JJAP.49.080201. 1090
1091
161. Winzer, A.; Szabó, N.; Wachowiak, A.; Jordan, P.M.; Heitmann, J.; Mikolajick, T. Impact of Postdeposition Annealing upon Film Properties of Atomic Layer Deposition-Grown Al₂O₃ on GaN. *Journal of Vacuum Science & Technology B, Nanotechnology and Microelectronics: Materials, Processing, Measurement, and Phenomena* **2015**, *33*, 01A106, doi:10.1116/1.4904968. 1092
1093
1094
162. Fernandes Paes Pinto Rocha, P.; Vauche, L.; Mohamad, B.; Vandendaele, W.; Martinez, E.; Veillerot, M.; Spelta, T.; Rochat, N.; Gwoziecki, R.; Salem, B.; et al. Impact of Post-Deposition Anneal on ALD Al₂O₃/Etched GaN Interface for Gate-First MOSc-HEMT. *Power Electronic Devices and Components* **2023**, *4*, 100033, doi:10.1016/j.pedc.2023.100033. 1095
1096
1097
163. Zhou, H.; Ng, G.I.; Liu, Z.H.; Arulkumaran, S. Improved Device Performance by Post-Oxide Annealing in Atomic-Layer-Deposited Al₂O₃/AlGaIn/GaN Metal-Insulator-Semiconductor High Electron Mobility Transistor on Si. *Appl. Phys. Express* **2011**, *4*, 104102, doi:10.1143/APEX.4.104102. 1098
1099
1100
164. Yuge, K.; Nabatame, T.; Irokawa, Y.; Ohi, A.; Ikeda, N.; Uedono, A.; Sang, L.; Koide, Y.; Ohishi, T. Influence of Post-Deposition Annealing on Interface Characteristics at Al₂O₃/n-GaN. **2019**, *3*. 1101
1102
165. Nakazawa, S.; Shih, H.-A.; Tsurumi, N.; Anda, Y.; Hatsuda, T.; Ueda, T.; Kimoto, T.; Hashizume, T. Effects of Post-Deposition Annealing in O₂ on Threshold Voltage of Al₂O₃/AlGaIn/GaN MOS Heterojunction Field-Effect Transistors. *Jpn. J. Appl. Phys.* **2019**, *58*, 030902, doi:10.7567/1347-4065/aafd17. 1103
1104
1105
166. Zhou, Q.; Liu, L.; Zhang, A.; Chen, B.; Jin, Y.; Shi, Y.; Wang, Z.; Chen, W.; Zhang, B. 7.6 V Threshold Voltage High-Performance Normally-Off Al₂O₃/GaIn MOSFET Achieved by Interface Charge Engineering. *IEEE ELECTRON DEVICE LETTERS* **2016**, *37*, *4*, doi:10.1109/LED.2015.2511026. 1106
1107
1108
167. Kubo, T.; Miyoshi, M.; Egawa, T. Post-Deposition Annealing Effects on the Insulator/Semiconductor Interfaces of Al₂O₃/AlGaIn/GaN Structures on Si Substrates. *Semicond. Sci. Technol.* **2017**, *32*, 065012, doi:10.1088/1361-6641/aa6c09. 1109
1110
168. Marron, T.; Takashima, S.; Li, Z.; Chow, T.P. Impact of Annealing on ALD Al₂O₃ Gate Dielectric for GaN MOS Devices. *Phys. Status Solidi C* **2012**, *9*, 907–910, doi:10.1002/pssc.201100414. 1111
1112
169. Asahara, R.; Nozaki, M.; Yamada, T.; Ito, J.; Nakazawa, S.; Ishida, M.; Ueda, T.; Yoshigoe, A.; Hosoi, T.; Shimura, T.; et al. Effect of Nitrogen Incorporation into Al-Based Gate Insulators in AlON/AlGaIn/GaN Metal-Oxide-Semiconductor Structures. *Appl. Phys. Express* **2016**, *5*, doi:10.7567/apex.9.101002. 1113
1114
1115
170. Negara, M.A.; Kitano, M.; Long, R.D.; McIntyre, P.C. Oxide Charge Engineering of Atomic Layer Deposited AlO_xN_y/Al₂O₃ Gate Dielectrics: A Path to Enhancement Mode GaN Devices. *ACS Appl. Mater. Interfaces* **2016**, *8*, 21089–21094, doi:10.1021/acsami.6b03862. 1116
1117
1118
171. Kang, M.-J.; Eom, S.-K.; Kim, H.-S.; Lee, C.-H.; Cha, H.-Y.; Seo, K.-S. Normally-off Recessed-Gate AlGaIn/GaN MOS-HFETs with Plasma Enhanced Atomic Layer Deposited AlO_xN_y Gate Insulator. *Semicond. Sci. Technol.* **2019**, *34*, 055018, doi:10.1088/1361-6641/ab10f1. 1119
1120
1121
172. Chen, H.-Y.; Lu, H.-L.; Chen, J.-X.; Zhang, F.; Ji, X.-M.; Liu, W.-J.; Yang, X.-F.; Zhang, D.W. Low-Temperature One-Step Growth of AlON Thin Films with Homogenous Nitrogen-Doping Profile by Plasma-Enhanced Atomic Layer Deposition. *ACS Appl. Mater. Interfaces* **2017**, *9*, 38662–38669, doi:10.1021/acsami.7b12262. 1122
1123
1124
173. Wang, Q.; Cheng, X.; Zheng, L.; Shen, L.; Li, J.; Zhang, D.; Qian, R.; Yu, Y. PEALD Induced Interface Engineering of AlNO/AlGaIn/GaN MIS Diode with Alternate Insertion of AlN in Al₂O₃. In Proceedings of the 2017 29th International Symposium on Power Semiconductor Devices and IC's (ISPSD); 2017; pp. 215–218. 1125
1126
1127

174. Wang, Q.; Cheng, X.; Zheng, L.; Ye, P.; Li, M.; Shen, L.; Li, J.; Zhang, D.; Gu, Z.; Yu, Y. Band Alignment between PEALD-AlNO and AlGa_N/Ga_N Determined by Angle-Resolved X-Ray Photoelectron Spectroscopy. *Applied Surface Science* **2017**, *423*, 675–679, doi:10.1016/j.apsusc.2017.06.192.
175. Nozaki, M.; Watanabe, K.; Yamada, T.; Shih, H.-A.; Nakazawa, S.; Anda, Y.; Ueda, T.; Yoshigoe, A.; Hosoi, T.; Shimura, T.; et al. Implementation of Atomic Layer Deposition-Based AlON Gate Dielectrics in AlGa_N/Ga_N MOS Structure and Its Physical and Electrical Properties. *Jpn. J. Appl. Phys.* **2018**, *57*, 06KA02, doi:10.7567/JJAP.57.06KA02.
176. Hosoi, T.; Azumo, S.; Kashiwagi, Y.; Hosaka, S.; Yamamoto, K.; Aketa, M.; Asahara, H.; Nakamura, T.; Kimoto, T.; Shimura, T.; et al. Comprehensive and Systematic Design of Metal/High-k Gate Stack for High-Performance and Highly Reliable SiC Power MOSFET. *Jpn. J. Appl. Phys.* **2020**, *59*, 021001, doi:10.7567/1347-4065/ab65a3.
177. Kojima, E.; Chokawa, K.; Shirakawa, H.; Araidai, M.; Hosoi, T.; Watanabe, H.; Shiraiishi, K. Effect of Incorporation of Nitrogen Atoms in Al₂O₃ Gate Dielectric of Wide-Bandgap-Semiconductor MOSFET on Gate Leakage Current and Negative Fixed Charge. *Appl. Phys. Express* **2018**, *11*, 061501, doi:10.7567/APEX.11.061501.
178. Nakazawa, S.; Shih, H.-A.; Tsurumi, N.; Anda, Y.; Hatsuda, T.; Ueda, T.; Nozaki, M.; Yamada, T.; Hosoi, T.; Shimura, T.; et al. Fast Switching Performance by 20 A / 730 V AlGa_N/Ga_N MIS-HFET Using AlON Gate Insulator. In Proceedings of the 2017 IEEE International Electron Devices Meeting (IEDM); 2017; p. 25.1.1-25.1.4.
179. Choi, M.; Lyons, J.L.; Janotti, A.; Van de Walle, C.G. Impact of Carbon and Nitrogen Impurities in High-κ Dielectrics on Metal-Oxide-Semiconductor Devices. *Appl. Phys. Lett.* **2013**, *102*, 142902, doi:10.1063/1.4801497.
180. Guo, Z.; Ambrosio, F.; Pasquarello, A. Extrinsic Defects in Amorphous Oxides: Hydrogen, Carbon, and Nitrogen Impurities in Alumina. *Phys. Rev. Applied* **2019**, *11*, 024040, doi:10.1103/PhysRevApplied.11.024040.
181. Hosoi, T.; Azumo, S.; Kashiwagi, Y.; Hosaka, S.; Yamamoto, K.; Aketa, M.; Asahara, H.; Nakamura, T.; Kimoto, T.; Shimura, T.; et al. Reliability-Aware Design of Metal/High-k Gate Stack for High-Performance SiC Power MOSFET. In Proceedings of the 2017 29th International Symposium on Power Semiconductor Devices and IC's (ISPSD); 2017; pp. 247–250.
182. Nagura, T.; Chokawa, K.; Araidai, M.; Hosoi, T.; Watanabe, H.; Oshiyama, A.; Shiraiishi, K. First-Principles Calculations of the Effect of Incorporating Hf Atoms in AlON Gate Dielectrics of Wide-Bandgap-Semiconductor Power Devices on the Hole Leakage Current. In Proceedings of the Extended Abstracts of the 2018 International Conference on Solid State Devices and Materials; The Japan Society of Applied Physics: Hongo Campus, The University of Tokyo, Tokyo, Japan, September 13 2018.
183. Manchanda, L.; Lee, W.H.; Bower, J.E.; Baumann, F.H.; Brown, W.L.; Case, C.J.; Keller, R.C.; Kim, Y.O.; Laskowski, E.J.; Morris, M.D.; et al. Gate Quality Doped High K Films for CMOS beyond 100 Nm: 3-10 Nm Al₂O₃ with Low Leakage and Low Interface States. In Proceedings of the International Electron Devices Meeting 1998. Technical Digest (Cat. No.98CH36217); IEEE: San Francisco, CA, USA, 1998; pp. 605–608.
184. Komatsu, N.; Masumoto, K.; Aoki, H.; Kimura, C.; Sugino, T. Characterization of Si-Added Aluminum Oxide (AlSiO) Films for Power Devices. *Applied Surface Science* **2010**, *256*, 1803–1806, doi:10.1016/j.apsusc.2009.10.009.
185. Chan, S.H.; Tahhan, M.; Liu, X.; Bisi, D.; Gupta, C.; Koksaldi, O.; Li, H.; Mates, T.; DenBaars, S.P.; Keller, S.; et al. Metalorganic Chemical Vapor Deposition and Characterization of (Al,Si)O Dielectrics for GaN-Based Devices. *Jpn. J. Appl. Phys.* **2016**, *55*, 021501, doi:10.7567/JJAP.55.021501.
186. Gupta, C.; Chan, S.H.; Agarwal, A.; Hatui, N.; Keller, S.; Mishra, U.K. First Demonstration of AlSiO as Gate Dielectric in GaN FETs; Applied to a High Performance OG-FET. *IEEE Electron Device Lett.* **2017**, *38*, 1575–1578, doi:10.1109/LED.2017.2756926.
187. Sayed, I.; Liu, W.; Georgieva, J.; Krishna, A.; Keller, S.; Mishra, U.K. Characterization of AlSiO Dielectrics with Varying Silicon Composition for N-Polar GaN-Based Devices. *Semicond. Sci. Technol.* **2020**, *35*, 095027, doi:10.1088/1361-6641/ab9ecb.
188. Kikuta, D.; Itoh, K.; Narita, T.; Mori, T. Al₂O₃/SiO₂ Nanolaminate for a Gate Oxide in a GaN-Based MOS Device. *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films* **2016**, *35*, 01B122, doi:10.1116/1.4971399.

189. Ito, K.; Kikuta, D.; Narita, T.; Kataoka, K.; Isomura, N.; Kitazumi, K.; Mori, T. Band Offset of $\text{Al}_{1-x}\text{Si}_x\text{O}_y$ Mixed Oxide on GaN Evaluated by Hard X-Ray Photoelectron Spectroscopy. *Jpn. J. Appl. Phys.* **2017**, *56*, 04CG07, doi:10.7567/JJAP.56.04CG07. 1169 1170
190. Kikuta, D.; Ito, K.; Narita, T.; Kachi, T. Highly Reliable AlSiO Gate Oxides Formed through Post-Deposition Annealing for GaN-Based MOS Devices. *Appl. Phys. Express* **2020**, *13*, 026504, doi:10.7567/1882-0786/ab658a. 1171 1172
191. Ito, K.; Tomita, K.; Kikuta, D.; Horita, M.; Narita, T. Analysis of Channel Mobility in GaN-Based Metal-Oxide-Semiconductor Field-Effect Transistors. *Journal of Applied Physics* **2021**, *129*, 084502, doi:10.1063/5.0040700. 1173 1174
192. Chokawa, K.; Narita, T.; Kikuta, D.; Shiozaki, K.; Kachi, T.; Oshiyama, A.; Shiraishi, K. Absence of Oxygen-Vacancy-Related Deep Levels in the Amorphous Mixed Oxide $(\text{Al}_2\text{O}_3)_{1-x}(\text{SiO}_2)_x$: First-Principles Exploration of Gate Oxides in GaN -Based Power Devices. *Phys. Rev. Applied* **2020**, *14*, 014034, doi:10.1103/PhysRevApplied.14.014034. 1175 1176 1177
193. Dicks, O.A.; Cottom, J.; Shluger, A.L.; Afanas'ev, V.V. The Origin of Negative Charging in Amorphous Al_2O_3 Films: The Role of Native Defects. *Nanotechnology* **2019**, *30*, 205201, doi:10.1088/1361-6528/ab0450. 1178 1179
194. Guo, Z.; Ambrosio, F.; Pasquarello, A. Oxygen Defects in Amorphous Al_2O_3 : A Hybrid Functional Study. *Appl. Phys. Lett.* **2016**, *109*, 062903, doi:10.1063/1.4961125. 1180 1181
195. Chokawa, K.; Shiraishi, K.; Oshiyama, A. Defect-Free Interface between Amorphous $(\text{Al}_2\text{O}_3)_{1-x}(\text{SiO}_2)_x$ and GaN(0001) Revealed by First-Principles Simulated Annealing Technique. *Appl. Phys. Lett.* **2021**, *119*, 011602, doi:10.1063/5.0047088. 1182 1183
196. Hu, Q.; Hu, B.; Gu, C.; Li, T.; Li, S.; Li, S.; Li, X.; Wu, Y. Improved Current Collapse in Recessed AlGaIn/GaN MOS-HEMTs by Interface and Structure Engineering. *IEEE Trans. Electron Devices* **2019**, *66*, 4591–4596, doi:10.1109/TED.2019.2940749. 1184 1185
197. Li, S.; Hu, Q.; Wang, X.; Li, T.; Li, X.; Wu, Y. Improved Interface Properties and Dielectric Breakdown in Recessed AlGaIn/GaN MOS-HEMTs Using HfSiO_x as Gate Dielectric. *IEEE Electron Device Lett.* **2019**, *40*, 295–298, doi:10.1109/LED.2018.2888486. 1186 1187
198. Nabatame, T.; Maeda, E.; Inoue, M.; Yuge, K.; Hirose, M.; Shiozaki, K.; Ikeda, N.; Ohishi, T.; Ohi, A. Hafnium Silicate Gate Dielectrics in GaN Metal Oxide Semiconductor Capacitors. *Appl. Phys. Express* **2019**, *12*, 011009, doi:10.7567/1882-0786/aaf62a. 1188 1189
199. Ochi, R.; Maeda, E.; Nabatame, T.; Shiozaki, K.; Sato, T.; Hashizume, T. Gate Controllability of HfSiO_x /AlGaIn/GaN MOS High-Electron-Mobility Transistor. *AIP Advances* **2020**, *10*, 065215, doi:10.1063/5.0012687. 1190 1191
200. Miyazaki, S.; Ohta, A. (Invited) Photoemission-Based Characterization of Gate Dielectrics and Stack Interfaces. *ECS Trans.* **2019**, *92*, 11–19, doi:10.1149/09204.0011ecst. 1192 1193
201. Dutta Gupta, S.; Soni, A.; Joshi, V.; Kumar, J.; Sengupta, R.; Khand, H.; Shankar, B.; Mohan, N.; Raghavan, S.; Bhat, N.; et al. Positive Threshold Voltage Shift in AlGaIn/GaN HEMTs and E-Mode Operation By $\text{Al}_x\text{Ti}_{1-x}\text{O}$ Based Gate Stack Engineering. *IEEE Trans. Electron Devices* **2019**, *66*, 2544–2550, doi:10.1109/TED.2019.2908960. 1194 1195 1196
202. Nguyen, D.D.; Suzuki, T. Interface Charge Engineering in AlTiO/AlGaIn/GaN Metal–Insulator–Semiconductor Devices. *Journal of Applied Physics* **2020**, *127*, 094501, doi:10.1063/1.5141399. 1197 1198
203. Nguyen, D.D.; Isoda, T.; Deng, Y.; Suzuki, T. Normally-off Operations in Partially-Gate-Recessed AlTiO/AlGaIn/GaN Field-Effect Transistors Based on Interface Charge Engineering. *Journal of Applied Physics* **2021**, *130*, 014503, doi:10.1063/5.0054045. 1199 1200
204. Dutta Gupta, S.; Joshi, V.; Roy Chaudhuri, R.; Shrivastava, M. Observations Regarding Deep-Level States Causing p-Type Doping in AlTiO Gate and Positive Threshold Voltage Shift in AlGaIn/GaN High Electron Mobility Transistors. *Journal of Applied Physics* **2021**, *130*, 015701, doi:10.1063/5.0053982. 1201 1202 1203 1204 1205