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Control of Interface Anisotropy for Spin Transfer Torque in Perpendicular Magnetic Tunnel Junctions for Cryogenic Temperature Operation

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The possibility of higher electrical efficiency in computing by operating at low temperatures raises the need for non-volatile memory cells optimized for cryogenic operation. We report a study on low temperature spin transfer torque switching of magnetic tunnel junctions with 20 to 100nm in diameter with thermal stability adapted to low temperature operation. The evolution of magnetic and electrical properties are characterized for four different stacks from 300K to 10K comprising insertions of Mg, Ru and permalloy (Py) in the storage layer to reduce its effective anisotropy. Two figures of merit are used to compare different devices and stacks, Δ/I_c and Δ/E_{sw} , normalizing the thermal stability Δ by the critical current or switching energy. Devices with a Py insertion layer show a higher FOM ($3.78k_B T_{op}/\mu A$) and switching energy E_{sw} below 655fJ for 100ns pulses at $T_{op} = 10K$. A procedure to optimize the reference layer stray field was also implemented to achieve full compensation using a synthetic antiferromagnetic layer for 20nm diameter devices.

I. INTRODUCTION

Spin transfer torque perpendicular anisotropy magnetic tunnel junctions (STT-pMTJ) are of particular interest for low temperature application due to their scalability, non-volatility and the possibility to adjust the retention of the cell to a given operating temperature¹². In the context of high performance computing (HPC)³, it can be envisioned that STT-pMTJ capable of cryogenic operation at 77K as well as 4K⁴⁵⁶⁷ would provide a non-volatile memory solution adapted for more energy efficient computing in these cryogenic environments.

Besides, in the context of quantum technologies, cryoelectronic components are needed to control Qbits. For these applications including possible interfaces with Qbits, the first obstacle for integration is the power dissipation of the memory. The typical dilution refrigerators available have a cooling power in the range of a few dozen μW to a few hundred μW , operating from 20mK to 120mK. Therefore, current MRAM development must achieve higher electrical efficiency of the write process to become compatible with the expected refrigeration cooling powers of these deep-cryogenic systems⁸⁹.

Compared to other non-volatile memory technology such as Phase Change RAM (PCRAM) or Resistive oxide RAM (RRAM), STT-MRAM have the advantage of not relying on a local heating of the cells during write which would be detrimental for low temperature operation. Besides, an important asset of STT-pMTJ at cryogenic temperatures is the possibility to reduce the write energy by reducing the switching barrier height while maintaining a sufficient memory retention at low temperature. Indeed, successful writing requires overcoming an energy barrier E_b providing the information retention. This is achieved by applying a spin polarized current to reverse the storage layer magnetization thanks to spin transfer, which changes the relative magnetic configuration between the storage and reference layers, either parallel or anti-parallel. Due to the reduction of the thermal activation energy $k_B T_{op}$ by at least an order of magnitude between 300K and 10K, the energy barrier E_b can be reduced by the same factor while still retaining the equivalent stability Δ as for a room-temperature

operation. Here T_{op} is the operating temperature at which the stability is measured.

The focus of this study is to enhance the performance of pMTJ devices at low temperatures by exploring different storage layer compositions to reduce its perpendicular magnetic anisotropy. This is achieved by adding insertion layers that will change the effective anisotropy K_{eff} , thus modulating the thermal stability Δ , the critical switching current I_c and switching energy E_{sw} , which are essential parameters for a storage component.

These three quantities will increase as the temperature T is reduced due to the enhancement of the surface anisotropy K_s and magnetization saturation M_s . As such, engineered pMTJs must account for the increase in K_{eff} at low temperatures, which can be achieved by using storage layers having lower perpendicular anisotropy that in STT-MRAM operating at room temperature, such that their blocking temperature T_b is typically below 200K. The blocking temperature is defined as the temperature at which coercivity drops to zero $H_c(T_b) = 0$ for a the characteristic time of the measurement. A qualitative assessment of E_b can be made using the relationship $T_b \propto E_b$ that arises from the thermally-assisted barrier crossing model¹⁰.

II. EXPERIMENT

The fabricated nanopillars are made with an out-of-plane magnetized FeCoB storage layer with the following reference layer electrode and tunnel barrier structure: W(0.3)/FeCoB(1)/Mg(0.8)/Ox(30s)/Mg(0.5), where numbers are the layer thickness in nm. The tunnel barrier consists of naturally oxidized Mg under 30 μ bar, and Ox represents the duration in seconds of the natural oxidation by O₂ pressure exposure. Four different storage layer structures were investigated in this study, referenced and described as follows, using the abbreviation Py for a Ni₈₀Fe₂₀ permalloy layer :

- Reference (Ref): FeCoB(1.1-1.8)/W(2)

- Mg: Mg(0.9-1.9)/FeCoB(0.9-1.9)/W(2)
- Ru: FeCoB(1.2-1.5)/Ru(0.1-0.2)/W(2)
- Py: FeCoB(0.6-1.4)/W(0.2)/Py(0.4-0.8)/W(2)

The three insertion stacks (Mg, Ru, Py) were chosen so that the PMA of the storage layer could be reduced. The Mg wedge on the interface between the tunnel barrier and the Fe-CoB layer has the role of modulating the oxidation state of the interface in which PMA arises, as the conditions of natural oxidation are the same for all devices on this sample. The Py insertion was chosen based on previous work by Jyotirmoy Chatterjee who measured the effects of different insertion layers on the surface anisotropy K_S and magnetization saturation M_S ¹¹. The Py stack was the sample with the lowest K in this study, which would provide the lowest PMA. For the Ru sample, it has been shown that using it as a capping layer can reduce the anisotropy of the storage layer to become easy-plane at room temperature¹². That strategy seemed a promising alternative to shift the blocking temperature to lower values.

The FeCoB and the insertions of Mg, Ru and permalloy, are deposited by physical vapor deposition (sputtering) with a layer thickness wedge. Their thickness range across the wafer is indicated in nm. The tunnel junction stack is a bottom reference structure, using a synthetic antiferromagnetic layer (SAF) of $[Co/Pt]_{\times 6}/Ru/[Co/Pt]_{\times 3}/Co(0.5)$ to stabilize the reference layer magnetization. They are processed into circular area MTJs with nominal diameters ranging from 20 to 100nm using e-beam lithography, reactive ion etching (RIE) and ion beam etching (IBE) steps after annealing at 300C for 10min.

The devices were initially magnetically characterized by measuring field dependent hysteresis loops, shown in Fig. 1. The offset field of 400 Oe measured at 80K of the field loop is ascribed to the stray field from the SAF reference layer which is not completely compensated. The resulting stray field will also depend on temperature. As the storage layer is engineered to have low anisotropy at low temperatures, and therefore low coercivity, the presence of an offset field becomes a limitation on how much the effective perpendicular anisotropy (PMA) can be reduced, since a bi-stable state at zero field is the main requirement for memory operation. Even a reduced stray field will result in different retentions of the parallel and antiparallel configurations and in an asymmetry of the STT switching voltage requiring larger currents for switching. To eliminate any requirements for external field compensation during operation, the SAF structure needs to be adjusted for low stray field. This issue can be corrected by properly optimizing the SAF, which is discussed in more details in section V.

For electrical characterization of the STT reversal, voltage dependent hysteresis loops were also measured, as shown in Fig. 1b. These loops and the corresponding switching probability after each voltage pulse are used to extract the critical switching voltages and stability (figure 1c). This particular device shows a TMR of 50% at 200K and 84% at 10K for a blocking temperature $T_b = 180K$. For the various compositions, the measured mean TMR is 85, 102, 53 and 53% at

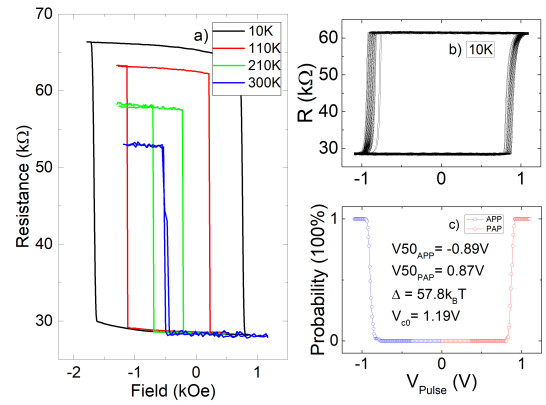


FIG. 1. Magnetic and electrical measurements for a device of the Mg stack with $t_{FeCoB} = 1.5\text{nm}$, $t_{Mg} = 0.9\text{nm}$ and 18nm of diameter. a) Field hysteresis loops for 10, 110, 210 and 300K. b) STT voltage loops for the same device at 10K, showing the switching distribution. c) Switching probability with voltage and extracted parameters.

10K for stacks Ref, Mg, Ru and Py, respectively. The drop in TMR for Ru and Py may be attributed to a poorer crystallographic structure associated with bcc/fcc structural competition or insufficient B removal from FeCoB upon annealing. The switching properties were characterized by applying 100ns voltage pulses with sweeping pulse amplitude up to 1.0V, while measuring the device resistance at a DC bias of 30mV.

By acquiring voltage loops at different applied fields, we can obtain the pulse phase diagrams shown in Fig. 2. The diagrams are shown for a device of the Mg insertion stack of 26nm diameter, as calculated from the parallel electrical resistance $R_p = 13k\Omega$, assuming an RA value of $7.1\Omega\mu\text{m}^2$. It shows the evolution of the STT switching behaviour down to 40K. We can extract from the diagrams the STT conversion efficiency factor $s_{\parallel} = \frac{\hbar}{2e} \frac{\eta}{t_{SL} M_S}$, which is related to the a_{\parallel} damping-like coefficient of the STT term the Laudau-Lifshitz-Gilbert-Slonczewski equation, where η is the polarization.

$$\frac{dm}{dt} = -\gamma(\mathbf{m} \times \mu_0 \mathbf{H}_{eff}) + \alpha(\mathbf{m} \times \frac{d\mathbf{m}}{dt}) - \gamma a_{\parallel}(T, V)[\mathbf{m} \times (\mathbf{m} \times \mathbf{p})] \quad (1)$$

where $a_{\parallel} = s_{\parallel} G_P V_{bias}$, G_P is the conductance of the parallel state, m is the storage layer magnetization, γ is the gyromagnetic ratio, μ_0 is the vacuum permeability, H_{eff} is the effective field, α is the Gilbert damping and p is the reference layer magnetization. According to the macrospin approach, the critical switching current is:

$$I_{c0} = \frac{2e}{\hbar} \frac{t_{SL} \alpha H_{\perp} M_S}{\eta} \quad (2)$$

With an external out-of-plane field H_{\perp} , we get a relationship that results in the linear boundaries of the stability diagram with slopes given by $\frac{dI_{c0}}{dH_{\perp}} = \frac{s_{\parallel}}{\alpha}$ ¹³. From 180K to 10K, the STT efficiency of the parallel to anti-parallel (PAP) transition increases from 2.1 to $2.6kOeV^{-1}$, while for the APP it

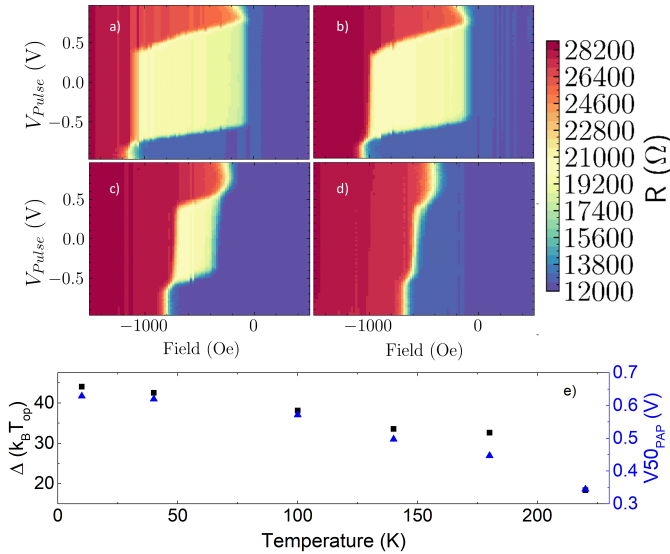


FIG. 2. STT switching phase diagrams of a device of stack Mg with $t_{FeCoB} = 1.43nm$, $t_{Mg} = 1.7nm$ and 26nm in electrical diameter, generated from applying voltage loops as shown in Fig. 1b for different out-of-plane fields at a) 40K, b) 140K, c) 180K and d) 220K. e) Dependence of Δ and $V_{50_{PAP}}$ with temperature.

increases from 1.7 to 5.0 $kOeV^{-1}$. Considering that the damping has been verified as having a very weak dependence with temperature¹⁴ in similar CoFeB layers, $a_{||}$ is enhanced by 24% and by almost a factor of 3, respectively.

We can calculate the switching energy to write this particular device as $E_{sw} = R_p I_c^2 \tau$, where τ is the pulse width. Using the 100% and 50% thresholds of switching probability to extract V_{c0} and $V_{50_{PAP}}$, respectively, we obtain $E_{sw} = 7.1pJ$ and $E_{50_{sw}} = 3.1pJ$, corresponding to a maximum power of $P = 71\mu W$ for 100ns pulses at 10K. The total switching energy can be minimized by further reducing the pulse width, as long as STT switching still occurs for pulse widths higher than the onset of the ballistic reversal regime.

Previous work exploring a larger range of pulse widths to characterize the switching¹⁴ reported $V_{50_{PAP}} \approx 0.5V$ for the same bit error rate used in this work, 50 voltage loops. Considering the same pulse width of 100ns, it results in $E_{50_{sw}} \approx 34.7pJ$ and $P \approx 347\mu W$. Compared to these literature reference, our reported devices represent an improvement of almost one order of magnitude.

III. ANALYSIS OF FIGURE OF MERIT

As all devices studied have different compositions and sizes, we used two figures of merit to compare them, which can be defined as follows: $FOM_1 = \Delta/I_c$ and $FOM_2 = \Delta/E_{sw}$. Where Δ being the thermal stability factor in units of $k_B T_{op}$. The first merit is relevant to the cell dimensions, since the associated selection transistor needs to deliver the current required for switching, while the second figure of merit is a measure of the overall STT switch efficiency, for a given retention

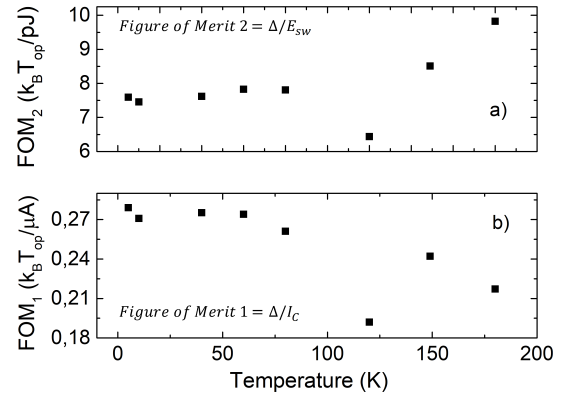


FIG. 3. Extracted electrical parameters for a device of stack Mg with $t_{FeCoB} = 1.53nm$, $t_{Mg} = 0.88nm$, 64nm in diameter and $R_p = 2.2k\Omega$. Dependence of a) FOM_2 and b) FOM_1 with temperature.

of each cell. The switching voltage values used to calculate all figures of merit in this work correspond to the 50% threshold of the PAP reversal, representing the larger amplitude of the two threshold voltages.

The improvement of Δ , reported in Fig. 2e, seems to be limited as the temperature is reduced below 100K. This might be explained by the fact that at low temperature, self-heating effects may become significant, affecting the real temperature of the device. Indeed, the values of Δ are reported based on the switching voltage dispersion, i.e. while current is applied possibly increasing the device temperature during the pulse application. This would explain the limited apparent increase in thermal stability, contrary to what is expected from both macrospin and domain wall reversal models⁵. It would also explain the reduction in the figure of merit resulting from a switching current increase without any corresponding thermal stability gain. This deviation is likely to be more pronounced at $T < 100K$ due to a strong reduction of the heat capacity of the device between 100K and 1K¹⁵, meaning that joule heating will be significant. This then results in the figure of merit flattening with decreasing temperature, as shown in Fig. 3b where it stabilizes for $T < 80K$. Consequently, there is a limited enhancement on FOM_1 of 28% and a reduction on FOM_2 of 29.4%, as the thermal stability factor does not increase as fast as I_c^2 between 180K and 10K.

IV. STACK COMPARISON

Across all four stacks, 27 devices in total were measured at 10K and their figures of merit are extracted and compared between different samples. Figure 4a shows the dependence of H_c normalized with temperature, which gives us the blocking temperature for devices of different stacks; Py: 45K, Ru:150K, Mg:230K and Ref:300K. These values will change within a range of ≈ 50 to 100K depending on the thickness of the storage layer and its area, but only Py based pillars showed $T_b < 50K$. Fig. 4b shows the dependence of FOM_1 with diameter, which increases for smaller pillar diameters. Assuming that the STT critical current density is constant, the current

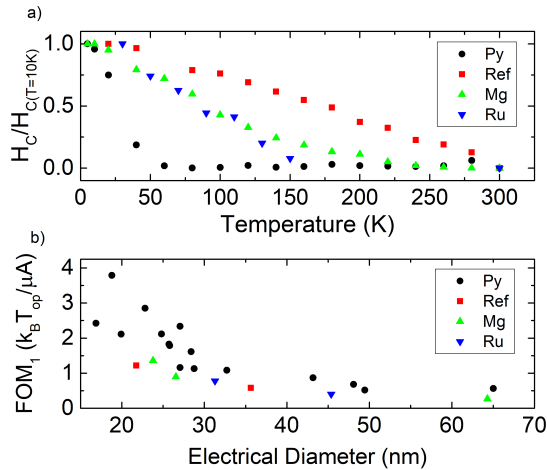


FIG. 4. Comparison of all measured devices across the four different stacks measured at 10K. a) Dependence of H_C with T for the four different stacks, showing the change in blocking temperature with maximum coercivity of 442, 952, 270 and 555 Oe for Py, Ref, Ru and Mg, respectively. b) Dependence of FOM_1 with electrical diameter.

required for switching would decrease as $1/D^2$, which is in general agreement with the limited data set presented here.

Interestingly we see that the Py insertion sample outperforms all other MTJ variants, meaning that STT is a few times more efficient for this particular composition, with FOM_1 going from 0.36 in an Mg device to 3.78 in a Py device, representing a tenfold maximum increase. This could be attributed to the lower M_S of Py and lower damping¹⁶. Another interesting point is that larger TMR is not directly correlated with a higher figure of merit FOM_1 , as the Py devices have on average lower TMR values, around 53%, while for the reference stack Ref, TMR is 85%. The higher figure of merit of the Py sample despite lower TMR, can be understood from the fact that the spin torque polarization depends on the square-root of the TMR,¹⁷ $\eta \propto \sqrt{TMR}$, while the critical current is directly proportional to M_S , $I_c \propto \alpha M_S$. For the Py sample overall, the lower M_S and Gilbert damping values, as reported in previous work⁴, more than compensate the STT efficiency loss from the lower TMR values.

The device of highest FOM_1 of the array in Fig. 4, corresponds to a junction of 18.8nm electrical diameter and $R_p = 71k\Omega$, with a switching energy $E_{50_{sw}} = 655 fJ$ for 100ns pulses as measured at 10K, corresponding to an order of magnitude in improvement over the best estimate in section II. This corresponds to a power of $7.1\mu W$ with switching voltages $V_{c0} = 0.95V$ and $V_{50_{PAP}} = 0.63V$. The switching energy can be reduced by using shorter pulses, as long as gains from the shorter pulse length τ are not negated by the expected increase of voltage amplitude as $1/\tau$, as is the case for the ballistic reversal regime.

V. SAF STRAY FIELD COMPENSATION

As mentioned previously, the measured devices show a high stray field from the reference SAF layer structure. For the reported samples, the reference layer structure corresponds to a first block of Co/Pt bi-layers repeated 6 times, which is antiferromagnetically coupled through a Ru spacer to a second block with 3 Co/Pt bi-layers. To achieve a better SAF compensation at the storage layer level, we fabricated a reference layer stack with a modified SAF structure, using Co/Pt blocks of 6 and 2 repetitions, while also including a wedge on the reference layer FeCoB, at the interface with the MgO barrier. Figure 5 shows a plot of the stray field as function of the FeCoB layer thickness, for devices of 20nm nominal diameter annealed at 300C for 10min, fabricated using the same process flow as the above reported devices.

The stray field H_{stray} varies linearly with the FeCoB layer thickness, in accordance with earlier macrospin calculations that establish the linear dependence with the magnetic moment ratio m_2/m_1 , m_1 and m_2 being the magnetic moments of the top and bottom SAF blocks¹⁸, respectively. Considering that the only layer thickness variation on the SAF stack is the FeCoB layer thickness, then the ratio of the moments is inversely proportional to the FeCoB layer thickness. A linear fit of the data provides the expected FeCoB ($\approx 1nm$) layer thickness required to achieve full compensation of the reference layer. A dispersion of $\pm 50Oe$ in stray field values is due to variability of cell diameter across the wafer, as the SAF compensation thickness depends on the actual cell diameter, the moment ratio increasing as the diameter is decreased. This procedure provides a simple optimization of the SAF structure to ensure that at the expected operating temperature, the device will indeed be able to operate as a memory with 2 bistable states at zero field, with the additional requirement that the device coercivity must be larger than the stray field variability, $H_c > 50Oe$ in this case.

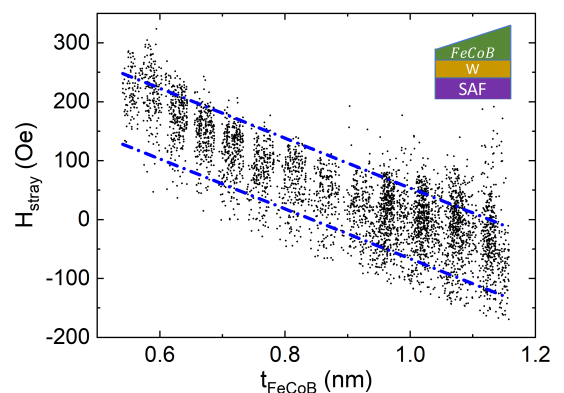


FIG. 5. Stray field dependence with the FeCoB reference layer thickness. The critical thickness of $\approx 1nm$ gives us a mean of zero offset and a dispersion of $\pm 50Oe$.

VI. CONCLUSIONS

This work shows pMTJ efficient STT writing at 10K, by reducing the effective anisotropy of the storage layer using thin material insertions adjacent to the FeCoB layer. Comparing a low anisotropy reference with other stacks including Mg, Ru and permalloy insertions shows that a higher figure of merit and reduced energy consumption for writing can be achieved for the permalloy insertion devices. The improvements can be attributed to the lower M_s and damping of the modified storage layer. A further improvement, almost by a factor of 4, in the figure of merit is possible through the reduction of the pillar diameter from 35nm to below 20nm.

Achieving a minimal switching energy is possible using shorter pulse widths, but this requires a detailed study to verify the onset of STT ballistic reversal.

ACKNOWLEDGMENTS

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DATA AVAILABILITY STATEMENT

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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