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Full-SiC Single-Chip High-Side and Low-Side Dual-MOSFET for Ultimate Power Vertical Integration – Basic Concept and Technology

Ralph Makhoul^(1,2), Nour Beydoun⁽³⁾, Abdelhakim Bourennane⁽¹⁾, Luong Viêt Phung⁽²⁾, Mihai Lazar⁽³⁾, Frédéric Richardeau⁽⁴⁾, Philippe Godignon⁽⁵⁾, Dominique Planson⁽²⁾, Hervé Morel⁽²⁾, David Bourrier⁽¹⁾

⁽¹⁾LAAS-CNRS, Université de Toulouse, CNRS, UPS, Toulouse, France

⁽²⁾Ampère, Univ Lyon, INSA Lyon, Université Claude Bernard Lyon 1, Ecole Centrale de Lyon, CNRS, Ampère, UMR5005, 69621 Villeurbanne, France

⁽³⁾Light, nanomaterials, nanotechnologies, Université technologique de Troyes & CNRS EMR 7004, 12 rue Marie Curie, 10004 Troyes, France

⁽⁴⁾LAPLACE, Université de Toulouse, CNRS, INPT, UPS, Toulouse, France

⁽⁵⁾IMB-CNM, Campus UAB (08193) Bellaterra, Spain

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Keywords

« Switching cell », « SiC MOSFET », « Device integration », « Device modelling », « Device simulation ».

Abstract

A full monolithic integration in multi-terminal SiC dies of a generic H-bridge power converter (800V/10A) consisting of dual N-type vertical MOSFET switches within only two multi-terminal chips is proposed. Innovative two multi-terminal monolithic power SiC-chips are introduced and studied by 2D Sentaurus™ simulations. The first one integrates the high-side row switches of the bridge and the second one integrates the low-side row switches. Static and dynamic operating modes were validated through 2D-Mixed-Mode simulations. Main new process bricks allowing back-side insulating trenches based on plasma combined with photo-electrochemical etching are experimentally evaluated for the first time on power device SiC wafer.

Introduction

With the significant improvement in performance of SiC power VDMOS and their widespread adoption in the field of critical applications such as electric vehicles and railway, there is today a growing interest for the monolithic integration of dedicated power conversion functions in SiC dies [1]. Power converters are generally realized using Vertical Double diffused MOSFET (VDMOS) bare chips that are bonded on a power substrate and interconnected to each other using multiple bond wires. These latter require an expensive and time-consuming wiring operation and are source of aging problems. Moreover, the stray inductance of wire bonds limits the turn-off switching speed and increases losses of the converter using wide-bandgap devices. To overcome these drawbacks, the power converter can be realized using a minimum number of multi-terminal chips, that integrate monolithically the VDMOS switches, and a dedicated packaging 2D partial flip-chip on DBC/IMS substrate process. However, due to the chip size limitations, monolithic integration in multi-terminal dies is nowadays limited to low current ratings.

In previous works, the monolithic integration of power converters for medium power converters was applied to the case of converters consisting of silicon RC-IGBT switches [2] and permitted the proposition of new and original concepts of multi-terminal chips that involve the two-chip [3], three-chip [4] and finally the ultimate full monolithic single chip-converter [3].

In silicon carbide, few works were however reported on the monolithic integration of power functions built around the VDMOS. Furthermore,

most of them mainly focused on the monolithic integration of auxiliary low voltage functions within a single high voltage VDMOS. Indeed, one can find the P-Well monolithic functionalization of a series normally-on cascode JFET current limiter [5], integration of auto-adjust JFET with VDMOS [6], integration of VDMOS with a CMOS gate buffer [7]. In the category of monolithic bidirectional switches, on SiC material, two vertical common drain-type VDMOS switches was recently reported in literature [8-10].

This article focuses on the innovative full monolithic integration of H-bridge high-side row chip common drain-type and low-side row chip common source-type, consisting of SiC VDMOS switches. The article is organized as follows: first of all, the basic concept of the monolithic integration in two multi-terminal chips is presented; then, the operating modes, off-state, on-state and switching, were validated through 2D TCAD Sentaurus™ Mixed-Mode simulations; after that, in order to provide the vertical insulation of the source-type chip a mandatory specific technological process brick was set-up for etching of back-side thick SiC wafer. It combines Inductively Coupled Plasma - Reactive Ion Etching (ICP-RIE) process and UV laser Photo-electrochemical (PEC) process; finally, a conclusion is suggested covering the conceptual and technological sections proposed in this article.

Principle of the single-chip high-side row and low-side row monolithic dual VDMOSFET

The power converter circuit is divided into two distinct and separate blocks as shown in Fig. 1 (a). The high-side row is composed of quasi-parallel connected VDMOS devices that share the same drain-side electrode. These VDMOS devices can be integrated quasi directly in a “common-drain” multi-terminal SiC power chip sharing their SiC bulk and epi-layer parts. The low-side is also composed of quasi-parallel connected VDMOS devices that share the same source-side electrode. This second chip is much more complex to develop as it requires a deep vertical insulating region that must be realized by etching a thick in back-side SiC substrate. A judicious packaging on DBC/IMS substrate of these two multi-terminal power chips using partial flip-chip

connection make possible the realization of low stray inductance multi-phase power converter.

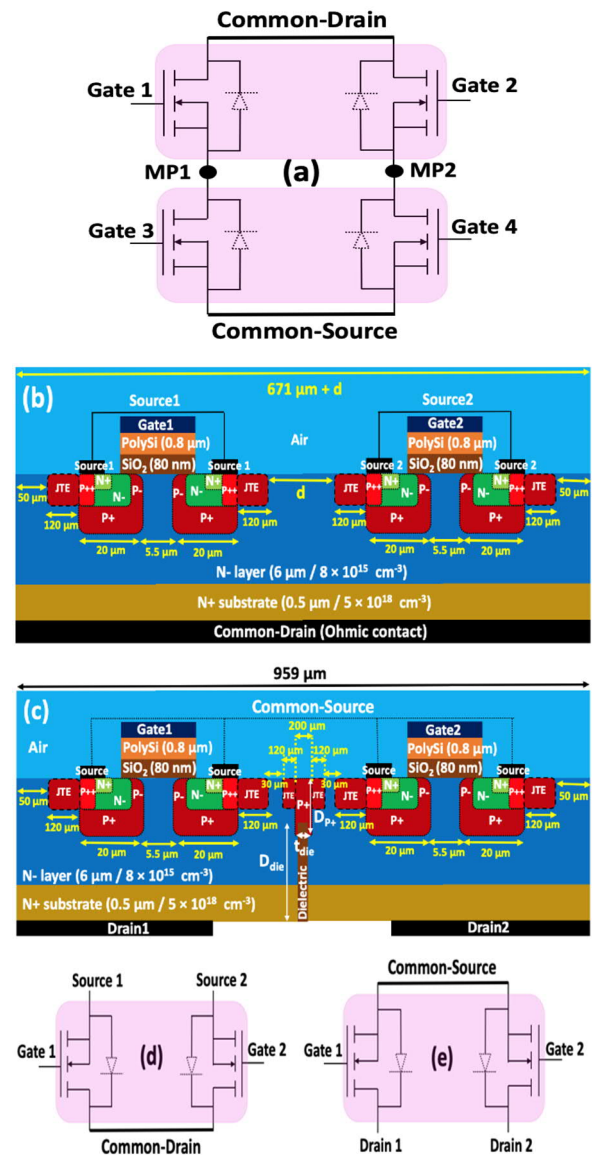


Fig. 1: (a) Half-bridge using N-type VDMOS devices, (b) Cross-sectional principle of the Common-Drain type structure (high-side row), (c) Cross-sectional principle of the Common-Source type structure (low-side row), (d) Common-Drain simplified equivalent electrical circuit, (e) Common-Source simplified equivalent electrical circuit.

Each of the two three-terminal proposed design are sketched in Fig. 1 (b) and (c) which are composed of two VDMOS sections. The common drain chip as well as the common source chip taken separately constitute half of a switching cell. The two VDMOS sections, in each power chip, can be in on-state or off-state. In off-state, the VDMOS within the multi-terminal chip must support the applied voltage. The design of these

chips has also to minimize the electrical interactions between the two VDMOS sections due to the extension of the lateral Space Charge Region (SCR).

The front-side of each three-terminal device is composed of MOS sections and lightly doped P-diffusions (JTE termination). The back-side of the two three-terminal power chips are composed of thick N^+ substrate. In the common-drain type three-terminal structure, the VDMOS sections share an N^- drift region which is sufficiently thick to support the applied 800 V. The optimization of the separation distance is carried-out using 2D simulations under SentaurusTM. The common source-type structure requires a mandatory insulation region between the two NVDMOS sections. This is achieved by a combination of a frontside P^+ well and a backside deep trench filled by a dielectric. Experimental results on the technological realization of this trench is provided by L2n (Light, nanomaterials, nanotechnologies) laboratory and its platform.

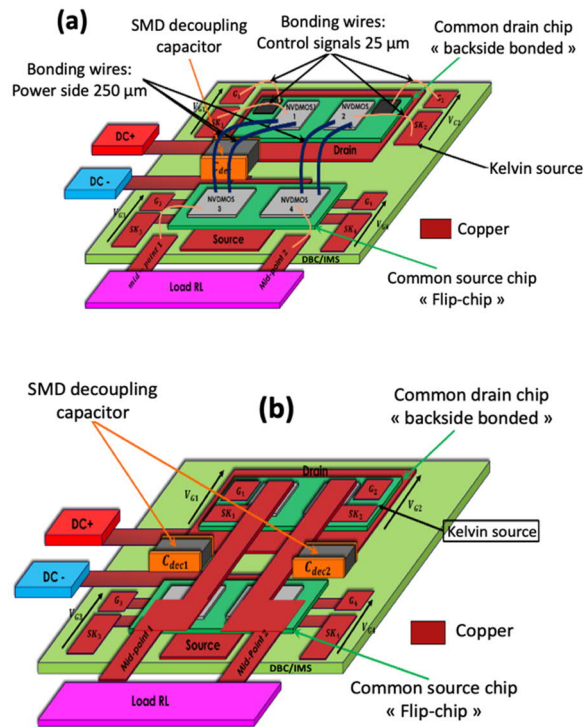


Fig. 2: Top view of the H-bridge on the SMI/DBC substrate using partial flip-chip technique: (a) with SiC chips backside bonded on the FR4 substrate, (b) wire bonds are replaced by copper tracks.

A judicious packaging on DBC/IMS substrate of these two multi-terminal power chips using partial flip-chip connection make possible the

realization of low stray inductance multi-phase power converter. Fig. 2 illustrates the two possible packaging of the two proposed multi-terminal chips. In Fig. 2 (a), the high-side row multi-terminal chip is directly bonded by its backside on a DBC/IMS substrate [3]. However, the low-side row multi-terminal chip is advantageously flipped and is bonded by its source side as previously proposed [11-12]. In this configuration the switching loop is not planar-type as in a standard drain-side soldering packaging but orthogonal-type with a lowering loop area. A windowed insulating Kapton layer is placed between the flipped SiC chip and the DBC/IMS substrate. For the sake of illustration, the assembly of Fig. 2 (a) makes use of bonding wires while the assembly of Fig. 2 (b) makes use of direct copper-bars bonded on the power electrodes [19]. In Fig. 2 (b) using wider and thinner copper tracks plated close to the substrate. This latter permit reducing the loop area and the stray inductance. Moreover, in this latter, the mid-point voltage variations, dv/dt during switching, does not occur on the surface of the IMS/DBC substrate that radically reduces the common-mode current leakage at the turn-on dv/dt .

2D SentaurusTM simulations of the single-chip high-side row and low-side row monolithic dual VDMOSFET

The proposed three-terminal chips were studied using 2D TCAD SentaurusTM simulations [13]. The active area of each VDMOS section in Fig. 1 is 5 mm^2 . The monolithic three-terminal chips have to support the applied voltage both vertically and laterally at the upper-side of the chip, and to carry a nominal current of 10 A. The proposed vertical monolithic integrated devices should support between 600 and 800 V voltage and carry a nominal current of 10 A at 300 K.

The physical and geometrical parameters of the VDMOS illustrated in Fig. 1 were imposed by the CNM laboratory (Centro Nacional de Microelectrónica) process flow, an experienced and recognized technology center in Europe for SiC technology for more than twenty years and in particular in SiC MOSFETs [14].

A. Common-Drain three-terminal power chip

Fig. 1 (b) represents the 2D cross-sectional view of the elementary common-drain type three-terminal power chip. Fig. 3 shows the equivalent

electrical schematic of the common-drain type three-terminal power chip where the VDMOS 2 (V_{G2S2} OFF) is in the OFF-state and the VDMOS 1 in the ON-state (V_{G1S1} ON).

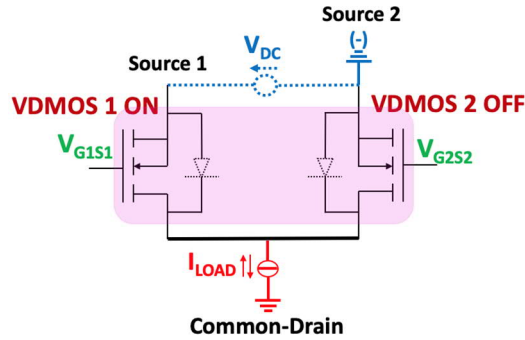


Fig. 3: Equivalent electrical schematic of the common-drain type three-terminal power chip at $V_{DC} = 800$ V, $I_{LOAD} = 10$ A, $V_{G1S1} = 15$ V, $V_{G2S2} = 0$ V, $T_{CASE} = 300$ K.

The first validation study on the common-drain type three-terminal power chip requires to determine the minimum lateral distance "d" to withstand the voltage of 800 V and avoid electrical interaction between the 2 sections of the VDMOS. Fig. 4 represents the variation of the breakdown voltage of the VDMOS 2 which is in the off-state as a function of the distance "d". One can notice that for a distance greater than or equal to 12 μm the three terminal chip is able to withstand the voltage of 800V. Once the VDMOS 2 is in the OFF-state, two space charge regions (SCR) spread out: the first one spreads vertically in the N- layer while the second one spreads out laterally. For the lateral SCR, a distance "d" equal to 12 μm is sufficient to support the applied voltage.

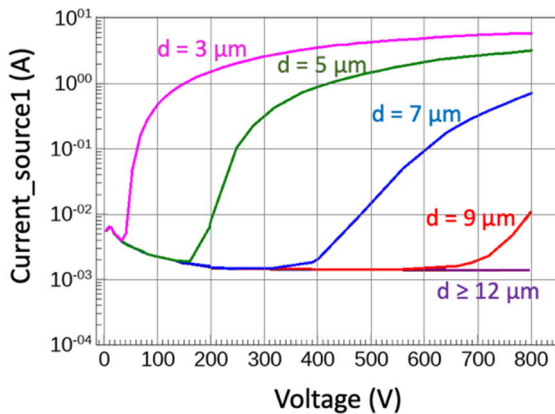


Fig. 4: Variation of the breakdown voltage of the VDMOS 2 as a function of the distance "d".

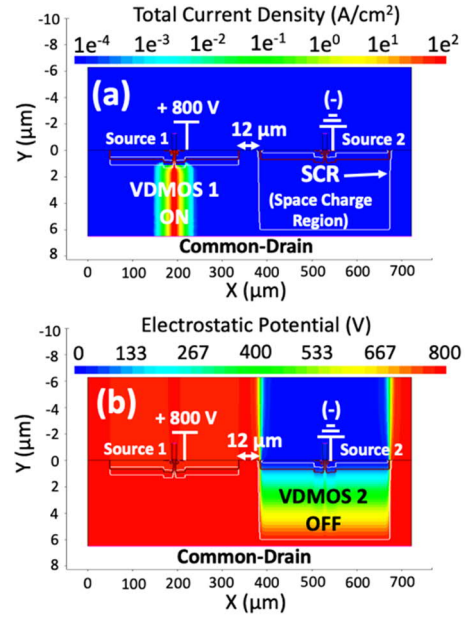


Fig. 5: Equipotential lines and current density distribution in the common-drain type three-terminal power chip (X to Y ratio: 30): (a) VDMOS 1 is in the ON-state, (b) VDMOS 2 in the OFF-state. ($d = 12$ μm) (Leakage current = 6 μA) ($E_{\text{max SiC}} = 2.1$ MV/cm).

Fig. 5 gives the corresponding distribution of equipotential lines and current density within the elementary common-drain type chip. In the case a) we can notice that the VDMOS 1 is in ON-state and carries a current density of 100 A/cm². In the case b) the VDMOS 2 is in OFF-state and withstands 800 V.

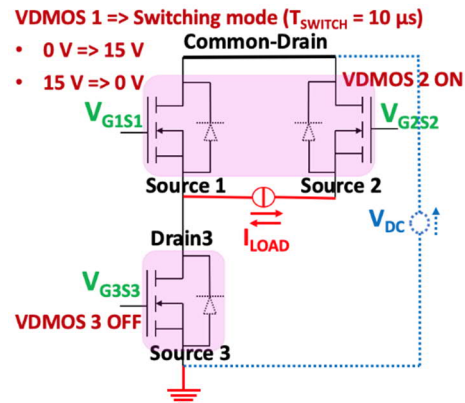


Fig. 6: Equivalent electrical schematic of the common-drain type three-terminal power chip using an additional discrete freewheeling body diode's MOSFET in low-side connection. Such a basic schematic is mandatory to easily put forward switching operation of the proposed common-drain type chip at $V_{DC} = 400$ V, $I_{LOAD} = 10$ A, V_{G1S1} in switching mode ($T_{SWITCH} = 10$ μs), $V_{G2S2} = 15$ V, $V_{G3S3} = 0$ V, $T_{CASE} = 300$ K.

Fig. 6 represents the equivalent electrical schematic of the common-drain type three-terminal power chip.

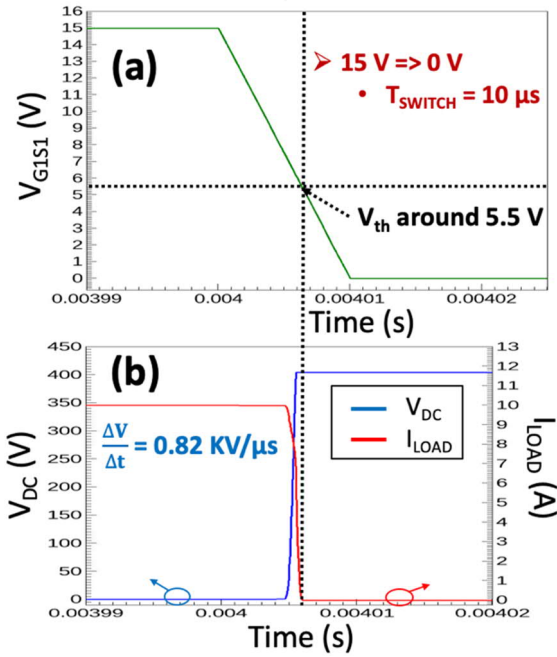


Fig. 7: VDMOS-part switching waveforms of the proposed common-drain type three-terminal power chip ($V_{G2S2} = 15$ V, $V_{G3S3} = 0$ V): (a) V_{G1S1} in switching mode ($T_{SWITCH} = 10$ μ s), (b) $V_{DC} = 400$ V, $I_{LOAD} = 10$ A, $T_{CASE} = 300$ K.

Fig. 7 shows the VDMOS drain-source and gate-source voltage/current waveforms of the of the electrical schematic at turn-off illustrated in Fig. 6. A voltage of 400 V is applied between the Common-Drain and the VDMOS 3. A load current of 10 A is applied between the Source 1 and Source 2. An equivalent trapezoidal shaped waveform is applied to the gate with respect to the source voltage. The voltage value was imposed from 0 to 15 V with a switching time (T_{SWITCH}) of 10 μ s. This switching time was used because we have noticed that it improves the simulations convergence and reduces the simulation time as compared to the case of simulations that use usual switching times that are of the order of a nano-second. From Fig. 7 (a) that shows the VDMOS 1 turn-off, and the drain-source voltage/current waveforms presented in Fig. 7 (b), we have found that the equivalent threshold voltage “V_{th}” is about 5.5 V

B. Common-Source three-terminal power chip

Fig. 1 (c) represents the 2D cross-sectional view of the elementary common-source type three-

terminal power chip. Fig. 6 shows the equivalent electrical schematic of the common-source type three-terminal power chip where the VDMOS 2 (V_{G2S2} OFF) is in the OFF-state and the VDMOS 1 in the ON-state (V_{G1S1} ON).

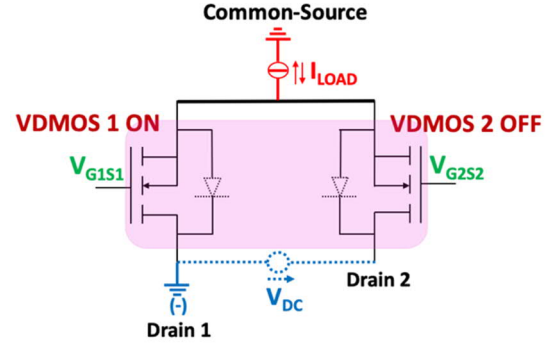


Fig. 8: Equivalent electrical schematic of the common-source type three-terminal power chip at $V_{DC} = 800$ V, $I_{LOAD} = 10$ A, $V_{G1S1} = 15$ V, $V_{G2S2} = 0$ V, $T_{CASE} = 300$ K.

The technological challenge for the realization of the common-source type three-terminal power chip is related to the realization of the full vertical insulation, which combines a deep trench in the backside filled with a dielectric, and a deep P⁺ implementation on the top side above this trench (Fig. 1.c). This insulation is essential to prevent any lateral current flow in both the N⁻ drift layer and the N⁺ substrate between the two VDMOS sections.

The first validation study on the common-source type three-terminal power chip requires to optimize the 3 technological parameters D_{P+} , D_{die} and t_{die} (Fig. 1.c) in order to withstand up to 800 V and prevent any lateral current flow between the two VDMOS sections.

Table I: Influence of “ D_{P+} ” and “ D_{die} ” on the breakdown voltage “ V_{BR} ” of the VDMOS 2. (Leakage current = 6 μ A)

D_{P+} (μ m)	D_{die} (μ m)	V_{BR} (V)
1.5	5.5	800
2.5	4.5	721
3.5	3.5	610
4	3	547
4.5	2.5	486

Table I shows the variation of the breakdown voltage of the VDMOS 2 as a function of the depth of the P+ layer "D_{p+}" and the depth of the dielectric trench "D_{die}" in the N- layer (D_{Die} = N-layer - D_{p+}). Considering the technological realization of the P+ implantation zone, the minimum depth of this zone is 2.5 μm. According to table I and for D_{p+} equal to 2.5 μm the VDMOS 2 withstands a voltage of 721 V. Beyond this depth, the breakdown voltage decreases drastically thanks to a significant increase of the leakage current which provokes the premature breakdown.

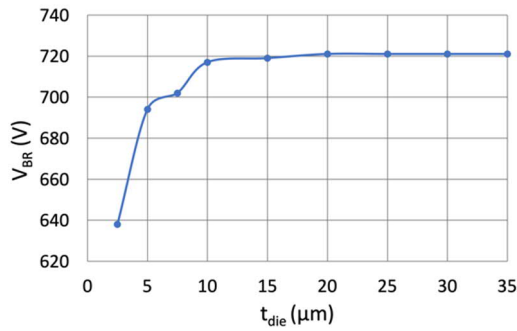


Fig. 9: Variation of the breakdown voltage "V_{BR}" of the VDMOS 2 as a function of the dielectric thickness "t_{die}". (D_{p+} = 2.5 μm) (Leakage current = 6 μA)

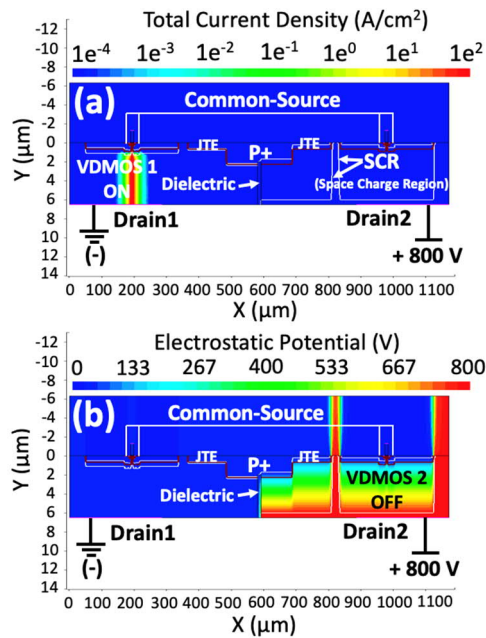


Fig. 10: Equipotential lines and current density distribution in the common-source type three-terminal power chip (X to Y ratio: 30): (a) VDMOS 1 is in the ON-state, (b) VDMOS 2 in the OFF-state. (D_{p+} = 2.5 μm and t_{die} = 20 μm) (Leakage current = 6 μA) (E_{max SiC} = 2.1 MV/cm)

Fig. 9 shows the variation of the breakdown voltage of the VDMOS 2 as a function of the thickness of the dielectric "t_{die}" and for D_{p+} = 2.5 μm. We can see that for a thickness greater than or equal to 20 μm the VDMOS 2 can withstand the optimal voltage of 721 V. Also, this thickness seems sufficient to prevent any lateral current flow between the two VDMOS sections.

Fig. 10 gives the corresponding distribution of equipotential lines and current density within the elementary common-source type chip. In case a) we can notice that the VDMOS 1 is in ON-state and carries a current density of 100 A/cm². In case b) the VDMOS 2 is in OFF-state and withstands 800 V.

Technological realization of the deep vertical insulating SiC etched-trench region

In our experimental work, we are reporting the SiC etching using two techniques: fluorinated plasma etching and electrochemical etching to perform the trenches needed in our devices.

Compared to our previous studies reported [15-17], in our Plassys MU400 fluorinated plasma ICP/RIE equipment we could reach a maximum etching rate for SiC up to 0.6 μm/min. We tried to increase the time of etching in order to increase the obtained etching thickness but the Ni mask could completely be consumed as shown in Fig. 11 (b) if the thickness of the Ni layer is not increased.

The ability to increase the Ni-deposited metal layer is limited in our cleanroom facilities, since our e-beam evaporators allow to deposit of a maximum thickness of metal layer about 250 nm.

We performed electrolysis as reported in our previous study to have a thicker metal layer [18]. We could have a metal layer equal to around 4 μm that allows us to perform deeper SiC plasma etching. The parameters we used in our performed plasma etching are based on studies done before where the optimum parameters to obtain deep etching and smooth etched surface have been investigated [15-17].

Firstly, we performed plasma etching for 30 min and we got 15 μm etching thickness then we could have performed twice the plasma etching with a 30 min duration for the etching time and the etching thickness doubled up to around 30 μm.

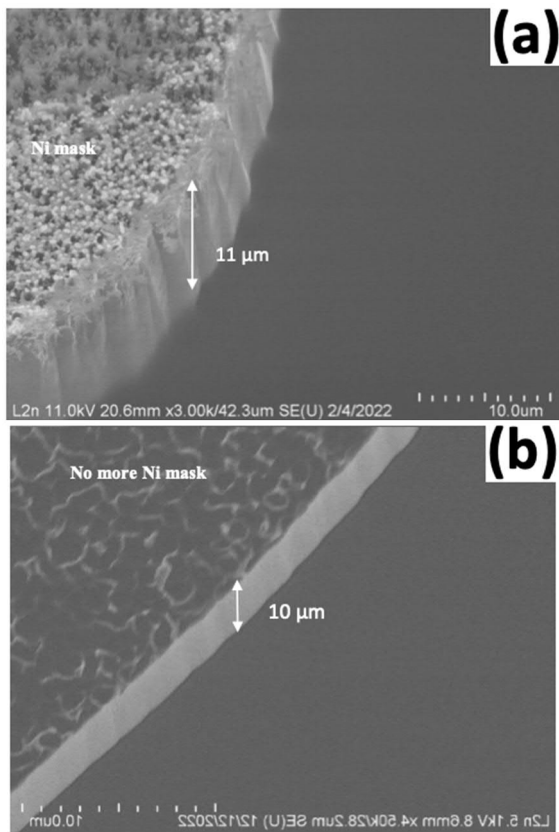


Fig. 11: (a) SEM images of etched SiC masked with Ni Mask, (b) SEM image of etched SiC and the Ni mask consumed totally.

This is today the limit of our plasma etching system, with a reasonable etching time and preserving the initial SiC state obtaining vertical and smooth trenches.

To perform the vertical insulation through the entire SiC N^+ -substrate, we need an etching thickness corresponding to the thickness of the entire N^+ substrate (100 to 350 μm) which is above the maximum etching thickness that we could obtain by plasma etching. Therefore, we go to electrochemical etching using KOH (potassium hydroxide) wet solution. In our studies, we tried different metal layers such as nickel, chrome, copper, gold, titania, silver, and silicon to pattern SiC but these metals started to release before the release of SiC. Due to the high strength of SiC, which supports and necessities high applied voltage, it is not possible to pattern it by electrochemical etching with a common metal and dielectric hard mask layers.

P-type SiC needs higher voltage than n-type SiC to release. Therefore, in our work, we used p-type SiC to pattern n-type SiC by KOH

electrochemical etching. To perform this patterning, first, we deposited Ni mask on p-type SiC and pattern it using photoresist and lithography then we perform plasma etching on the SiC p-type layer up to the N^+ substrate. Then electrochemical etching as shown in Fig. 12 was performed. Using electrochemical etching we could obtain at least 80 μm etching thickness.

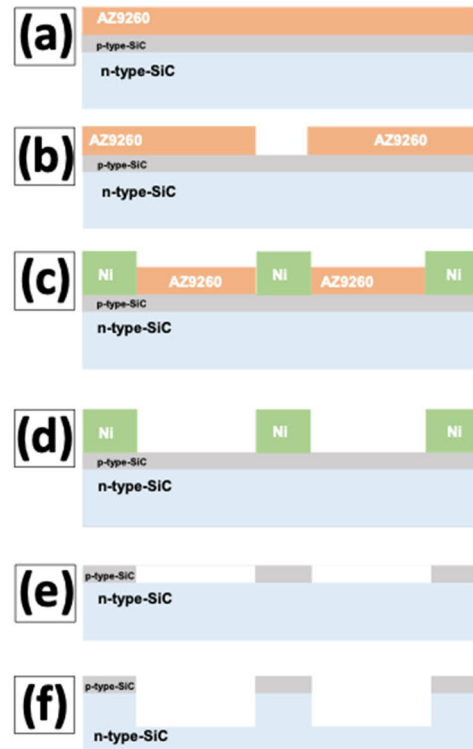


Fig. 12: Schematized image showing: (a) n-type SiC covered by p-type SiC and AZ9260 photoresist, (b) after patterning the photoresist using lithography UV irradiation, (c) after deposition of 200 nm Ni metal layer, (d) after performing lift-off using acetone and alcohol, (e) after performing plasma etching, (f) after performing electrochemical etching and the p-type SiC act as a stoping layer

Despite the deep etching thickness that we obtained using electrochemical etching, the electrochemical etched surface has more roughness compared to the plasma etched surface. This different surface-state is due to the porous surface formed on the SiC electrochemical etching process as shown in Fig. 13.

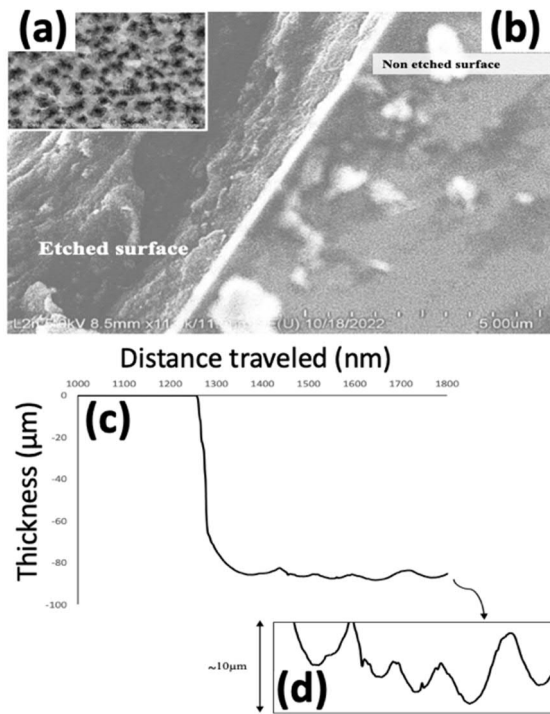


Fig. 13: (a) SEM image of SiC electrochemical etched surface: to the right we have the non-etched surface and to the left we have the etched surface. (b) Inset showed the porous surface of the electrochemical etched part of SiC. (c) Dektak stylus profilometer measurements showing the thickness of the SiC electrochemical etched surface. (d) Inset with the roughness of the electrochemical etched surface.

Conclusion

In this paper, a design perimeter for a full-SiC single-chip high-side and low-side dual-MOSFET for ultimate power vertical integration is proposed. The operating modes of the common-drain and common-source three-terminal power chip were validated using 2D Sentaurus™ mixed-mode simulations. A minimum distance of 12 μm is required to minimize the electrical interaction between the two VDMOS sections of the common-drain three-terminal power chip. A 2.5 μm depth for the P⁺ layer and a 20 μm dielectric thickness is required to prevent any lateral current flow between the two VDMOS sections of the common-source three-terminal power chip. Electrical insulation using a deep trench in the back side and a deep P⁺ implementation above this trench is introduced. This technological step requires deep etching through the N⁺ substrate up to the P⁺ layer created in surface. We propose to combine fluorinated ICP/RIE dry plasma and wet KOH

electrochemical etching to obtain the deep trenches. Higher etching thicknesses can be obtained by electrochemical process but in this case rough etched surfaces are obtained and compatible masks are difficult to find to pattern, excepting using SiC sacrificial p-type layers. The impact of the rough surface should be considered on the electrical insulating and electric field crowding in the MOSFET active area. For this, plasma etching should be also utilized at the process end in order to smooth the rough trenches and the bottom surface.

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