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ABSTRACT

In this work, Al_2O_3-passivated, monolithic, and crystalline Al–Ge–Al heterostructure nanowire field effect transistors (FETs) with Ge channel lengths ranging from 18 to 826 nm are analyzed from a low-frequency noise perspective. 1/f and random telegraph noise (RTN) are analyzed in an accumulation mode, where the hole channel is formed by applying a back-gate potential V_G. The normalized power spectral density of drain current fluctuations of 1/f noise (S_{ID}/I_D^2) at medium currents follows nearly an $1/I_D$ trend. 1/f noise is analyzed within both the mobility and carrier number fluctuation models (MFM and CNFM), respectively. Taking the MFM into account, the Hooge noise parameter α spreads in the interval of 1.5×10^{-4} to 4×10^{-2}, with lower values for shorter devices. Using the same data and the CNFM, the density of interface states D_{it} in the $Al_2O_3/Ge_xO_y/Ge$ system was estimated using the transconductance extracted from the quasi-static transfer I/V characteristics. The extracted D_{it} values range from 5×10^9 to $3 \times 10^{12}\,cm^{-2}\,eV^{-1}$. Contact noise has also been observed in some devices at high currents. RTN analyzed in time domain exhibits a relative RTN amplitude in the 0.3%–20% range. Capture and emission time constants as a function of V_G exhibit a typical behavior for metal oxide semiconductor FETs. The extracted noise parameters are comparable with Ge and III–V nanodevices of top-down and bottom-up technologies.

Nanoscale Ge devices are attractive for both fundamental studies of low-dimensional nanostructures as well as for future high-performance nanoelectronic and quantum devices.[1–3] In this context, single-crystalline vapor–liquid–solid (VLS) grown Ge nanowires (NWs) have drawn significant attention as they enable a suitable platform to perform investigations on confinement effects, quasi-ballistic transport,[4] surface treatments, and high quality metal–semiconductor junctions.[5–7] Low frequency noise (LFN) analysis on NW devices has been proven to give useful information of surface trapping and scattering mechanisms in NW devices.[8,9] Carrier number[10] and mobility fluctuation models[11] (CNFM and MFM) are used to interpret noise in NWs.[12,13] 1/f has been studied in unpassivated NW field effect transistors (FETs) based on the NiGe–Ge system[14] and Ge FinFETs.[15–18] In particular, Wu *et al.* have shown a large variation in Hooge noise parameter α in Ge FinFET devices of the same dimension, which has been attributed to device-to-device variability.[19–21] Random telegraph noise (RTN) in Ge nanodevices is rarely reported.[14,18,22] In this paper, we analyze LFN in Al_2O_3-passivated FETs based on monolithic Al-Ge-Al NWs with different channel lengths L. 1/f noise analyzed in the frequency domain is interpreted in terms of both the CNFM and MFM. The noise parameter α and equivalent density of interface trap states D_{it} are determined. Contact noise is also investigated and modeled. RTN is analyzed in the time domain and interpreted in terms of the CNFM. Our main finding is a large spreading of the noise parameter α (and D_{it}) and of the relative RTN amplitude dI_D/I_D (dI_D being the RTN amplitude), over two to three orders of magnitude, which is attributed to device-to-device variability typical for downscaled devices, in general.[19–21] Interface and border traps[23] in the $Al_2O_3/Ge_xO_y/Ge$ system are considered to be mainly responsible for the observed noise fluctuations.

The Al–Ge–Al heterostructure devices are integrated into a back-gated FET architecture[13] [see Fig. 1(a)]. The starting materials are intrinsic VLS grown Ge NWs with diameters of approximately 35 nm and atomically flat facets [see Fig. 1(b)]. The NWs are enwrapped in a

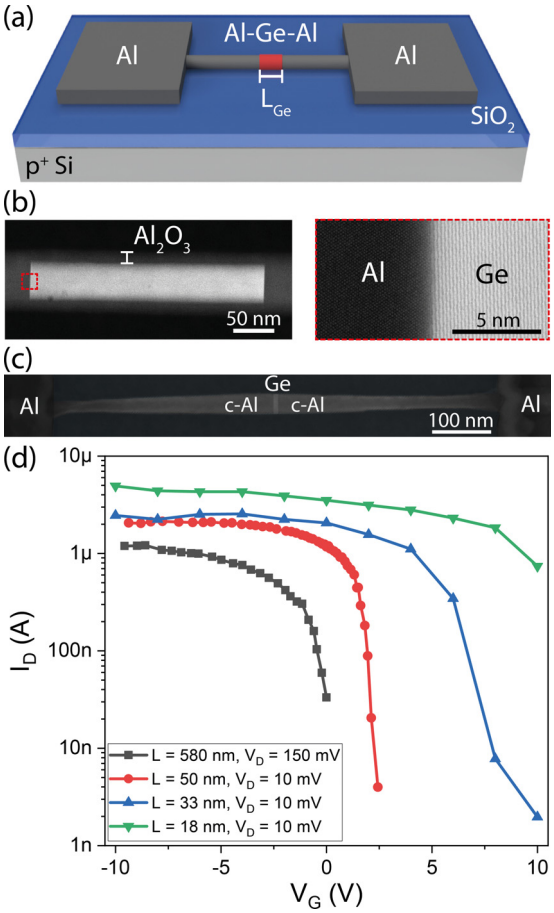

FIG. 1. (a) Schematic of the Al–Ge–Al heterostructure integrated in a NW FET device. (b) Left: high angle annular dark field scanning transmission electron microscopy (HAADF STEM) images of an entire Al–Ge–Al NW heterostructure enwrapped in a 22 nm Al_2O_3 shell. Right: a zoomed-in view on the Al–Ge interface using TEM. (c) SEM image of a device with L = 18 nm. (d) The quasi-static transfer IV characteristic measurements of selected devices with an indicated channel length L.

22 nm thick atomic layer deposited Al_2O_3 shell to passivate the NW surface,[24] thus ensuring reproducible and more stable transistor characteristics and preventing oxidation of the NWs.[25] As the NWs are conformally coated with Al_2O_3 ($\varepsilon_r = 8$), the equivalent oxide thickness (EOT) increases from 100 nm (SiO_2 back-gate oxide) to $d_{ox} = 111$ nm. Within the process, a native Ge_xO_y of about 2 nm is formed, causing charge carrier trapping induced shift of the threshold voltage.[26] Due to uncertainties, i.e. exact composition and thickness of the Ge oxide, this layer is neglected within the EOT. For NW device integration, Al leads are fabricated by e-beam lithography, sputter deposition, and lift-off techniques. Monolithic single-elementary Al contacts are formed by employing a thermally induced Al–Ge exchange initiated by rapid thermal annealing at 350 °C, resulting in an atomically sharp Al–Ge interface.[4] A scanning electron microscopy (SEM) image of a device with L = 18 nm is shown in Fig. 1(c). The devices exhibit a drift of the drain current I_D, due to the presence of a Ge_xO_y layer.[25,27]

Therefore, when changing the V_G, after setting a new V_G value, we waited until no visible drift is observed in time domain waveform. Spectral measurements are performed with a simultaneous monitoring of the time domain signal, which allows us to unambiguously distinguish and decompose 1/f spectrum from the RTN-related Lorentzian.

Figure 1(d) shows typical quasi-static transfer I_D–V_G characteristics in accumulation of devices with selected L values, V_G being the back-gate voltage, which is negative in accumulation. The voltage ramping speed was approximately 500 mV/min, so in comparison with I_D–V_G measurements in Ref. 14, where a faster sweeping rate was used, negligible hysteresis was observed. Due to strong Fermi-level pinning close to the valence band of the Al-Ge material system, a dominant p-type behavior is observed.[28] Moreover, a large spread of the subthreshold slope S is evident, originating from the back-gate architecture.

Figure 2(a) shows the power spectral density (PSD) of drain current fluctuations S_{ID} as a function of frequency of a device with L = 170 nm exhibiting a $1/f^{\gamma}$ spectrum (here, shortly 1/f) with γ

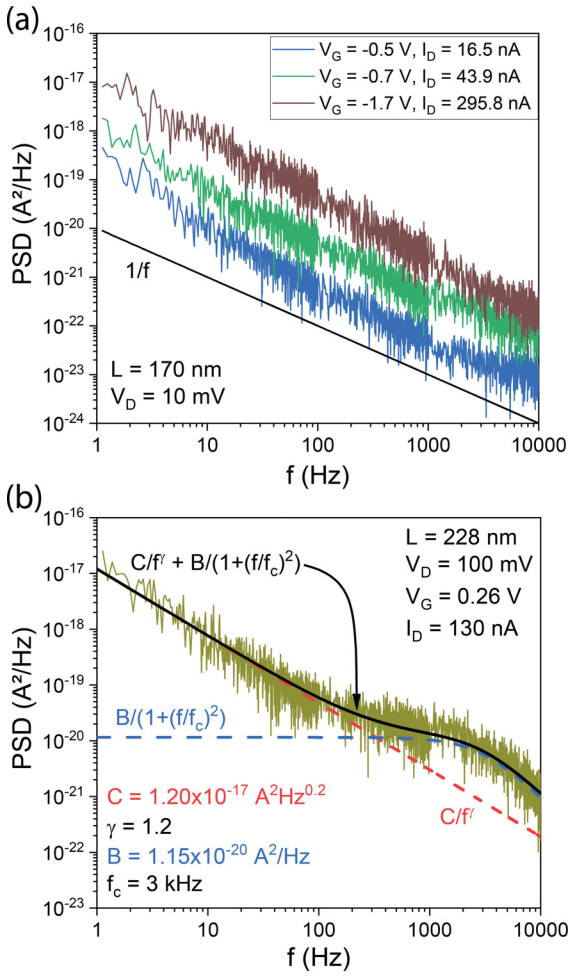

FIG. 2. (a) Typical PSD of a device with L = 170 nm for different gate voltages V_G with indicated mean drain currents I_D with $\gamma \approx 1.15$. (b) Measured PSD spectra (noisy data) exhibiting superposition of $1/f^{\gamma}$ component with a Lorentzian in a device with L = 228 nm. Simulated spectra (black solid line) with decomposed $1/f^{\gamma}$ (red dashed line) and Lorentzian (blue dashed line) components are given.

exponent near 1.15, which is constant over at least three frequency decades. I_D is the curve parameter. If RTN is superimposed to the 1/f component, the spectrum is decomposed to a 1/f and a Lorentzian component. An example of such an experimental spectrum fitted to a simulated spectrum (black solid line) with decomposed 1/f (red dashed line) and Lorentzian (blue dashed line) components is given in Fig. 2(b).

Only the decomposed 1/f component is considered in the S_{ID} evaluation in the following. The exponent γ ranges mostly between 0.9 and 1.2 with some exceptions of $\gamma = 1.25$. The averaged value of γ as a function of L is given in the inset of Fig. 3(d). Note that 1/f data with $\gamma > 1.25$ are not taken into account in the 1/f noise analysis. The normalized spectral density S_{ID}/I_D^2 extracted at 1 Hz as a function of I_D for devices with various L values in three different L intervals are plotted in Figs. 3(a)–3(c) for better distinction. A typical $S_{ID}(I_D)$ curve exhibits a plateau at low currents [see e.g. curves for L = 826 nm in Fig. 3(a) or L = 144 nm in Fig. 3(b)], followed by a nearly $1/I_D$ roll-off at medium currents. More complex S_{ID}/I_D^2 vs I_D dependencies, e.g. with a concave shape [see e.g. curve for L = 50 nm in Fig. 3(c)], are also observed. For devices with L = 170 and 228 nm [see Fig. 3(b)], a rise or at least a saturation of S_{ID}/I_D^2 at high currents is observed, which is attributed to contact noise (see below).

Within the MFM, noise occurs due to uncorrelated mobility fluctuations caused by scatterers like defects, and the normalized PSD is inversely proportional to the total number of carriers N within the active device volume,

$$S_{ID}/I_D^2 = \alpha/(fN), \tag{1}$$

where α is the already mentioned Hooge noise parameter. N can be expressed in terms of the channel resistance $R_{ch} = L^2/q\mu N$, where μ is the hole mobility, and q is the elementary charge. In the regime where the channel resistance R_{ch} dominates the contact resistance R_{cont}, i.e. $R_{ch} \gg R_{cont}$, we have $R_{ch} \approx V_D/I_D$, and the α parameter can be extracted in the region where $S_{ID}/I_D^2 \approx 1/I_D$,

$$\alpha = S_{ID}/I_D^2 \times fL^2/(q\mu R_{ch}) = S_{ID}fL^2/(q\mu I_D V_D), \tag{2}$$

where α values as a function of L extracted from Figs. 3(a)–3(c) are plotted in Fig. 4(a) (black bars and left axis). In the evaluations, a hole mobility of 300 $cm^2/V\,s$[27] has been used, whereas also other works reported mobility values around 300 $cm^2/V\,s$.[9,25] It should be remarked that there might be mobility fluctuations from device to device. So, in fact, the product $\alpha\mu$ would be fitting parameters in Eq. (2). However, for better comparison to already published works, α is extracted using the above-mentioned mobility value. One can remark that α values tend to be smaller for lower L. The α values in the 1.5×10^{-4}–4×10^{-2} range in Fig. 4(a) overlap with values in the 2×10^{-3}–1.2×10^{-2} range for Ge FinFETs.[16]

Within the CNFM, noise is due to flatband voltage fluctuations in a FET caused by carrier capture/emission with broad distribution of time constants[29] and S_{ID}/I_D^2 can be expressed in terms of the device transconductance g_m,[10,20,30,31]

$$S_{ID}/I_D^2 = (g_m/I_D)^2 \times q^2 D_{it} kT/(fWLC^2_{ox}), \tag{3}$$

where D_{it} is the density of interface traps in $cm^{-2}\,eV^{-1}$, kT is the thermal energy, and $W = 2\pi r$ is the NW width with r being the radius. Importantly, here the perimeter is considered since the Fermi level is assumed to be pinned at the same position along the NW cross section. C_{ox} is the capacitance per unit of area, expressed here for simplicity as $C_{ox} = \varepsilon_r\varepsilon_0/d_{ox}$ with ε_r being the relative permittivity of SiO_2 ($\varepsilon_r = 3.9$), ε_0 being the vacuum permittivity, and $d_{ox} = 111$ nm is the above-mentioned EOT. The measured S_{ID}/I_D^2 dependence is fitted by the right side of Eq. (3), where D_{it} is taken as the fitting parameter. Figure 3(d) shows the result of such a procedure where the S_{ID}/I_D^2 vs I_D data of a device with L = 50 nm are plotted together with $(g_m/I_D)^2$. The concave shape of S_{ID}/I_D^2 is qualitatively reproduced. The extracted values of D_{it} are plotted on the right axis of Fig. 4(a). Again, a large

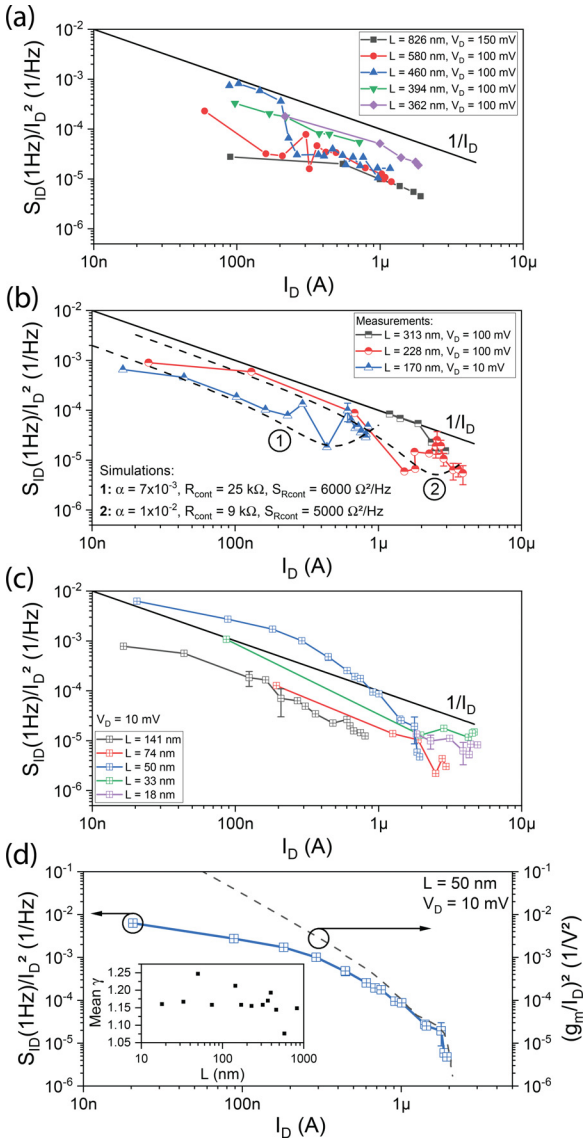

FIG. 3. (a)–(c) Symbols are measured normalized PSD (S_{ID}/I_D^2) vs I_D data for devices with different L. The data in (a)–(c) are arranged with decreasing L values. The $1/I_D$ slope is indicated in (a)–(c). Dashed lines 1 and 2 in (b) are simulations. (d) Replotted experimental S_{ID}/I_D^2 vs I_D data from (c) in correlation with $(g_m/I_D)^2$ extracted from the quasi-static transfer characteristic for a device with L = 50 nm. The inset in (d) shows the mean γ values for devices with different L.

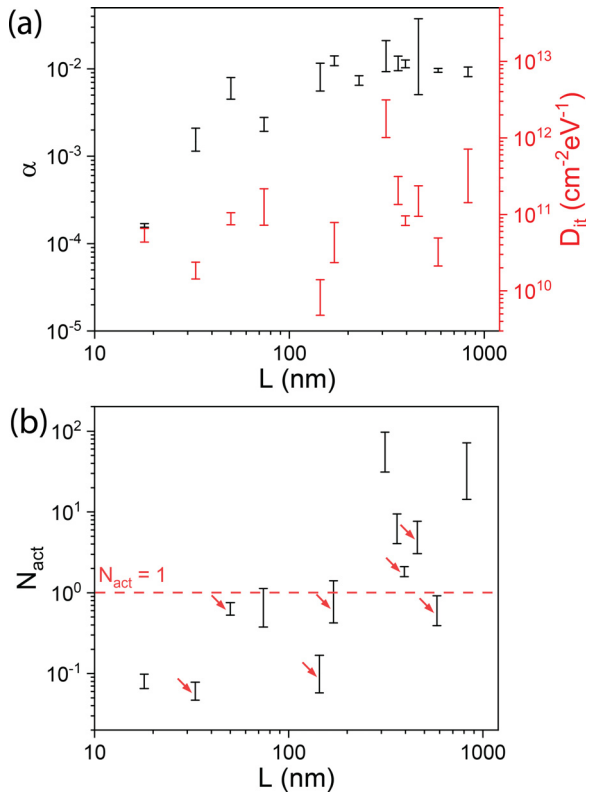

FIG. 4. (a) Extracted Hooge parameter α (black bars) and D_{it} (red bars) as a function of L. The bars indicate a data range, originating from uncertainties in the fitting procedure. (b) N_{act} derived from D_{it} for devices with different L, where the red arrows indicate devices, which also showed a Lorentzian component.

spreading in D_{it} is observed. The found D_{it} values in the 5×10^9–3×10^{12} cm^{-2} eV^{-1} range are comparable or higher than equivalent D_{it} values in the 6×10^9–6×10^{10} cm^{-2} eV^{-1} interval found from 1/f noise evaluation of n-channel Ge FinFETs.[15] The D_{it} values obtained from our 1/f noise analysis are also compared with D_{it} values from the evaluation of I_D/V_G hysteresis measurements using fast V_G sweeps (≈0.2 V/s). A threshold voltage shift dV_{th} in the range of 1–10 V has been measured (see also Ref. 25). Using sheet charge density approximation, D_{it} can be estimated as $D_{it} = C_{ox} \times dV_{th}/(qE_g)$, where we considered a constant D_{it} distribution over the Ge bandgap E_g (0.67 eV) for simplicity. The extracted values of $D_{it} = 3 \times 10^{11}$ to 3×10^{12} cm^2 eV^{-1} are consistent with D_{it} extracted in Fig. 4(a). We notice that due to complex electrostatics and not reliable model for relation between subthreshold slope S and D_{it} in NWs, we did not use S for the D_{it} evaluation, as was done earlier, e.g. in Si MOSFETs.[32] Finally, Fig. 4b shows the number of active surface traps $N_{act} = D_{it} \times WL \times 4kT$ within the CNFM as a function of L using the integration of D_{it} over the active surface area WL and 4kT (102 meV at 295 K). N_{act} varies between ≈0.1 and ≈100 for devices with L from 18 to 826 nm. A positive correlation between N_{act} and L is found.

Contact noise is modeled considering as a series combination of uncorrelated resistance noise sources due to channel resistance S_{Rch} and contact resistance S_{Rcont}. For simplicity, S_{Rch} will be expressed in terms of the MFM, but qualitatively the same behavior could be obtained using the CNFM for S_{Rch}.[11] The relative current noise PSD can be expressed as

$$S_{ID}/I_D^2 = (S_{Rch} + S_{Rcont})/(R_{ch} + R_{cont})^2, \quad (4)$$

where $R_{tot} = R_{ch} + R_{cont}\, V_D/I_D$. Expressing S_{Rch} in terms of R_{ch},

$$S_{Rch}/R_{ch}^2 = \alpha/(Nf) = R_{ch}q \times \mu/L^2 \times \alpha/f, \quad (5)$$

we get a final expression for the normalized S_{ID}, evaluated at f = 1 Hz,

$$S_{ID}/I_D^2 = \left[q\mu/L^2 \times \alpha(V_D - I_D R_{cont})^3/I_D + S_{Rcont} I^2\right]/V^2. \quad (6)$$

Curves 1 and 2 in Fig. 3(b) show the simulated S_{ID}/I_D^2 vs I_D dependencies for devices with L = 228 and 170 nm, using Eq. (6), with the parameters α, R_{cont}, and S_{Rcont} given in the legend of Fig. 3(b). R_{cont} is consistent with the resistance evaluated in the saturation part of the I_D–V_G dependence, i.e. in strong accumulation where R_{cont} dominates [see Fig. 1(d)]. The ≈$1/I_D$ part or downward concave bending of the S_{ID}/I_D^2 vs I_D dependence, where the channel noise dominates at low currents and is proportional to α, is fitted by the cubic term in Eq. (6). In this current range, $V_D \gg I_D R_{cont}$ holds. The S_{ID}/I_D^2 rise at high currents in curves 1 and 2 is due to the dominance of the term with S_{Rcont} in Eq. (6). The general trend of the experimental data is reproduced by simulations. The calculated normalized contact resistance noise values of S_{Rcont}/R_{cont}^2 in the range of 1–6 × 10^{-5} 1/Hz are consistent with that in InAs NWs with a value of 1 × 10^{-5} 1/Hz.[33]

We have found stationary and intermittent RTN in both short and long channel devices. Figure 5(a) shows a typical example of stationary current fluctuations as a function of V_G. At more negative V_G, so in accumulation, the RTN mean pulse width in the upper RTN state ⟨t+⟩ decreases, while RTN in lower RTN state ⟨t−⟩ rises. Figure 6 shows the V_G dependence of ⟨t+⟩ and ⟨t−⟩in two devices. The decrease in ⟨t+⟩ with increasing hole concentration in the channel is due to an increased hole capture probability of interface or border states.[14,29] The rising of the hole emission time constants with negative V_G can be due to localized traps further in the oxide away from the $Ge/Ge_xO_y/Al_2O_3$ interface, i.e., on border traps.[23] Given the low number of data points, we were, not able to reliably identify the trap depth position.[34] Figure 5(b) summarizes the normalized RTN amplitude, dI_D/I_D as a function of I_D. dI_D/I_D varies in the 0.3%–20% range. One may see a plateau at depletion and an overall decrease in dI_D/I_D at high currents. Considering that the change of the charge state of an interface defect causes the RTN fluctuations, we have tried to fit each dI_D/I_D vs I_D dependence to the following expression,[20,21,35] which is a time domain equivalent of Eq. (3),

$$dI_D/I_D = \beta q/(WLC_{ox}) \times (g_m/I_D). \quad (7)$$

Here, the coefficient β is a fitting coefficient, where β = 1 represents an ideal case for the equivalent sheet charge density q/WL homogeneously distributed over the active area. An example of such a fitting is given in Fig. 7(a), where dI_D/I_D–I_D data are matched to g_m/I_D vs I_D data with β ≈ 9.3 (for L = 460 nm). The extracted β values as a function of L for all measured devices with RTN are given in Fig. 7(b). These values group in the ≈1–3.3 range for L < 200 nm but reach the value of ≈9.3 for the device with L = 460 nm. Similar range of β values have been observed in top-down downscaled MOSFETs.[35] The β value can depend on the size of the effective current modulation area of

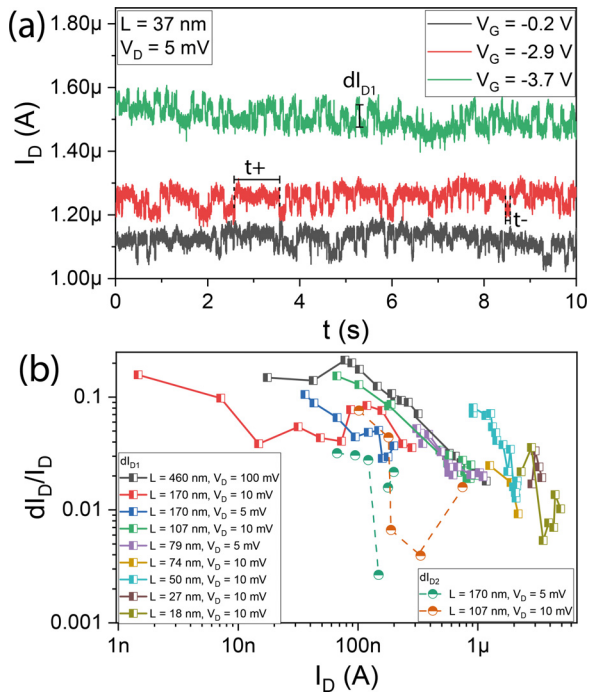

FIG. 5. (a) RTN waveform of a device with L = 37 nm for different gate voltages V_G in accumulation. (b) The relative amplitude of RTN as a function of I_D for devices with different L. dI_{D1} indicates the amplitude of a dominant RTN, while dI_{D2} is the amplitude of an additional RTN appearing at higher currents.

traps,[35] exact position of traps along the NW[36] but also on the surface potential variations along the channel.

We think that the surface properties, in our case, the $Ge/Ge_xO_y/Al_2O_3$ interface, play an important role in the noise behavior, using both the MFM and CNFM for interpretations. The carrier trapping/de-trapping at interface and border trap states and the scattering on

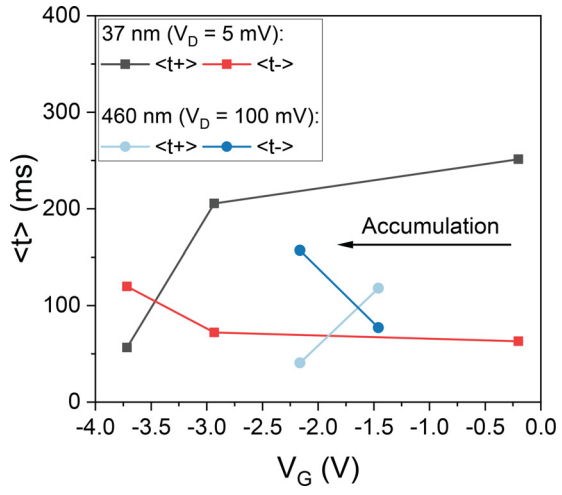

FIG. 6. RTN mean pulse width as a function of back-gate voltage V_G for devices with L = 37 and 460 nm.

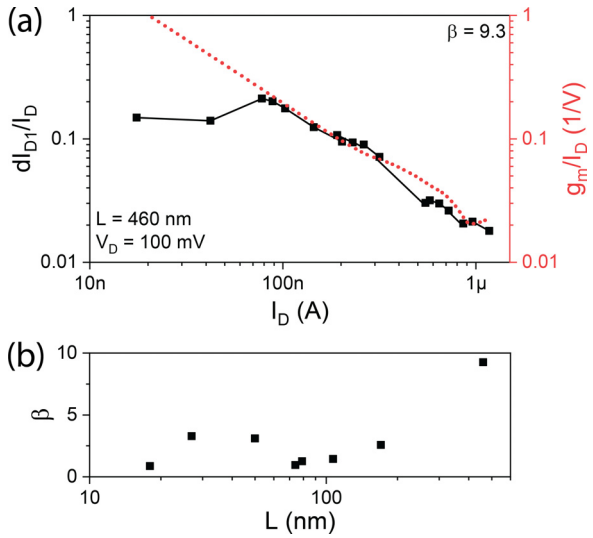

FIG. 7. (a) Result of fitting for the extraction of β with the measured relative RTN amplitude indicated by symbols and g_m/I_D is the red curve (right y-axis). (b) Extracted β values for devices ranging from L = 18 to 460 nm.

defects or surface potential landscape along the NW can control the fluctuations. Carrier number fluctuations or even correlated carrier number fluctuations are considered as origin of 1/f and RTN within the CNFM.[31,36,37] On the other hand, both surface and bulk origin of mobility fluctuations in the MFM have been considered as noise sources in NWs.[12,14] We are not in favor of any model, both mechanisms (i.e. MFM and CNFM) can be treated as occurring in parallel. To support this statement, we discuss data in Fig. 4(b) at lower L where the number of active traps N_{act} is of the order of 0.1. Using the CNFM, $N_{act} = 1$ means implicitly an existence of a two-level RTN giving rise to a single Lorentzian. However, N_{act} was extracted from the magnitude of the pure 1/f noise spectrum or from the 1/f component of a spectrum with a superimposed Lorentzian. Thus, having $N_{act} < 1$ contradicts that the CNFM is the origin of 1/f noise. So it is likely that both MFM and CNFM mechanisms can occur simultaneously, not excluding each other. Within the framework of the used models, it therefore seems that for low L the 1/f noise is related to the MFM. Exact distinction between the CNFM and MFM is still a matter of discussion[11] and is beyond the scope of this paper. The large spread in α and D_{it} values [cf. Fig. 4(a)] can be related to device-to-device variability[19,38] of these downscaled devices. Indeed a large spread, over two orders of magnitude has been found in D_{it} in Si MOSFET devices[20] and in Ge FinFETs.[15] Wu *et al.* also found a large spread in α values of Ge FinFETs.[16] Exact position of traps along the channel,[36] in particular in the subthreshold region,[39] and the spread in the defect parameters[29] can play a role in this variability. The observed spread in β values of RTN [Fig. 7(b)], found also in Ref. 35, supports this view. Wu *et al.* also pointed out that the observed lower α values for shorter channel devices can be a sign of reducing mobility fluctuations due to less scattering mechanisms in ballistic devices.[16] We have seen the similar effect in our bottom-up devices, but our statistical set is smaller than that of the top-down devices of Wu *et al.* So, the strength of our interpretation is weaker than that of Wu *et al.*

1/f and RTN has been analyzed in Ge NW FETs with different channel length L. Our results show a large spread in the magnitude of 1/f noise, represented in terms of Hooge coefficient α or interface state density D_{it}, and of RTN relative amplitude, represented via parameter β. The spread is attributed to device-to-device variability commonly found in downscaled devices. The obtained α, D_{it}, and β are consistent with previously literature data found in Si and Ge devices. Despite atomic flat facets of Ge NWs, these are the omnipresent interface and border states at the $Ge/Ge_xO_y/Al_2O_3$ interface, which controls the noise considering both carrier number and mobility fluctuation models. So optimization of semiconductor/dielectric interface is needed. Furthermore, we have found a pronounced contact noise in at least two devices at high current levels. However, based on these results, it is difficult to state where the contact noise values represent some typical value for the atomically flat Al-Ge junction or whether other effects, like, e.g. charges at the $Ge/Ge_xO_y/Al_2O_3$ interface at the NW perimeter around the junction, play a role in the contact fluctuation mechanism. Larger statistical set of samples is needed in the future studies of contact noise.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Raphael Behrle: Formal analysis (equal); Investigation (equal); Writing – original draft (equal). **Masiar Sistani:** Funding acquisition (equal); Project administration (equal); Supervision (equal); Writing – review & editing (equal). **Alois Lugstein:** Resources (equal). **Zahra Sadre Momtaz:** Investigation (supporting). **Martien I. den Hertog:** Investigation (supporting). **Dionyz Pogany:** Conceptualization (equal); Investigation (equal); Methodology (equal); Project administration (equal); Supervision (equal); Writing – original draft (equal); Writing – review & editing (equal). **Walter M. Weber:** Project administration (equal); Supervision (equal).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding authors upon reasonable request.

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