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Electrically Active Traps in 4H-Silicon Carbide (4H-SiC) PiN Power Diodes

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Abstract:

The electrically active traps in 4H-silicon carbide (4H-SiC) PiN power diodes are identified by deep-level transient Fourier spectroscopy (DLTFS). The junction termination extension (JTE) and floating JTE rings (periphery protections) are realized using the Al^+ ion-implantation process in the PiN diode structure, to mitigate the electric field crowding at the junction edges and obtain the theoretically projected off-state performance. The 4H-SiC PiN diode exhibits forward voltage drop of ~2.6 V at 1 mA, ideality factor of ~1.6, series resistance of ~1.2 Ω, low reverse leakage current < 0.5 nA at 200 V, blocking voltage > 200 V, built-in barrier potential of ~2.1V, and effective doping concentration for the drift layer of $\sim 7.9\times10^{14}$ cm^{-3}. The temperature-induced changes in the forward I-V characteristics are investigated from 25 °C to 150 °C. From the DLTFS results, three hole traps H1 at $E_V + 0.16$eV, H2 at $E_V + 0.3$ eV, and H3 at $E_V + 0.63$ eV, and two electron traps E1 at $E_C – 0.19$ eV and E2 at $E_C – 0.67$ eV are identified in the 4H-SiC PiN diodes. The current-mode DLTFS (I-DLTFS) and thermally stimulated capacitance (TSCAP) spectroscopy measurements are also carried out to acquire further information about the traps in the 4H-SiC PiN diodes.

Keywords: Silicon carbide, PiN diode, I-V characteristics, defects, DLTFS, TSCAP.

1 Introduction

4H-silicon carbide (4H-SiC) is an attractive compound semiconductor for power applications due to its superior physical properties such as wide band gap of 3.26 eV (enables high-temperature operation), high critical breakdown electric field (E_{CR} 10 times of silicon), high saturation velocity (fast switching speed), and high thermal conductivity (3 times of silicon) [1-3]. High breakdown voltages (V_{BR} > 1 kV) can be easily achieved with a simple Schottky barrier diode (SBD) structure fabricated on 4H-SiC epitaxial layers (even without field plate and surface passivation); in contrast the silicon-based technology requires complicated device structures (increases the fabrication cost) to attain similar V_{BR}. Since E_{CR} of 4H-SiC is much higher than Si, one can reduce the drift layer thickness (yielding a small die size) and increase the doping density to achieve the same V_{BR}, alongside lower on-state series resistance [3]. Currently, the 4H-SiC device technology has matured to the industrial-grade standard, such that 4H-SiC power diodes (Schottky barrier diode (SBD), Junction barrier Schottky (JBS) diode, and Merged PiN Schottky (MPS) diode) and power MOSFETs are commercially available at reasonable prices. The 4H-SiC SBDs demonstrated high breakdown voltage > 3.3 kV, fast reverse and forward recovery (due to lack of minority carrier injection), low switching losses, and maximum junction operating temperature > 175 °C, thus making them ideal for high-power applications with the least requirement of a heat sink [1, 4]. However, the 4H-

SiC SBDs exhibit relatively high leakage current while operating at larger reverse voltages (> 200 V) through the barrier lowering effect and tunnelling current generation mechanisms [1, 5]. The breakdown voltage of the commercial 4H-SiC SBDs is limited up to 3.3 kV. Due to the absence of drift conductivity modulation in the 4H-SiC SBDs, the drift layer series resistance reduces the forward current at higher voltages and induces overheating than predicted [6]. So, the 4H-SiC SBDs may not withstand inrush currents during the power switching operations.

Ultra-high breakdown voltage devices ($V_{BR} > 10$ kV) are necessary for the smart grid, medium-voltage direct current (MVDC), and high-voltage direct current (HVDC) energy transmission applications [7, 8]. The 4H-SiC PiN diodes with periphery protection have shown ultra-high breakdown voltage ($V_{BR} > 10$ kV), high current handling capability (> 50 A), low reverse leakage current, and drift conductivity modulation, as compared to the well-developed 4H-SiC SBD technology [7, 8]. Especially, the bipolar PiN rectifiers benefit from the drift conductivity modulation due to the minority carrier (hole) injection; as a result on-state series-resistance decreases [3]. The principal reason behind the reverse leakage current of the PiN diode is due to the thermal generation of carriers inside the depletion region; this conduction mechanism is expected to be small in the wide bandgap 4H-SiC material. To achieve theoretically projected breakdown voltage and reduce the reverse leakage current, the electric field crowding around the junction edges should be mitigated by the junction termination extension (JTE) and floating JTE ring techniques [7].

The n-type 4H-SiC epilayer quality has been considerably improved in recent years, such that the trap concentration (N_T) of the performance-limiting defect $Z_{1/2}$ (E_C - 0.67 eV) is lower than $N_T < 5\times10^{12}$ cm^{-3} [9]. A typical 4H-SiC PiN diode structure integrates double p-type epitaxial layers (p and p$^+$ layers) [7, 8]. The incomplete ionization of acceptor dopants occurs in the p-type 4H-SiC layers even at room temperature (reduced free hole density in the valence band), due to the deeper Al-related acceptor ionization energy at E_V + 0.22 eV. So, the p-type epilayer quality is sub-standard than the n-type in the 4H-SiC. The JTE and floating p$^+$ ring protections are realized by Al$^+$ ion-implantation [7, 8], to achieve theoretical breakdown voltage and low reverse leakage current. Although peripheral projection is beneficial in attaining high breakdown voltage, at the same time, the ion-implantation process creates crystal damage in the active volume of the diode [10, 11]. The ion-implantation-induced crystal defects introduce electrically active traps inside the energy bandgap of 4H-SiC and affect the diode characteristics via charge trapping/detrapping dynamics [10-12]. Thus, identifying electrically active traps in the PiN diodes is essential to improve the crystalline quality of 4H-SiC wafers.

Several authors employed the conventional deep-level transient spectroscopy (DLTS) to characterize the electrically active traps in the non-irradiated [13], Al$^+$-implanted [11], and proton-irradiated [14-16] 4H-SiC PiN diodes. On the other hand, the deep-level transient Fourier spectroscopy (DLTFS) yields several advantages over the conventional DLTS technique such as, direct computation of trap signatures (energy level, capture cross-section, and trap concentration) through a single thermal scan, estimation of time constant using Fourier coefficient ratio (instead of evaluating transient amplitude and offset), better signal-to-noise (SNR) ratio, rejection of non-exponential transients, and the possibility of separating overlapping transients. Hence, the DLTFS is a powerful characterization technique to detect the electronic trap levels in the semiconductor devices [17-19]. Stuchlíková *et al.* [20] applied the DLTFS method to detect the traps in SiC PiN diodes fabricated on natural and/or isotope-pure epitaxial layers; the authors determined eight deep-level traps in the energy range of 0.6-1.1 eV, but the periphery protection might not be included in the PiN diode structure. Dong *et al* [21] identified three electron traps at E_C – 0.65 eV, E_C – 0.87 eV, and E_C – 1.1 eV in the electron-irradiated 4H-SiC PiN diodes, but t the hole traps at $E_V + E_T$ were not observed. To acquire further quantitative information about the traps, this work is targeted to characterize the electrically active defects in the 4H-SiC PiN diodes by the DLTFS experiment. Moreover, current-mode DLTFS (I-DLTFS) [18, 19, 21] and thermally stimulated capacitance (TSCAP) spectroscopy [5, 18] measurements are conducted to complement the DLTFS results and to obtain additional details about the traps in the 4H-SiC PiN power diodes. This work also incorporates the electrical (I-V and C-V) characterization of the 4H-SiC PiN diodes.

2 Experiment

2.1 4H-SiC PiN Diode Structure

The PiN power diodes were fabricated on the commercially available homoepitaxial 4H-SiC wafers (4-inch diameter), procured from Wolfspeed Inc. (formerly CREE). The 4H-SiC wafers were double-side polished, and the silicon-face of the epilayer (at the diode active area) had a chemically mechanically polished (CMP) surface. The 4H-SiC epilayer structure includes 110 µm thick lightly doped (7×10^{14} cm^{-3}) n$^-$ epitaxial layer (drift layer) grown on n$^+$ 4H-SiC substrate (10^{18} cm^{-3}), 1 µm thick p-type layer with a doping density of 6×10^{17} cm^{-3}, and 0.5 µm highly-doped (6×10^{19} cm^{-3}) p$^+$ 4H-SiC layer. Thus, the homoepitaxial substrate already integrates the PiN diode structure due to the n-type, and p-type epitaxial layers grown on the 4H-SiC substrate. The detailed diode fabrication steps are given elsewhere [7] and are briefly summarized here: The Al$^+$ ion-implantation dose, junction termination extension (JTE) length, the number of floating JTE rings in the diode structure, and the distance between the JTE rings were optimized by using Sentaurus TCAD simulations, as reported in our earlier work [7]. The Al$^+$ ion-implantation dose of 8.5×10^{12} cm^{-2} (in JTE and floating ring regions) and the JTE length of 400 µm were found to be optimum for achieving high breakdown voltage and low reverse leakage current. Before the JTE and floating ring formation, mesa etching was carried out to isolate the devices and attain effective periphery protection. Seven lithography process steps were incorporated for the PiN diode fabrication with the periphery protections. Accordingly, six floating JTE rings were incorporated into the device design, and the distance between the rings increased moving outwards of the junction. The anode and cathode electrodes of a typical PiN diode require an Ohmic contact. A high work function metal was chosen to make the Ohmic contact with the highly-doped p$^+$ active layer (anode contact). Whereas, a low work function metal was selected to create the Ohmic contact with the highly-doped n$^+$ substrate. Further details of the diode fabrication steps are not provided to protect the intellectual property rights (IPR). The schematic 2D cross-section and photograph of the fabricated 4H-SiC PiN diodes are shown in Fig. 1. The 4H-SiC PiN diodes are square sized with a length of 3 mm (diode active area 9 mm^2). The diode corners have the curved edges (not having the usual sharp terminations) with a radius of 600 µm.

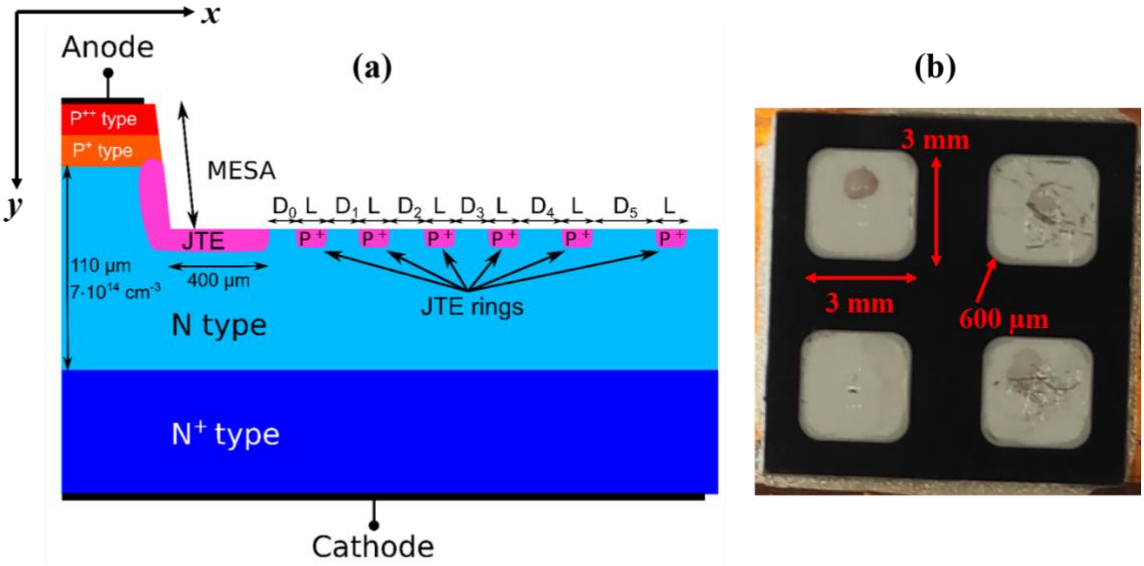

Fig. 1 (a) Schematic 2D cross-section and (b) photograph of the fabricated 4H-SiC PiN diodes.

2.2 Diode Characterization

I-V characteristics of the 4H-SiC PiN diodes were measured at different temperatures (25 °C to 150 °C) by the Keithley 2410 SMU and the DC probe station with temperature variation. The Boontoon 7200 capacitance meter was used to acquire the C-V characteristics of the diode at a high signal frequency of 1 MHz. The schematic view of the capacitance-mode and current-mode deep-level transient Fourier spectroscopy (C-DLTFS and I-DLTFS) measurement setup is depicted in Fig. 2. The diode-under-test (DUT) was placed on the sample stage of the Janis cryostat. The sample cooling was achieved using the liquid helium cryogenic system. During the thermal ramp-up scan, the DUT temperature was controlled and measured by the lakeshore 336 temperature controller. Initially, a quiescent reverse bias voltage of V_{QR} = -10 V was applied to the DUT; then the diode voltage was changed from V_{QR} = -10 V to V_P = -0.1 V for a pulse duration of 100 µs to populate the majority carrier traps in the 4H-SiC PiN diodes. Note that, electron traps in the n-type layers and hole traps in the p-type layers were populated under this reduced reverse bias pulsing condition. After the trap-filling pulse, the diode voltage was returned to the initial quiescent reverse bias of V_{QR} = -10 V. The resulting signal was recorded for two different emission transient periods of T_{E1} = 20.48 ms, and T_{E2} = 2.048 s. The capacitance transients were measured by the Boontoon 7200 capacitance meter and the signals were further processed by the amplifier, anti-aliasing filter, and transient recorder stages (denoted as digital data acquisition system). During the I-DLTFS measurements, the current transients were directly recorded by the current amplifier by internally disconnecting the capacitance bridge [18, 19]. The transients were measured in regular temperature intervals during the thermal ramp-up DLTFS scan. The DLTFS characterizations were carried out for temperatures ranging from 50 K to 380 K. The transient signal was represented in terms of discrete Fourier coefficients, accordingly the transient amplitude and the emission time constant for computed for each transient [17-19]. Even one DLTFS thermal scan was adequate to extract the trap signatures (activation energy, capture cross-section, and trap density) from the Arrhenius analysis (unlike conventional DLTS), rather than repeating the DLTFS experiments for different rate windows [17-19]. Moreover, the DLTFS evaluates the complete transient, whereas the box-car and lock-in analysis methods only investigate a portion of the transient signal [23]. Therefore, the DLTFS measurements are expected to provide fairly accurate information about the trap parameters in the diode.

As a first step in TSCAP characterization [5, 18], the DUT was cooled (under reverse bias voltage -10 V) to a low temperature of 40 K (T_0); at that temperature, the majority carrier traps in the 4H-SiC PiN diode were filled by reducing the reverse bias voltage to -0.1 V. Afterwards, the diode voltage was resumed to the initial bias condition of -10 V and the sample temperature was increased from 40 K to 380 K using the temperature controller. Steady-state capacitance variations were measured with respect to the temperature (referred to as equilibrium TSCAP spectroscopy) during the thermal ramp-up scan [5, 18].

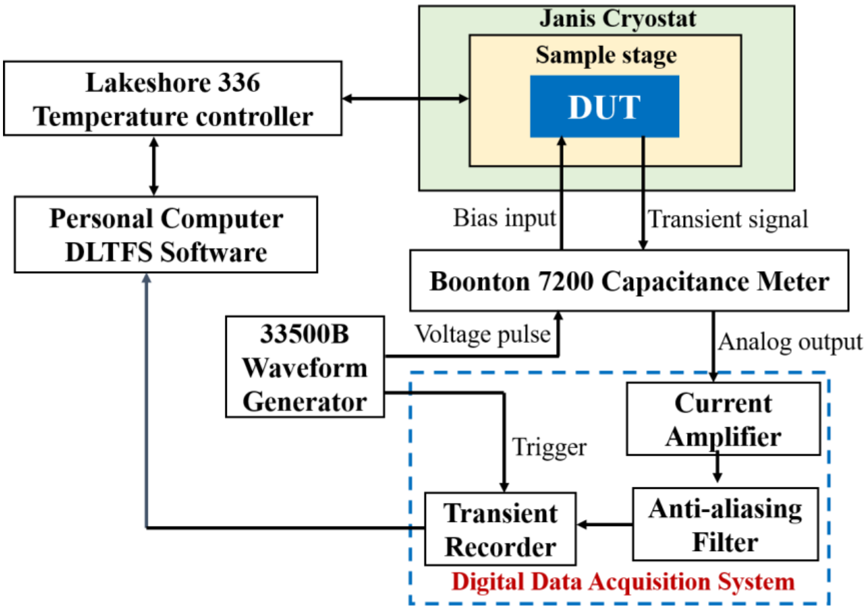

Fig. 2 Schematic view for the measurement setup of capacitance-mode and current-mode deep level transient Fourier spectroscopy (DLTFS).

3 Experiment

3.1 Electrical Characteristics

Figure 3(a) shows the forward I-V characteristics of the 4H-SiC PiN diode at 25 °C. The forward voltage drop across the diode at 1 mA is found to be 2.6 ± 0.05 V at 25 °C, which is about 2.5 times higher than that obtained with a typical 4H-SiC Schottky barrier diode (~ 1 V), due to the large built-in barrier potential of the 4H-SiC PiN diode ($V_{bi} > 2$ V). The built-in barrier potential (V_{bi}) is related to the intrinsic carrier concentration (n_i) as per the expression [3, 24]

$$V_{bi} = \frac{kT}{q} \ln\left(\frac{N_A N_D}{n_i^2}\right) \tag{1}$$

where q is the elementary charge, k is the Boltzmann constant, T is the temperature, N_D is the donor doping concentration, and N_A is the acceptor doping density. The low intrinsic carrier concentration of the 4H-SiC material (6.7×10^{-11} cm^{-3}) [3, 25], results in high V_{bi} and voltage drop across the junction (~2.6 V at 1 mA). The high voltage drop across the diode rectifier can induce a considerable on-state power dissipation during the power-switching operation [3]. The forward I-V properties (see Fig. 3(b)) are fitted by the diode current equation to analyze the forward current transport [24]:

$$I_F = I_0 (e^{(qV_F - I_F R_s)/nkT} - 1) \tag{2}$$

where I_F is the measured forward current, I_0 is the reverse saturation current (used as a fitting parameter), V_F is the forward bias voltage, n is the ideality factor, and R_s is the series resistance. The fitted I-V curve yields an ideality factor of 1.6 ± 0.1 (for the linear region of semilog I-V plot) and a series resistance of 1.2 ± 0.2 Ω for the 4H-SiC PiN diode. If the ideal diffusion current and low-injection mechanism entirely govern the forward current, the ideality factor of the diode should be almost equal to unity [3, 24]. The non-ideal effects such as recombination current and high-injection of minority carriers can increase the ideality factor by close to two [24]. In our diode, the ideality factor is intermediate (1.6) between these two ranges. This indicates that the mixed conduction process with recombination and diffusion current transport occurs in the bias region of 1.6 V < V_F < 2.7 V, as similar to the observations of Camara *et al.* [26]. So, it is considered that a negligible current flow occurs for low forward bias V_F < 1.6 V, then the mixed current conduction (recombination and diffusion) process governs the forward current up to 2.7 V, and beyond that series resistance effect comes into the picture. The on-state series resistance (R_s = 1.2 ± 0.2 Ω) contribution mainly arises from the lightly-doped n$^-$ drift layer ($N_D = 7\times10^{14}$ cm^{-3}, ρ = 7.44 Ω-cm). As because, the series resistance influence of n$^+$ substrate ($N_D = 10^{18}$ cm^{-3}, ρ = 5.2 mΩ-cm), p-type layer ($N_A = 6\times10^{17}$ cm^{-3}, ρ = 86.8 mΩ-cm), high-doped p$^+$ region ($N_A = 6\times10^{19}$ cm^{-3}, ρ = 0.87 mΩ-cm) may be insignificant. Nevertheless, the lightly-doped drift layer is necessary for a power diode design to withstand the high breakdown voltage and electric field.

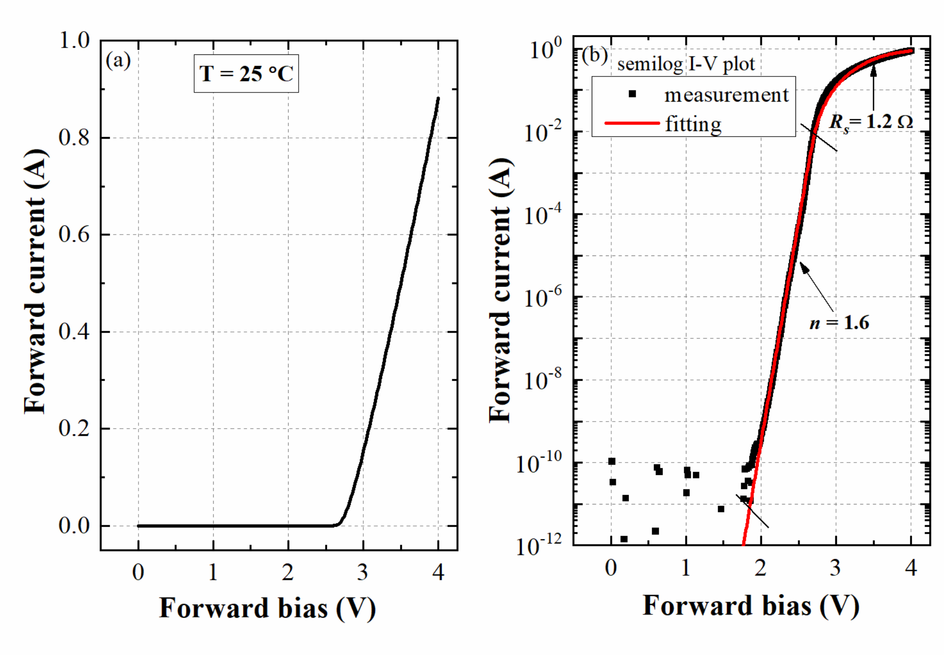

Fig. 3 (a) Forward I-V characteristics of the 4H-SiC PiN diode at 25 °C; (b) forward I-V is fitted by the diode equation.

To understand the temperature-induced variations in the on-state voltage drop and current transport components, the forward I-V characteristics of the 4H-SiC PiN diode are investigated with the increasing temperatures. The forward I-V characteristics of the 4H-SiC PiN diode at different temperatures (25 °C, 75 °C, 110 °C and 150 °C) are displayed in Fig. 4(a). It is noticed that the forward current (I_F) increases with the temperature, due to the augmentation in the intrinsic carrier concentration (n_i) and minority carrier diffusion length (L) [3, 24]. The forward voltage drop across the diode (at 1 mA) is found to decrease with the increasing temperature (2.6 V at 25°C, 2.48 V at 75 °C, 2.4 V at 110 °C, and 2.26 V at 150 °C) due to the reduction in the built-in barrier potential (V_{bi}), as dictated by the Equation (1). Therefore, the on-state power dissipation of the PiN diode rectifier is expected to decrease with the temperature. As the temperature rises, the electrons in the valence band acquire sufficient energy to move into the conduction band, consequently the intrinsic carrier concentration (n_i) upsurges and the Fermi level moves toward the middle of the bandgap. As a collective effect, the built-in barrier potential (V_{bi}) lowers upon increasing the temperature because of the augmented n_i and the Fermi level variation. As the temperature surge accelerate the carrier diffusion process, the minority carrier diffusion length (L_n, and L_p) also increases [3, 24]. It should be noted that the carrier mobility declines with the temperature due to the enhanced lattice phonon scattering (more precisely inter-valley scattering). However, the mobility degradation effects are nullified by the above effects such as reduced built-in barrier potential and increased diffusion length at higher operating temperatures. All these processes decrease the forward voltage drop across the junction and increase the forward current (I_F) with the temperature. As a result, the on-state conduction losses [3] reduce with increasing temperature. Figure 4(b) shows that the ideality factor (n) of the 4H-SiC PiN diode increases with the temperature, possibly due to the accelerated diffusion process (may lead to high-injection of minority carriers).

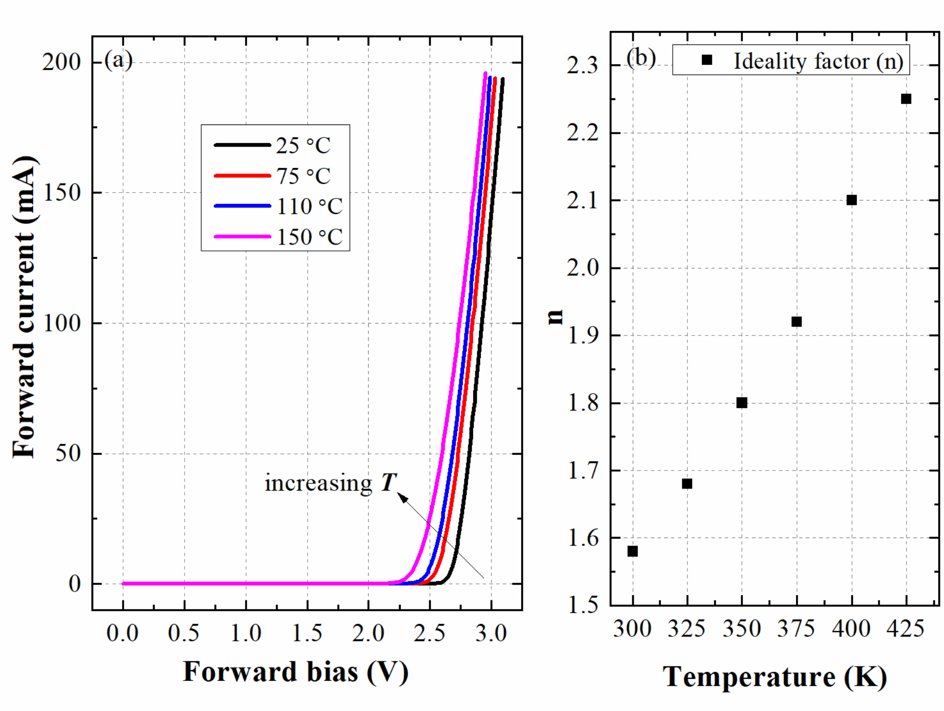

Fig. 4 (a) Forward I-V characteristics of the 4H-SiC PiN diode at different temperatures (25 °C, 75 °C, 110 °C and 150 °C); (b) the ideality factor (n) variation with the increasing temperature.

The reverse I-V characteristics of the 4H-SiC PiN diode at two different temperatures (25 °C and 150 °C) are plotted in Fig. 5. As expected, the diode leakage current increases with the reverse bias voltage, specifying that the reverse saturation current (due to minority carrier generation near the edge of the depletion region, which is independent of reverse bias [24]) is negligible in the 4H-SiC PiN diode. Unlike Schottky barrier diodes (SBDs), the PiN diodes have a buried junction, so the surface trapping are less pronounced. In addition, the JTE and floating rings in the PiN diode structure considerably reduce the electric field crowding around junction edges. Therefore, the thermal generation of carriers via mid-gap traps inside the depletion region is the only possible current conduction mechanism during the reverse bias operation of the 4H-SiC PiN diode. The PiN diode exhibits a low reverse leakage current of 4.9 ± 0.2 nA at 200 V. The reverse I-V characteristics (from 0 V to -200 V) remain unchanged even at 150°C, as seen in Fig. 5. Nonetheless, if the thermal generation current governs the leakage current transport, it should upsurge with the temperature due to the augmented thermal-assisted carrier generation via mid-gap traps. But, there is no change in the reverse leakage current even at 150 °C up to the bias of -200 V. Three possible explanations for this temperature-independent behaviour are: (a) current due to noise (associated with the current sensitivity of the SMU), (b) tunnelling current, and (c) edge leakage current. Since the electric field crowding is reduced by periphery protection, the tunnelling current transport may not occur in the PiN diodes. If the observed leakage current is due to the noise, it may not vary with the reverse bias voltage and also tends to provide random values during each measurement. The linear variation of the leakage current with respect to the reverse voltage may be caused due to the edge leakage current (I_{edge}) [27, 28], as fitted in the Fig. 5:

$$I_{edge} = \frac{V_R}{R_{sh}} \tag{3}$$

where V_R is the reverse voltage, and R_{sh} is the shunt resistance. If the reverse I-V characteristics are linear, the shunt resistance can be calculated from the slope of the linear I-V plot. Accordingly, shunt resistance (R_{ch}) for the 4H-SiC PiN diode is computed as 5.3×10^{11} Ω and the edge leakage current is predicted based on the Equation (3). Nevertheless, the edge leakage current is possible in the unterminated Schottky barrier diodes and its contribution is minimal in the PiN diodes (having buried junction). The reason for the temperature-independent reverse I-V is still unclear at the moment. Hence, reverse I-V measurements should be further carried out beyond -200 V to understand the leakage current transport mechanism, and research studies are underway to clarify this peculiar behaviour.

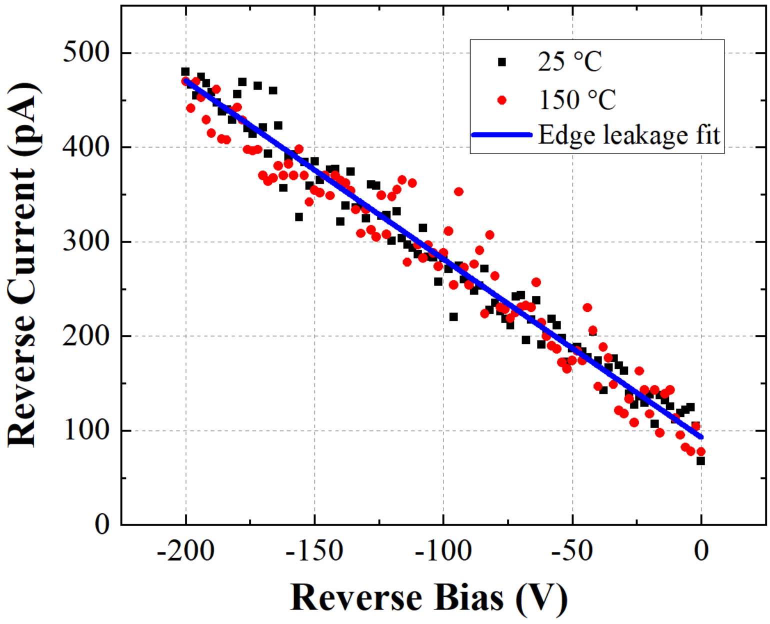

Fig. 5 Reverse I-V characteristics of the 4H-SiC PiN diode measured at 25 °C and 150 °C.

Figures 6 (a) and 6(b) show the C-V and $(1/C')^2$-V characteristics of the 4H-SiC PiN diode at 25 °C; Here *C'* represents the capacitance per unit area (F/cm^2). As a typical behavior, the depletion capacitance decreases with the reverse bias voltage due to the increase in the space charge width [3, 24]. The effective doping concentration of the drift layer can be estimated using the following equation [24]:

$$\left(\frac{1}{C'}\right)^2 = \frac{2(V_{bi}+V_{R})}{q\varepsilon_s N_D} \tag{4}$$

where V_R is the reverse bias voltage, and ε_s is the dielectric constant of the 4H-SiC. From the slope of $(1/C')^2$-V characteristics, the effective doping concentration (N_D) is computed 7.9×10^{14} cm^{-3}; this value is consistent with the specified doping density for the n^- drift layer. The $(1/C')^2$-V plot is found to be linear, as apparent in Fig. 5(b), revealing that the doping density is uniform in the drift layer along the depth. Furthermore, the built-in barrier potential (V_{bi} = ~2.1 V) of the 4H-SiC PiN diode is identified by linearly extrapolating the $(1/C')^2$-V plot to the *x*-axis point where $(1/C')^2 = 0$.

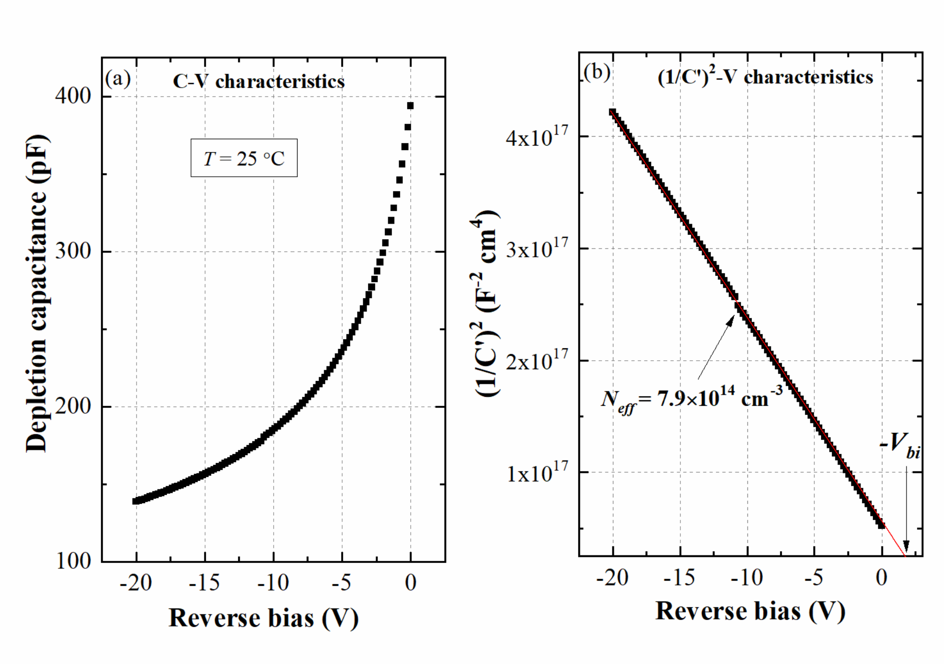

Fig. 6 (a) C-V and (b) $(1/C')^2$-V characteristics of the 4H-SiC PiN diodes obtained at 25 °C.

3.2 Traps in 4H-SiC PiN Diode

Figure 7 shows the capacitance DLTFS (C-DLTFS) acquired with the reduced reverse bias pulse condition (from V_{QR} = -10 V to V_P = -0.1 V) for two different emission (detrapping) transients of T_{E1} = 20.48 ms and T_{E2} = 2.048 s. Each Gaussian-shaped peak in the DLTFS spectrum reveals the existence of an electrically active defect (trap) in the 4H-SiC PiN diode. Negative DLTFS peaks (H1, H2, and H3) are observed for the T_{E1} = 20.48 ms case. In our measurement setup, positive and negative DLTFS peaks correspond to electron trap (positioned below the conduction band at E_C - E_T) and hole trap (located above the valence band at E_V + E_T), respectively. The justification for this observation is given as follows: Generally, the capacitance transients discriminate the majority and minority carrier emission from the trap level in the semiconductor [18, 23]. Assume that, a single electron trap (majority carrier trap) exists in the n-type semiconductor. The trap filling pulse populates the electron traps in the diode, so the depletion capacitance increases because of the reduced depletion width. When the diode is instantaneously switched to the quiescent reverse voltage, the traps inside the depletion region take a finite characteristic time for detrapping, thus the resultant depletion capacitance is lower than its quiescent value due to the presence of trapped electrons in the positively-ionized space charge region [18, 23]. Once the electron emission starts taking place, the depletion capacitance increases with the time, which is recorded as a rising capacitance transient during DLTFS measurements [19]. Similarly, hole trap in the n-type semiconductor (minority carrier emission) can induce a decreasing capacitance transient during the detrapping process [18, 19, 23]. As a result, the sign of the capacitance transient decides the direction of the peak position in the DLTFS spectra. In our measurement setup, positive and negative DLTFS peaks correspond to electron trap (positioned below the conduction band at E_C - E_T) and hole trap (located above the valence band at $E_V + E_T$), respectively.

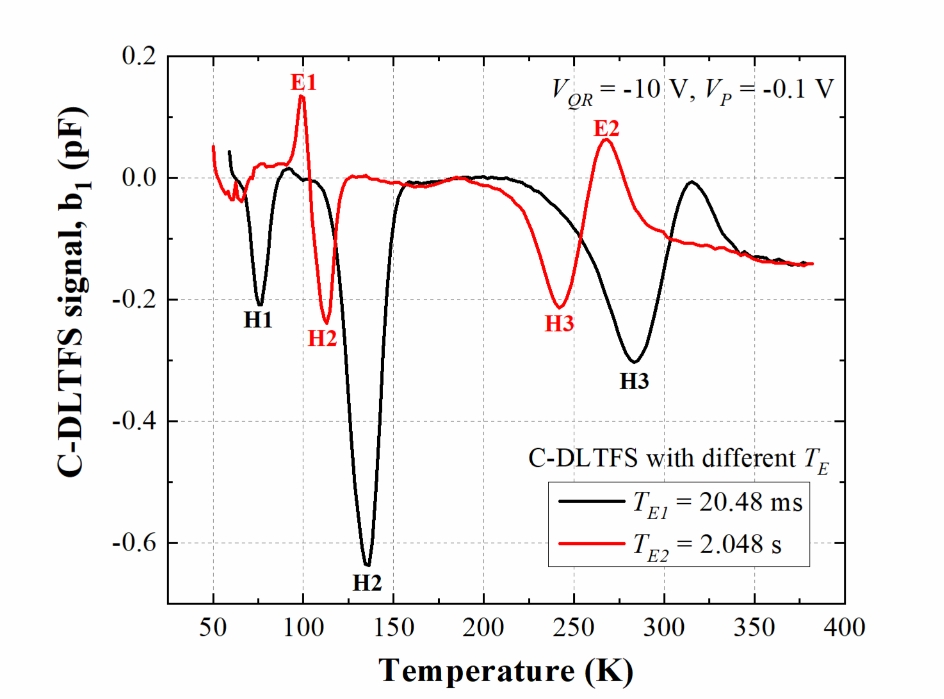

Fig. 7 Capacitance DLTFS (C-DLTFS) acquired with the reduced reverse bias pulse (from V_{QR} = -10 V to V_P = -0.1 V) for two different emission (detrapping) transients of T_{E1} = 20.48 ms and T_{E2} = 2.048 s.

The Arrhenius analysis [18, 19, 29] of the DLTFS peak yields the activation energy (E_a) and capture cross-section (σ) for the hole traps H1 (E_V + 0.16 eV, 5.7×10^{-13} cm^2), H2 (E_V + 0.3 eV, 10^{-15} cm^2), and H3 (E_V + 0.63 eV, 2.2×10^{-14} cm^2). The trap concentration (N_T) is calculated from the maximum peak position (ΔC) in the DLTFS spectrum, as per the equation [18, 19]:

$$N_T \approx 2N_D \frac{\Delta C}{C_R} \tag{5}$$

where C_R is the quiescent reverse bias capacitance. The computed trap density for the hole traps H1, H2, and H3 is 5×10^{12} cm^{-3}, 1.5×10^{13} cm^{-3}, and 6.8×10^{12} cm^{-3}, respectively. Both positive (E1, and E2), and negative (H2, and H3) peaks are detected in the C-DLTFS acquired with T_{E2} = 2.048 s case. The trap parameters for the electron traps are computed as E1 (E_C – 0.19 eV, 3×10^{-18} cm^2, and 3.2×10^{12} cm^{-3}) and E2 (E_C – 0.67 eV, 6.2×10^{-15} cm^2, and 1.4×10^{12} cm^{-3}). Identical trap signatures are determined for the traps H2, and H3 for the T_{E2} = 2.048 s case, but their peak position occurred at a lower temperature due to the prolonged detrapping transient time ($T_{E2} > T_{E2}$). The electron traps are detected only at the longer emission transient (T_{E2} = 2.048 s), which may be due to the extended available time for the carrier emission (detrapping) process and the low trap density for E1 and E2 (N_T < 5×10^{12} cm^{-3}). On the other hand, the hole traps are visible in both cases due to their high trap concentration (N_T > 5×10^{12} cm^{-3}). It is visualized that the peaks E2 and H3 are merged and produced a single peak at ~282 K for the shorter detrapping transient T_{E1} = 20.48 ms (overlapped emission rate is another possibility); further investigations are required to support this hypothesis. Overall, three hole traps H1 at E_V + 0.16 eV, H2 at E_V + 0.3 eV, and H3 at E_V + 0.63 eV and two electron traps E1 at E_C – 0.19 eV and E2 at E_C – 0.67 eV are identified from the C-DLTFS measurements.

Figure 8 displays the current DLTFS (I-DLTFS) spectra obtained with the reduced reverse bias pulse (V_{QR} = -10 V to V_P = -0.1 V) for two emission transients of T_{E1} = 20.48 ms and T_{E2} = 2.048 s. Unlike C-DLTFS, only one distinct negative peak T6 is observed for both cases (T_{E1} and T_{E2}). The peak maximum temperature for T6 is noted ~326K (for T_{E1} = 20.48 ms), and ~278 K (for T_{E2} = 2.048 s). The activation energy and capture cross-section of the trap T6 are deduced ~0.68 eV and 2×10^{-15} cm^2, respectively. Unlike the capacitance transients, the current transient signals have the same sign irrespective of carrier emission, since the applied voltage (electric field) directs the current flow in a one direction [18, 19, 22]. Thereby, the resulting DLTFS peaks are always in the same direction, as shown in Fig. 8. The I-DLTS characterization cannot differentiate the electron and hole traps in the diode [18, 19, 22], so the energy location of the trap T6 is not identified from the I-DLTS. However, a correlation is found between the trap activation energies of T6 (0.68 eV), E2 (0.67 eV), and H3 (0.63 eV).

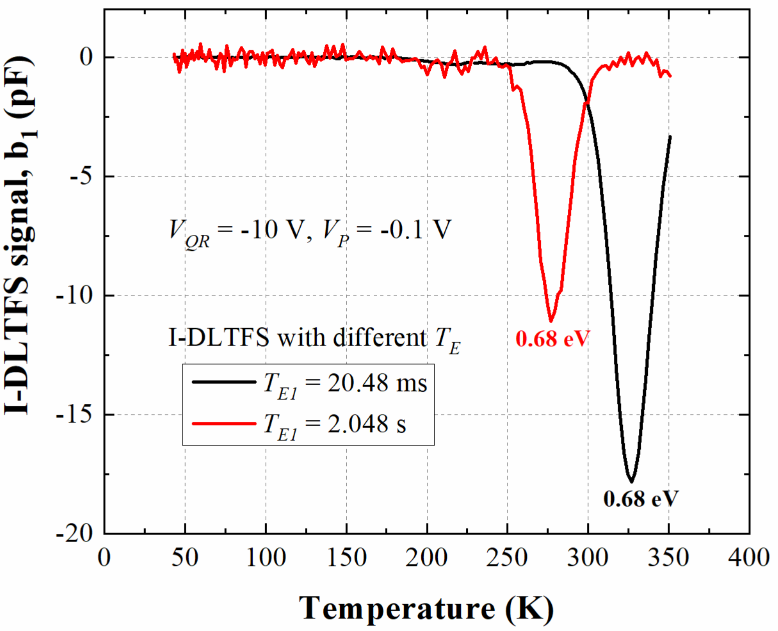

Fig. 8 Current DLTFS (I-DLTFS) spectra obtained with the reduced reverse bias pulse for two different emission transients of T_{E1} = 20.48 ms and T_{E2} = 2.048 s.

The TSCAP spectroscopy of the 4H-SiC PiN diode measured at the reverse bias V_R = -10 V is plotted in Fig. 9. A rapid increment in the depletion capacitance (i.e. rising TSCAP step E1') is noticed for temperatures ranging from 95 K and 115 K. For the n-type semiconductor, this growing TSCAP step arises due to the electron emission process from the trap level located below the conduction band edge at E_C – E_T (electron trap). The thermal activation energy of the trap (E_T) can be estimated from the mid-temperature point ($T_{1/2}$) of the TSCAP step signal (E1') using the equation [18, 23]:

$$E_T = kT_{1/2} \ln\left[\frac{vkT_{1/2}^2}{q(E_T + 2kT_{1/2})}\right] \tag{6}$$

The escape frequency factor [18, 23] value ($v = \sigma_n N_C v_{th}$) is selected based on the C-DLTFS results and the energy level, and capture cross-section for the TSCAP step E1' are calculated E_C – 0.2 eV and 5×10^{-18} cm^2; these values are similar to the trap parameters of E1 (E_C – 0.19 eV, and 3×10^{-18} cm^2). Accordingly, it is considered that the DLTFS signal E1 and the TSCAP step E1' are produced by the same trap at E_C – 0.19 eV. Note that, the characterization principle of the DLTFS and TSCAP techniques is entirely different. In the DLTFS method, the traps are filled at frequent temperature intervals during the thermal scan, and subsequently the emission (detrapping) transient is measured. On the other hand, the traps are populated only at a specified low temperature (T_0, no trap filling after) in the TSCAP procedure [5, 18, 23]. During the thermal ramp-up scan, the changes in the diode depletion capacitance are recorded versus temperature at a fixed reverse voltage. So, the TSCAP detection sensitivity is poor for the low trap density (N_T) cases, while the DLTFS is more effective in identifying the traps with $N_T < 10^{12}$ cm^{-3}. Due to this dissimilarity, the traps E2, H1, H2, and H3 are not determined from the TSCAP spectroscopy. Since the temperature-induced changes in the depletion capacitance are measured at a stable reverse bias voltage (under equilibrium condition, not under the transient), the TSCAP characterization is often referred to as equilibrium thermal scan.

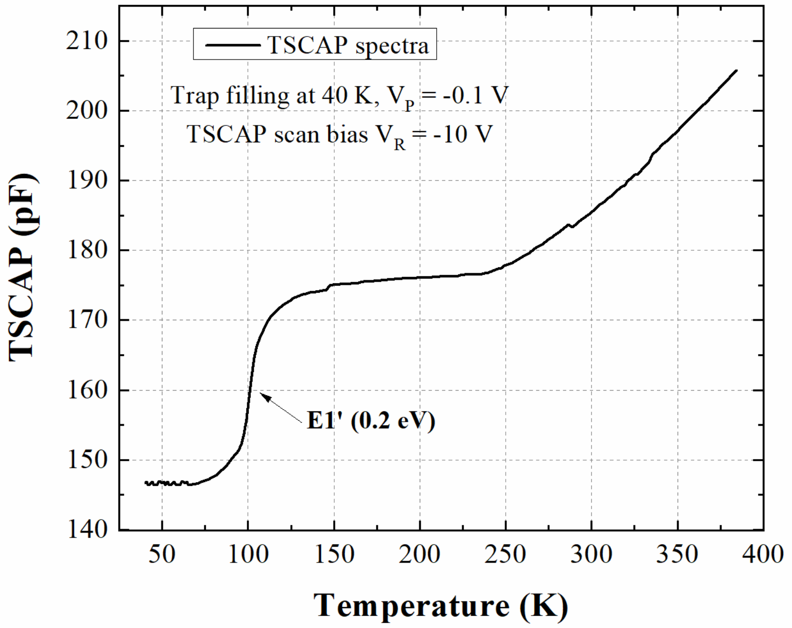

Fig. 9 The TSCAP spectroscopy of 4H-SiC PiN diode measured at the reverse bias V_R = -10 V (trap filling at 40 K by reducing the reverse bias to -0.1 to populate the majority carrier traps).

The trap parameters in the 4H-SiC PiN diode identified through the C-DLTFS, I-DLTFS, and TSCAP measurements are summarized in Table 1. The shallow electron trap E1 at E_C – 0.19 eV is produced due to the omnipresent Ti impurities in the n-type 4H-SiC epitaxial layer [9, 25, 30]. The carbon-vacancy (V_C) related carrier lifetime defect $Z_{1/2}$ (performance limiting defect in the n-type 4H-SiC layers) may generate the deep-level electron trap E2 at E_C – 0.67 eV in the diode [5, 9, 25, 30]. The shallow hole trap H1 at E_V + 0.16 eV is attributed to the intrinsic L-center defect [31] and Al acceptor impurities [31]. The possible defects for the hole trap H_2 at E_V + 0.3 eV are boron (B) and gallium (Ga) acceptor impurities [31] and UK1 [32] defects observed in the p-type 4H-SiC epilayers. The deep-level hole trap H3 at E_V + 0.63 eV is ascribed to the boron-related D-center state [30, 21] and the HK1 [23] defect identified in the p-type 4H-SiC epitaxial layers. The energy location (electron or hole trap) of trap T6 is not identified from the I-DLTS characterization. Anyhow, the activation energy of the deep-level trap T6 at 0.68 eV are related to the HK1 [32] and $Z_{1/2}$ [5, 9, 25, 30] defects. Among these, the electron traps such as Ti and $Z_{1/2}$ are omnipresent defects in the n-type 4H-SiC epitaxial layers. These traps were also observed in the 4H-SiC PiN diodes not having the periphery protections (JTE and floating rings) [10, 12]. The hole traps at E_V + 0.16 eV, E_V + 0.3 eV, and E_V + 0.63 eV were identified in the p-type 4H-SiC layers [31, 32]. However, these hole traps were not detected in the unprotected 4H-SiC PiN diodes [10, 12]. These points suggest that the hole traps H1, H2, and H3 may originate from the Al^+ ion-implanted JTE and floating JTE ring regions of the 4H-SiC PiN diode. The emission time constant (τ_e) for the traps is computed using the carrier emission rate (e_m) equation [23, 25]:

$$\tau_e = \frac{1}{e_m} = \frac{g}{\sigma N_{C/V} v_{th}} \exp\left(\frac{E_a}{kT}\right) \tag{7}$$

where g is the degeneracy factor, σ is the trap capture cross-section, $N_{C/V}$ is the effective density of states in the conduction or valence band for the electron and hole traps, and v_{th} is the thermal velocity of carriers [23, 25]:

$$v_{th} = \sqrt{\frac{3kT}{m^*}} \tag{8}$$

where m^* is the electron or hole effective mass for the electron or hole traps. The $N_{C/V}$ and m^* are chosen based on the values reported by Kimoto and Cooper [25]. Accordingly, the emission time constant (τ_e) for the traps E1 (0.85μs), E2 (77.7 ms), H1 (4.6 ps), H2 (0.59 μs), H3 (9.2 ms), and T6 (354 ms) are estimated at 300 K. So, the emission time constant is longer (τ_e > ms, resulting in slower emission rates) for the deep trap energies (E_a > 0.6 eV) and low capture cross-sections ($\sigma < 10^{-15}$ cm^2). Accordingly, the deep-level traps such as E2 at E_C – 0.67 eV, H3 at E_V+0.63 eV, and T6 at 0.68 eV may play a crucial role in reducing the minority carrier lifetime of the 4H-SiC PiN diode. Hence, the forward current density is anticipated to decrease (on-state voltage drop and conduction loss increase) due to the trapping effect. However, extensive TCAD device simulation studies are required to evaluate the trapping-induced changes (due to the defects) in the electrical characteristics of the 4H-SiC PiN diodes; these are the future scopes of the current work.

Table 1 Trap parameters in 4H-SiC PiN diodes identified from C-DLTFS, I-DLTFS, and TSCAP.

Trap Label	Used Technique	Energy level E_T (eV)	Capture cross-section σ (cm^2)	Trap density N_T (cm^{-3})	Possible defects reported in the literature
E1, E1’	C-DLTFS, TSCAP	E_C – 0.19	(3-5)×10^{-18}	3.2×10^{12}	Ti impurity [9], [21]
E2	C-DLTFS	E_C – 0.67	6.2×10^{-15}	1.4×10^{12}	$Z_{1/2}$ [5], [9], [21]
H1	C-DLTFS	E_V + 0.16	5.7×10^{-13}	5×10^{12}	L-center [22], Al [22]
H2	C-DLTFS	E_V + 0.3	10^{-15}	1.5×10^{13}	B [22], Ga [22], UK1 [23]
H3	C-DLTFS	E_V + 0.63	2.2×10^{-14}	6.8×10^{12}	D-center [21], [22], HK1 [23]
T6	I-DLTFS	0.68	2×10^{-15}	--	HK1 [22] or $Z_{1/2}$ [5], [9], [21]

4 Conclusion

The electrical and trap characterization studies are carried out for the 4H-SiC PiN power diodes. The ideality factor of 1.6 and the series resistance of 1.2 Ω of the diode are extracted from the forward I-V at 25 °C. The intermediate ideality factor (1.6) indicates that the mixed conduction process with recombination and diffusion current transport occurs in the linear region of semilog I-V plot. The forward voltage drop across the diode (from 2.6 V at 25 °C to 2.26 V at 150 °C) decreases with the temperature rise due to the associated reduction in the built-in barrier potential. The effective doping concentration (7.9×10^{14} cm^{-3}) of the drift layer and built-in barrier potential (2.1 V at 25 °C) of the diode are computed from the $(1/C')^2$-V properties. The C-DLTFS results show three hole traps H1 at E_V + 0.16 eV, H2 at E_V + 0.3 eV, and H3 at E_V + 0.63 eV and two electron traps E1 at E_C – 0.19 eV and E2 at E_C – 0.67 eV in the 4H-SiC PiN diodes. The deep-level trap at 0.68 eV is identified from I-DLTFS, and the same trap E1' at E_C – 0.2 eV is detected from the TSCAP spectroscopy. Among these, the electron traps E1 and E2 are omnipresent in the n-type 4H-SiC epitaxial layers. It is considered that the hole traps H1, H2, and H3 may originate from the Al^+ ion-implanted JTE and floating JTE ring regions of the 4H-SiC PiN diode. It is anticipated that the deep-level traps such as E2 at E_C – 0.67 eV, H3 at E_V+0.63 eV, and T6 at 0.68 eV play a crucial role in reducing the minority carrier lifetime of the 4H-SiC PiN diode.

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Author Contributions
The author contributions to this manuscript are given as follows: P. Vigneshwara Raja: Conceptualization, Data curation, Formal analysis, Investigation, Writing - original draft, Writing - review & editing. Christophe Raynaud: Investigation, Methodology, Supervision, Validation, Visualization, Project administration. Besar Asllani: Investigation, Data curation, Investigation, Formal analysis, Writing - review & editing. Herve´ Morel: Investigation; Supervision, Validation, Project administration, Writing - review & editing. Dominique Planson: Investigation, Methodology, Supervision, Funding acquisition, Project administration, Validation, Visualization, Writing - review & editing.

Data Availability
The datasets analysed during this study are available from the corresponding author upon reasonable request.

Declarations
The authors declare no conflicts of interest.

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