Robust Al0.23Ga0.77N channel HFETs on bulk AlN for high voltage power electronics

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J. Mehta [a,*], I. Abid [a], R. Elwaradi [b], Y. Cordier [b], F. Medjdoub [a]

[a] IEMN, CNRS, Université de Lille, 59650 Villeneuve d'Ascq, France
[b] Université Côte d'Azur, CNRS, CRHEA, rue Bernard Grégory, 06560 Valbonne, France

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ABSTRACT

$Al_xGa_{1-x}N$ heterojunction FETs (HFETs) have been an eye catcher for high voltage power electronics with its potential to outperform the predecessors by virtue of high critical breakdown field of the material, which can be tuned by varying Al mole-fraction. In this work, we demonstrate $Al_{0.23}Ga_{0.77}N$ channel HFETs on bulk AlN with a maximum drain current density > 300 mA/mm and a specific R_{on} = 4 mΩ·cm^2. A buffer electric breakdown field >10 MV/cm was measured. A high voltage robustness comparison of $Al_{0.23}Ga_{0.77}N$ channel HFETs and thin GaN HFETs close to their respective hard breakdown voltages is also concluded, which reveals the superior reliable operation of $Al_{0.23}Ga_{0.77}N$ channel HFETs up to 80% of hard breakdown voltages along with a consistent I_{ON}/I_{OFF} ratio subsequent to 2000V voltage sweep.

1. Introduction

Insulated Gate Bipolar Transistors (IGBTs) and Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) have been leading the high voltage power electronics since decades delivering optimum performances withstanding multiple kilovolts. In 2013, *Wolfspeed, Inc. (formerly CREE, Inc.)* demonstrated the highest rated SiC IGBTs with an active area 42 mm^2 with a breakdown voltage of 20.7 kV using a drift layer of 160 μm corresponding to a peak electric field of 1.58 MV/cm [1]. This structural thickness eventually increases device footprint and bulk in high voltage convertor modules. Nowadays, GaN high electron mobility transistors (HEMTs) and SiC MOSFETs are leading the industrial development of high voltage and radio frequency (RF) power electronics with highest rated commercial devices available up to 1700V and 325A with junction temperatures up to 423K [2]. However, for lateral device architecture the critical electric field strength of these materials are already at peak that is < 3.4 MV/cm, limiting their operation in multiple kilovolt regime. In the last decade, ultra-wide band gap (UWBG) semiconductors such as AlGaN, AlN that can provide up to 15 MV/cm electric breakdown field have shown prominent candidacy for the development of high voltage FETs paving a way towards thinner heterostructures alongside reducing the overall device dimension. Nevertheless, the increase in Al mole fraction in AlGaN channel eventually makes the contacts rectifying on applying the conventional Ti/Al/Ni/Au metal stack followed by rapid thermal annealing (RTA) < 800°C. First demonstration of $Al_{0.53}Ga_{0.47}N/Al_{0.38}Ga_{0.62}N$ HEMTs was made by *T. Nanjo et.al* in 2008 with breakdown voltage of 1650V for gate-drain spacing (L_{GD}) =10 μm [3]. In 2019, *Sandia National Laboratories, USA* demonstrated extreme temperature operation of $Al_{0.85}Ga_{0.15}N/Al_{0.7}Ga_{0.3}N$ HEMTs with 58% reduction in DC output with low leakage current at 500°C along with minimal loss in switching current [4]. In 2021, *I. Abid et.al*, demonstrated $AlN/Al_{0.5}Ga_{0.5}N$ transistors withstanding up to 4300V with leakage current density below 1 μA/mm with L_{GD}= 40 μm.

Many different types of substrates such as sapphire, silicon, AlN etc. have been utilized to grow high quality AlGaN channel heterostructures and demonstrate their extreme voltage and temperature performances for the next generation of power devices [5–7]. The major drawback of AlGaN/AlGaN heterostructures is the poor electron mobility in the 2-dimensional electron gas (2-DEG) due to high alloy disorder scattering, which brings low output currents at device level as compared to GaN HEMTs. In 2022, a detailed study on the charge control and transport properties of polarization induced 2-DEGs in AlN/AlGaN/AlN double heterostructures with Al mole fraction up to 0.74 has been shown by *J. Singhal et al.* giving an overview on alloy scattering based on temperature dependent transport properties [8]. The quality of 2-DEG also depends on the choice of substrate used for the epitaxy. Thus, the 2-DEG properties and overall crystal quality of AlGaN/AlGaN

* Corresponding author.
E-mail address: jashrinku.mehta@univ-lille.fr (J. Mehta).

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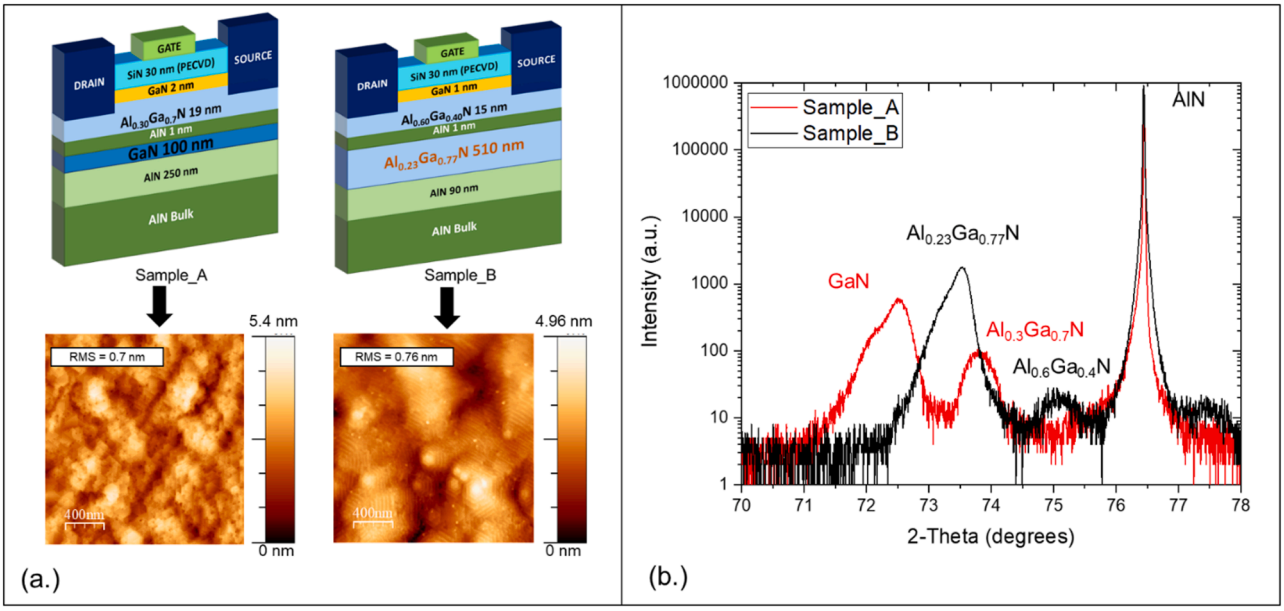

Fig. 1. (a.) Schematic cross sectional diagram of $Al_{0.3}Ga_{0.7}N$ /GaN and $Al_{0.60}Ga_{0.40}N$/ $Al_{0.23}Ga_{0.77}N$ channel Heterostructures along with their respective AFM scans and (b.) HRXRD ω/2Θ scans of GaN and AlGaN.

heterostructures may be improved by employing bulk AlN substrates. In this study, we compare sub-micron GaN channel HEMT with $Al_{0.23}Ga_{0.77}N$ channel HEMT fabricated on bulk AlN, analyze their transfer and output characteristics along with their high voltage operation.

High voltage reliability and robustness of FETs are critical prerequisites for pushing the devices towards real applications. Extensive work have been done over the years on GaN HEMTs for RF and power devices, to understand the trapping, de-trapping and material degradation mechanisms using time dependent step stress measurement technique [9–15]. For instance, 650 V lateral GaN power switching are qualified by several industrials, but are significantly overdesigned because of the absence of avalanche breakdown, which still plague large volume market penetration. Therefore, enlarging the safe operating area closer to the breakdown voltage enables reduced device dimensions for a given voltage range. In this work, we experimentally demonstrate reliability and robustness of these devices close to their hard breakdown voltages, eventually evaluating safe operating voltages.

2. Structural Properties and Device Fabrication

The heterostructures were grown by ammonia source molecular beam epitaxy (NH_3-MBE) in a Riber Compact 21 reactor [16] on c-plane Al-polar 2-in. diameter commercial bulk AlN substrate from HexaTech, Inc. (AlN-10 series). First, a 90 nm and a 250 nm thick AlN buffer layer was regrown in the 850-900°C temperature range for AlGaN channel heterostructure and for GaN channel heterostructure respectively [17, 18]. Then, the growth temperature was reduced to 790-800°C for both heterostructures to grow the remaining epilayers as shown in Fig. 1a. Atomic force microscopy (AFM) confirms the smoothness of the surface for both heterostructures with root mean square roughness (RMS) below 1 nm for scans on 2 × 2 μm^2 and 10 × 10 μm^2 areas. High-resolution X-ray diffraction (HRXRD) analysis as shown in Fig. 1b indicates that the strain relaxation rate of the GaN channel layer is limited to 71% and the full width at half maximum (FWHM) of the (302) omega scan peak corresponding to this layer is 0.7°. These results indicate that the GaN thickness is not sufficient to efficiently filter the majority of threading dislocations nucleated at the interface with the AlN buffer layer as observed in a series of similar structures grown with GaN channel thickness varying from 8 nm to 500 nm [17]. On the other hand, the $Al_{0.23}Ga_{0.77}N$ channel HRXRD analysis reveals that the layer is almost entirely strain relaxed (86% relaxation rate). The FWHM of the (302) omega scan peak corresponding to this layer is 0.64°. Therefore, $Al_{0.23}Ga_{0.77}N$ channel has slightly better crystal quality than GaN channel heterostructure with less threading dislocations owing to the smaller lattice mismatch strain with AlN combined with a larger thickness. Furthermore, as the main part of dislocations is nucleated and bent in the vicinity of the channel/AlN interface [17], one main difference between both structures is that the thicker channel allows to increase the distance between the 2DEG induced at the top of the channel and the defective bottom interface.

Device Fabrication started by partially etching the AlGaN barrier in both cases using BCl_3/SF_6 chemistry with inductively coupled plasma (ICP) etching followed by surface wet treatment using buffer oxide etch solution. Electron beam evaporation of Ti/Al/Ni/Au contacts was performed in a Plassys MEB550SL followed by a RTA of 825°C and 850°C for GaN and AlGaN channel HFET, respectively. The devices were mesa isolated by ICP all the way down to AlN substrate. Prior to e-beam evaporation of Ni/Au gate contacts, a 30 nm SiN dielectric layer was deposited by plasma enhanced chemical vapor deposition (PECVD) to passivate the device surface. The L_{GD} in the mask is varied from 5-40 μm whereas the gate length (L_G) is 3 μm and the gate-source spacing (L_{GS}) is 2.5 μm. Finally, Ti/Au pads were evaporated concluding the metal insulator semiconductor (MIS)-HFETs fabrication process.

Table 1
Hall Effect measurements at room temperature.

Sample	Sheet Resistance [ohm/sq.]	Mobility [$cm^2/V.s$]	Concentration [cm^{-2}]
GaN channel	895	840	8×10^{12}
$Al_{0.23}Ga_{0.77}N$ channel	1550	342	1.18×10^{13}

3. Device Characterization and Results

Hall measurements were performed on wafer using Van der Pauw pattern. The 2-DEG mobility of GaN channel device is as expected to be degrading with channel downscaling due to increased scattering effects and possible involvement of regrowth interface which is much closer to

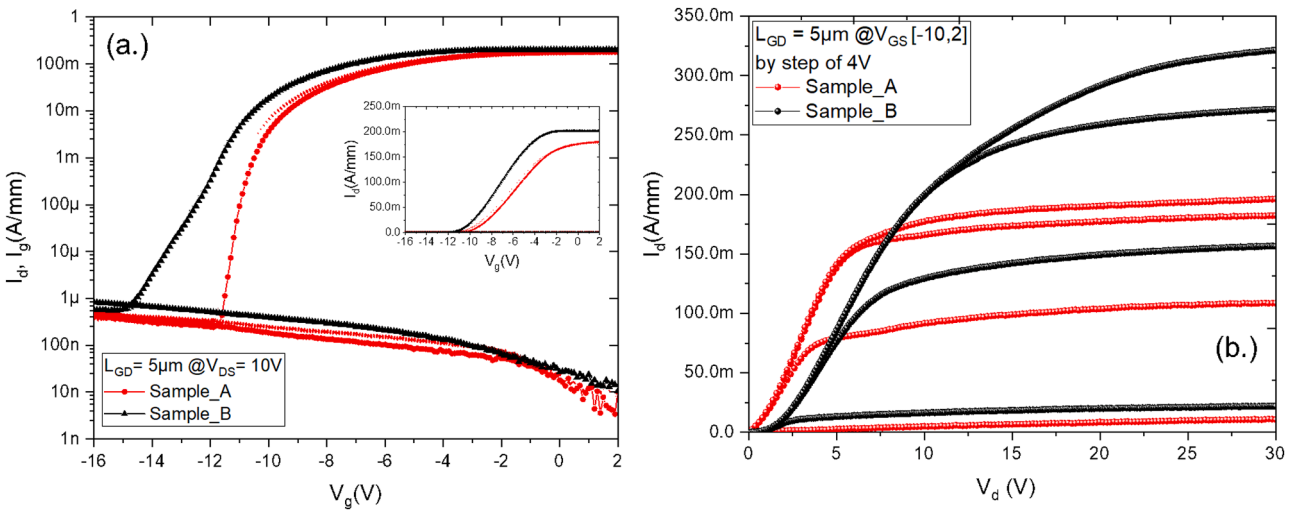

Fig. 2. (a.) Transfer characteristics with forward and reverse sweeps and (b.) Output characteristics up to V_{DS}= 30V for V_{GS} = [-10,-6,-2, 2] V of $Al_{0.3}Ga_{0.7}N$ /GaN and $Al_{0.60}Ga_{0.40}N$/ $Al_{0.23}Ga_{0.77}N$ channel MIS-HFETs.

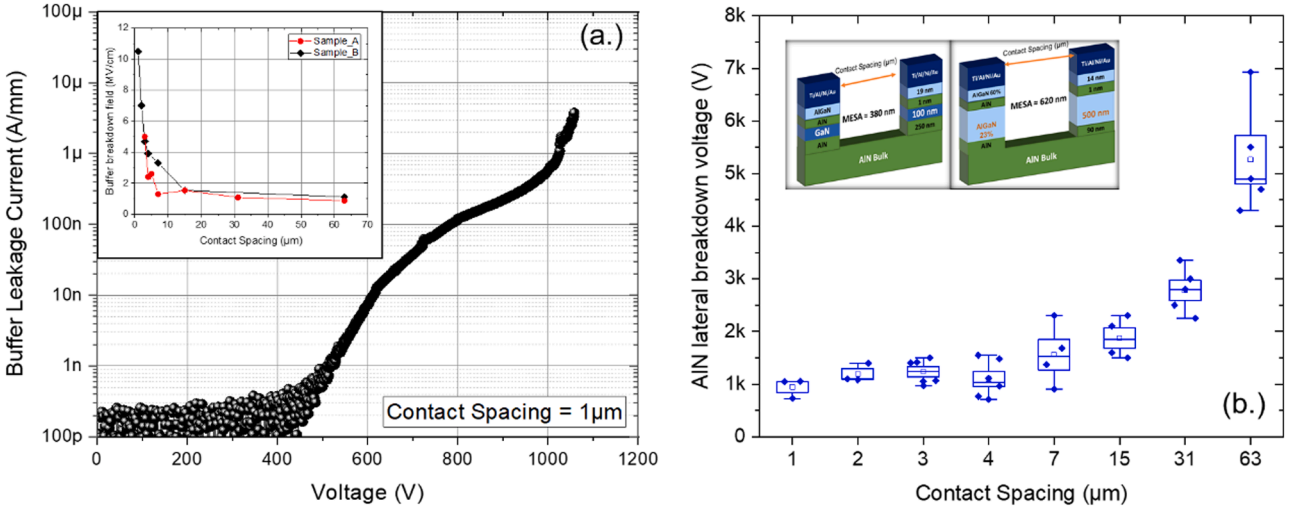

Fig. 3. (a.) Buffer leakage current characteristics for 1µm contact spacing and (b.) Mean values of AlN lateral breakdown voltage for various contact spacing of $Al_{0.3}Ga_{0.7}N$ /GaN and $Al_{0.60}Ga_{0.40}N$/ $Al_{0.23}Ga_{0.77}N$ channel MIS-HFETs.

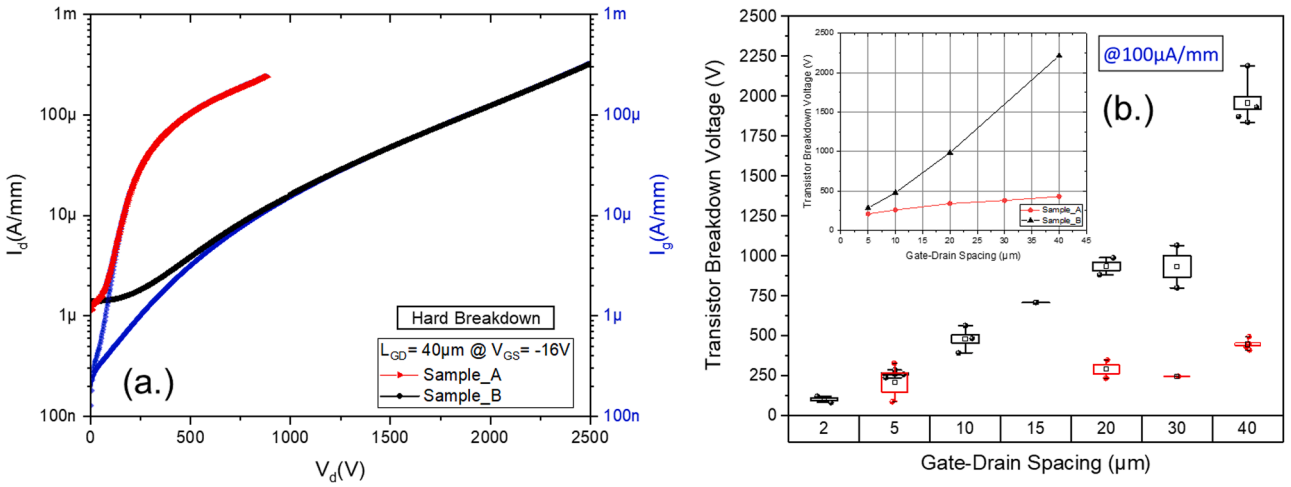

Fig. 4. (a.) Transistor hard electrical breakdown characteristics for a gate-drain spacing of 40 µm at V_{GS}= -16V, (b.) Mean values of transistor blocking voltage for various gate drain spacing of $Al_{0.3}Ga_{0.7}N$ /GaN and $Al_{0.60}Ga_{0.40}N$/ $Al_{0.23}Ga_{0.77}N$ channel MIS-HFETs.

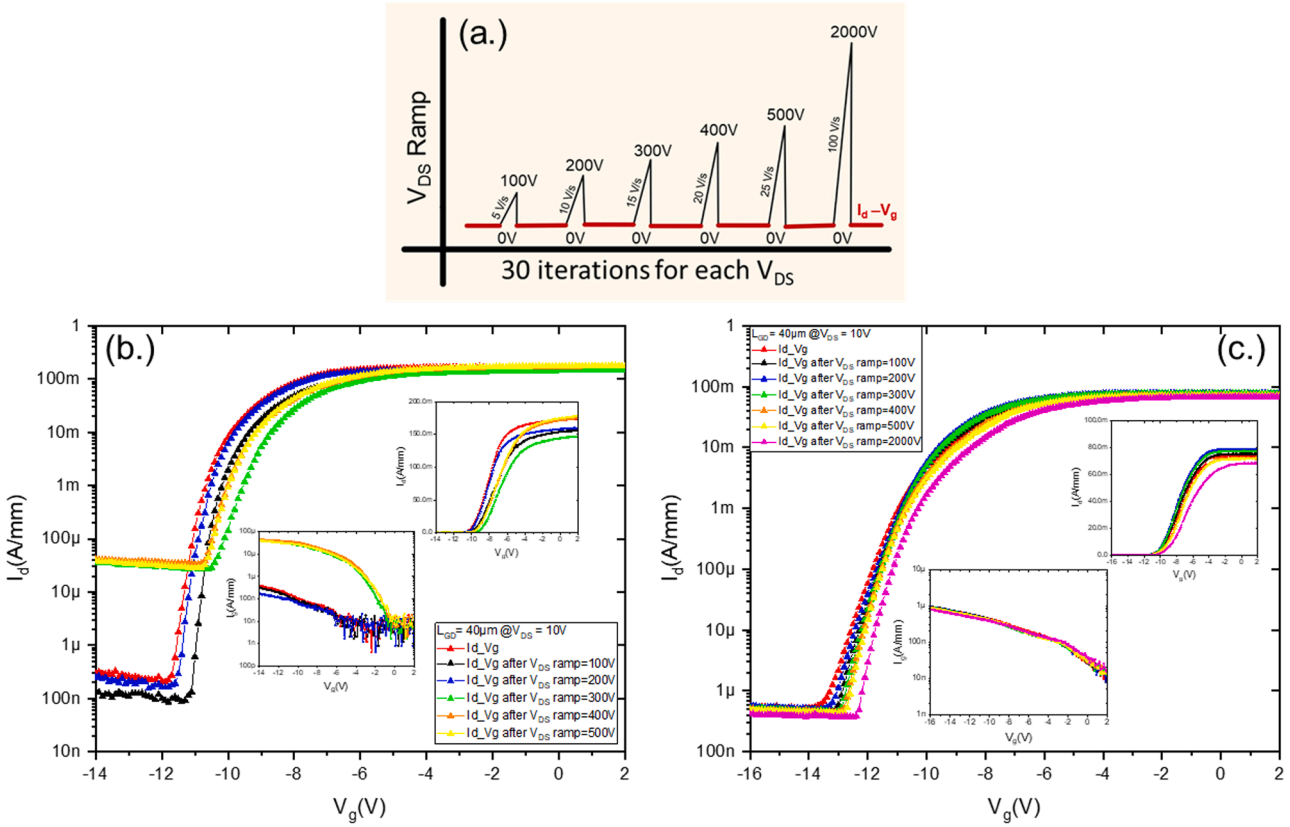

Fig. 5. (a.) Robustness test schematic for various V_{DS} ramp voltages, (b.) Transfer characteristics measured after each V_{DS} ramp for $Al_{0.3}Ga_{0.7}N$ /GaN and (c.) Transfer characteristics measured after each V_{DS} ramp $Al_{0.60}Ga_{0.40}N$/ $Al_{0.23}Ga_{0.77}N$ channel MIS-HFETs with their insets showing gate leakage current density.

the 2DEG than AlGaN channel HFET [19]. The GaN channel HFET showed around 840 cm^2/(V.s) for 100 nm thick channel, which is typically above 1500 cm^2/V.s for thick GaN channel [17]. The AlGaN channel HEMTs deliver a decent electron mobility of about 340 cm^2/(V.s) with a 2DEG electron density in the range of 10^{13} cm^{-2} as shown in Table 1. High voltage electrical measurements were carried out using Keysight B1505A Power Device Analyzer/Curve Tracer together with Keysight N1268A Ultra High Voltage Expander Unit, with samples immersed in fluorinert FC-40 to avoid arcing in air. The transfer characteristics of the samples are shown in Fig. 2a at drain-source voltage (V_{DS}) = 10V along with their respective gate-leakage current characteristics. It can be observed that the measured devices have low trapping below gate as confirmed by the low hysteresis between forward and reverse transfer characteristics. The output characteristics of GaN and $Al_{0.23}Ga_{0.77}N$ channel HFETs as shown in Fig. 2b, reveals a maximum drain current density (I_{DS}) of around 180 mA/mm and 320 mA/mm respectively. The specific R_{on} calculated at V_{GS}= 0V in the linear regime is around 4 mΩ.cm^2 for transistors with L_{GD}= 5 µm for both devices despite the ohmic contact resistances that can still be optimized. Over the last decade, many research groups are working towards the development of different techniques such as graded contacts, doped barrier contacts, various metal stack scheme to obtain ohmic contact resistance as low as 1.9×10^{-6} Ω cm^2 [20–22].

The AlN lateral breakdown characteristics for a 1 µm contact spacing with contact area of 100 µm × 100 µm is shown in Fig. 3a with an electrical breakdown voltage mean value > 1000V for a leakage current density < 10 µA/mm. The buffer breakdown field for both structures can be seen in the inset of Fig. 3a as high as 10 MV/cm for low contact spacing revealing the potential of UWBG materials. The AlN two terminal breakdown characteristic with different contact spacing is shown in Fig. 3b with breakdown voltages reaching 7kV for 63µm contact spacing, the inset diagram shows the mesa height of 380 nm and 620 nm for GaN and $Al_{0.23}Ga_{0.77}N$ channel HEFTs respectively well inside the AlN substrate.

The 3-Terminal breakdown characteristics (see Fig. 4a) shows that the hard breakdown is initiated by gate-leakage current in both the samples. $Al_{0.23}Ga_{0.77}N$ channel HFETs provides up to 4 times higher breakdown voltage (V_{BK}= 2500V) than thin GaN channel HFETs for large L_{GD}. Fig. 4b shows transistor blocking voltage variation with different gate-drain spacing fixed at a gate leakage current density of 100 µA/mm. As expected, this reveals that $Al_{0.23}Ga_{0.77}N$ channel HFETs hold 5 times more blocking voltage per micron than GaN channel HFETs.

4. Robustness Test at High Voltages

We demonstrate an off-state stress experiment based on ramping V_{DS} of transistors with L_{GD}= 40 µm close to the hard breakdown voltage for GaN and $Al_{0.23}Ga_{0.77}N$ channel HFETs. As shown in Fig. 5(a), the devices were ramped up to multiple voltages in steps. The measurements were repeated 30 times at each V_{DS} in order to stabilize the device off-state leakage path and thus detect any device degradation. Each V_{DS} ramp is completed within 20s. After each ramp, the transfer characteristics of the devices were measured within 10s. It can be noticed that off-state leakage current density is quite stable until V_{DS} ramp = 200V followed by a two-fold increase in gate leakage current from V_{DS} ramp = 300V for GaN channel HFETs. This creates an irreversible gate current leakage path (see Fig. 5b) checked after several weeks confirming the permanent degradation which may be supported by the inverse piezoelectric effects [10]. $Al_{0.23}Ga_{0.77}N$ channel HFETs shows excellent performance with stable device operation up to 2000V (close to hard breakdown voltages) as shown in Fig. 5c. The superior robustness of $Al_{0.23}Ga_{0.77}N$ channel HFETs under high voltages reflects the benefit of using wider bandgaps.

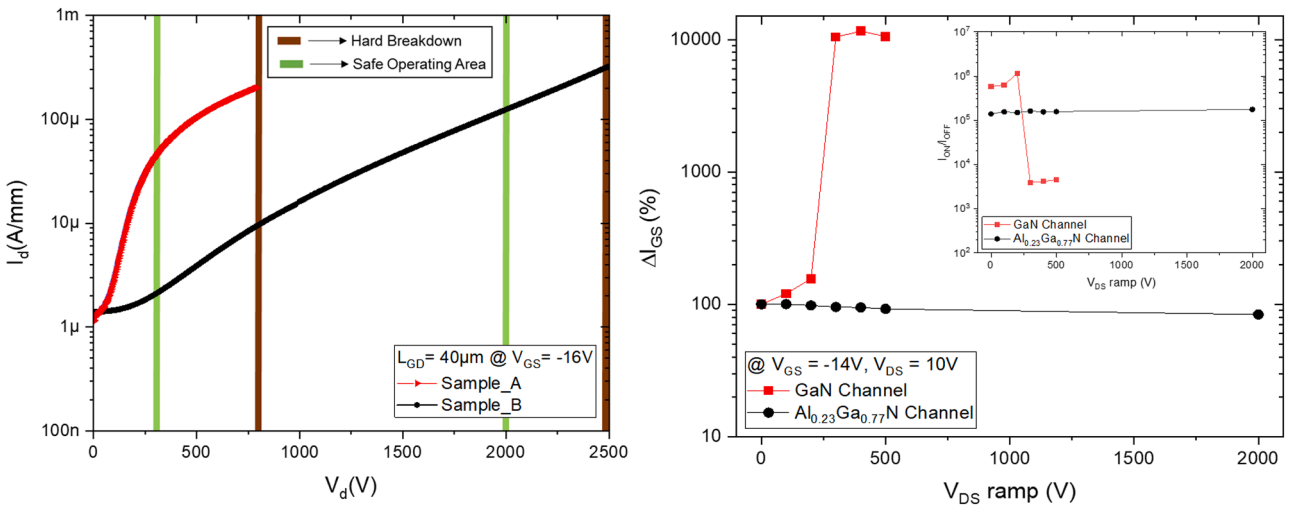

Fig. 6. (a.) Transistor voltage derating defined on drain leakage current against applied V_{DS} (b.) Maximum change in gate leakage current density (inset - I_{ON}/I_{OFF} ratio) for GaN and $Al_{0.23}Ga_{0.77}N$ channel HFETs for various V_{DS} ramp iterations.

Considering the robustness test, a transistor voltage derating can be derived based on defining the safe operating off-state blocking voltage from hard breakdown voltage. The hard breakdown voltage for measured GaN and $Al_{0.23}Ga_{0.77}N$ channel HFETs were 780 V and 2500 V respectively. As shown in Fig. 6a, the safe operating off-state voltage for the GaN and $Al_{0.23}Ga_{0.77}N$ channel HFETs is defined at the voltage after which the devices show degradation in off-state leakage current as shown by the green lines. It can be observed that a 65% voltage derating in thin GaN channel transistors is required for safe off-state operation. On the other hand, $Al_{0.23}Ga_{0.77}N$ channel transistors show only 20% voltage derating from hard breakdown voltage despite the lack of maturity, which is even lower than the 30% voltage derating as seen in state-of-the-art commercial GaN HEMTs and FETs [23,24]. The maximum change in gate leakage current during robustness tests is shown in Fig. 6b for multiple V_{DS} ramp voltages normalized at 100% considering fresh devices. The $Al_{0.23}Ga_{0.77}N$ channel HFETs shows maximum change in gate leakage < 200nA/mm up to 2000V demonstrating the stability of gate leakage current thus giving a highly stable I_{ON}/I_{OFF} ratio (see inset of Fig. 6b). On the other hand, GaN channel HFETs delivers significant leakage fluctuations from fresh device after every V_{DS} sweeps due to the generation of permanent leakage path.

5. Conclusion

AlGaN channel and GaN channel HFET heterostructures were grown on bulk AlN substrates. HRXRD and AFM scans revealed the better crystal quality and low surface roughness of $Al_{0.23}Ga_{0.77}N$ channel HFETs as compared to GaN channel HFETs owing to the lower lattice mismatch with AlN substrate. $Al_{0.23}Ga_{0.77}N$ channel devices showed I_D up to 320 mA/mm with specific R_{on} as low as 4 mΩ.cm^2 in the linear regime despite drain/source ohmic contacts that can still be optimized. The lateral breakdown measurements revealed high quality of AlN bulk with critical breakdown field reaching 10 MV/cm for low contact spacing. The transistor breakdown voltages scales with gate –drain spacing for both devices. $Al_{0.23}Ga_{0.77}N$ channel devices reached hard breakdown value up to 2500V against 780V for GaN channel HFETs. The Baliga power figure of merit for the fabricated $Al_{0.23}Ga_{0.77}N$ and GaN channel HFETs is around 120 MW/cm^2 and 32 MW/cm^2, respectively. Interestingly, $Al_{0.23}Ga_{0.77}N$ channel HFET delivered robust performance up to 2000V compared to GaN channel HFET showing permanent degradation after ramping up to 300V. The robustness tests also confirm the reliability of $Al_{0.23}Ga_{0.77}N$ channel HFET with only 20% voltage derating against more than 50% in the case of GaN channel HFETs. This work confirms the interest of employing an AlGaN channel in terms of high voltage robustness enabling safe operating off-state voltages much closer to the hard breakdown than that GaN HEMTs.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

Data will be made available on request.

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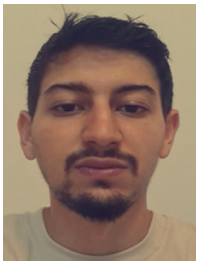
Jash MEHTA is a Ph.D. scholar within the WIND research group working on innovative wide bandgap devices at IEMN, CNRS France. He received his Bachelors in Electrical and Electronics Engineering in 2018 from Parul University, India. In 2019, he received his Master's in electronics, electrical energy, and automatics from INSA-CVL, France. He pursued a research internship at the R&D department of STMicroelectronics in 2019, where he worked on optimization of BST thin film varactors. He is pursuing his Ph.D. in fabrication and characterization of HFETs based on ultra-wide bandgap materials for high voltage power electronics. His research interests include nano-fabrication, electrical characterization, and T-CAD simulation study of FETs.



Idriss ABID is a CNRS scientist within the WIND team focused on wide bandgap material and devices at IEMN in France. He received his Ph.D. in Electrical engineering from the University of Lille in 2021. Then, he started his post Doc in the same team. Multiple achievements and some state-of-the-art results have been realized in the field of high power electronics. His research interests are the fabrication and characterization of innovative wide bandgap devices.

Yvon Cordier received the Ph.D. degree from the Lille University of Science and Technology in 1992 and he joined the Central Research Laboratory of Thomson-CSF, Orsay, France, where he developed III–V epitaxial structures for electronic and optoelectronic devices. In 1996, he joined the Institute of Electronics, Microelectronics, and Nanotechnology (IEMN) as a permanent researcher of the Centre National de la Recherche Scientifique (CNRS), and studied the growth of AlInAs/GaInAs metamorphic heterostructures on GaAs substrate. In 2001, he joined the Centre de Recherche sur l'Hetero-Epitaxie et ses Applications (CRHEA), Valbonne, France. He has authored or coauthored more than 200 publications, holds 5 patents, and is heading as Research Director a group developping the growth of semiconductor materials, including GaN, SiC, 2D materials and ZnO for electronics.

Farid Medjdoub is a CNRS senior scientist and leads a research team WIND focused on wide bandgap material and devices at IEMN in France. He received his Ph.D. in Electrical engineering from the University of Lille in 2004. Then, he moved to the University of Ulm in Germany as a research associate before joining IMEC as a senior scientist in 2008. Multiple state-of-the-art results have been realized in the frame of his work. Among others, world record thermal stability up to 1000°C for a field effect transistor, best combination of cut-off frequency / breakdown voltage or highest lateral GaN-on-silicon breakdown voltage using a local substrate removal have been achieved.