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High-Speed Digital Electronics Board on a Novel Biobased and Biodegradable Substrate

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Abstract— This paper describes a comparative study between traditional and sustainable approaches on a high-speed digital electronics design, demonstrating a solution similar to modern embedded systems. The system was produced on traditional flame retardant 4 (FR4) substrate and on bio-sourced and biodegradable, sustainable printed circuit board (PCB) substrate based on polylactic acid (PLA) and flax fibers, to evaluate the maturity of ecological substrates. The substrate was first characterized from a radio-frequency point of view, using resonant cylindrical cavities and a resonant microstrip line. Then, the circuit design was constrained by the measured relative permittivity and loss tangent, in order to guarantee a good matching of the differential lines and to reach a low signal distortion. Similarly, the physicochemical properties of the substrate induced the choice of processes for etching and soldering the components. The matched transmission lines were simulated with ADS software using input/output buffer information (IBIS) models of the digital circuits. Their characterization was conducted with eye diagram and time domain reflectometry technics. As an introduction, a life-cycle analysis (LCA) was conducted to evaluate the ecological impact part of the FR4 PCB among this electronic board life cycle impact.

Keywords— Printed circuits, PCB, Biodegradable materials, Ecodesign, Dielectric substrate, Signal integrity.

I. INTRODUCTION

The development of sustainable electronic devices and assemblies has become a major challenge in reducing greenhouse gas emissions, scarcity of non-renewable mining, and limiting the volume of waste from electrical and electronic equipment (WEEE).

New biosourced and biodegradable substrates have appeared during the last years [1], [2], [3], providing alternatives for the traditional flame retardant 4 (FR4) materials. For high-frequency applications, these organic substrates generally have the flaw of having high electromagnetic losses due to their absorption of ambient humidity [4]. Because their dielectric properties significantly differ from FR4 substrate ones, the design of high-speed digital circuits requires geometry adaptation when laying out permittivity-dependent structures like low voltage differential lines (LVDS) or matched microstrip lines.

As an introduction, the first part of this paper is a life cycle analysis of the electronic board presented here. Part two details the radiofrequency (RF) characterization results of a new bio-sourced dielectric substrate supplied by Meshlin (HUN), in which the primary constituent is a polylactic acid (PLA) / flax composite [5]. Both constituents are 100%

biosourced and biodegradable. Compared to FR4, this substrate has relatively low glass transition and fusion temperatures [6]. A third part, therefore, shows how the printed circuit board (PCB) design was adapted to tune the matched lines impedance and how the subtractive PCB technology and soldering processes were tailored. Signal integrity is characterized in a fourth part.

II. LIFE CYCLE ANALYSIS (PRODUCTION & END-OF-LIFE)

To estimate the part of the ecological impacts of the FR4 PCB among the electronic components, a partial LCA was conducted with the "Bilan Produit" tool from the French Agence de la Transition Ecologique (ADEME). The aim is to evaluate the PCB part of the impacts in comparison to the rest of the board's materials; therefore, choice was made to limit the study to the production phase and end of life of the product. The "product" is limited to the high-speed digital electronic board detailed further in the paper. Because of the testing and measurement functionalities of the board, one may argue that the electronic parts filling ratio of the PCB is not representative of a commercial product (mainly because of the room occupied by artificially lengthened matched lines). This is why, for computing the LCA, the PCB area was divided by two; comparing PCB impacts against electronic parts impacts can thus be considered realistic.

Fig.1 summarizes the significant impacts of the electronic board materials dispatched in 5 categories. The vertical scale unit is one day impact of an average European citizen. The blue on the diagram is the PCB impact part of the electronic

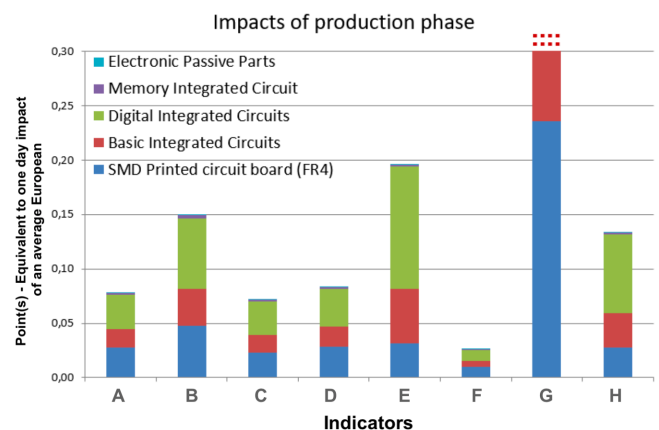


Fig. 1. Production and end-of-life results of the LCA. A.) Energy Consumption; B.) Resources Consumption; C.) Greenhouse gases GWP 100 mod; D.) Acidification; E.) Eutrophication (air water soil); F.) Photochemical pollution; G.) Aquatic ecotoxicity; H.) Human toxicity;

board. Please note that the total value for the aquatic ecotoxicity indicator is off-scale and is almost 1.8 point.

Depending on indicators, FR4 PCB impact varies between 20% to 40% of the total impact. This life cycle analysis concludes that FR4 PCB is a major contributor to the ecological impact of a digital electronics board. Therefore, studying alternative materials with biodegradable and possibly biosourced characteristics is a key path to more sustainable electronics.

III. PLA/FLAX SUBSTRATE CHARACTERIZATION

The studied substrate comes with 35 μm standard thickness laminated copper on both sides of the 1.6 mm thickness prepregs, including a flame retardant, to match traditional requirements (Fig. 2).



Fig. 2. PLA/Flax laminated substrate [5].

The RF characterization was conducted on two batches, with differences in the manufacturing of the product. For the first batch, cylindrical resonant cavities were used (930 MHz and 2480 MHz) on samples from which copper layers were removed (Fig. 3). The second batch was characterized by using a resonant transmission line. Extracted relative permittivity and loss tangent are detailed in Table I.

TABLE I. PLA/FLAX RF CHARACTERIZATION RESULTS

# Batch	Frequency (MHz)	ϵ_r	Loss tan
1	930	2,49 \pm 0,17	0,05 \pm 0,01
1	2480	2,31 \pm 0,16	0,04 \pm 0,01
2	1200-9470	2,18 \pm 0,16	NC

The visual aspect of the material from batch #2 shows that the surface condition was optimized to get a lower roughness. Our measurements across almost one decade of frequencies demonstrate that the material has a very low dispersion; it guaranties that all the spectrum frequencies of a digital signal propagating on the line will see the same characteristic impedance, therefore ensuring a low signal distortion around its edges.

Both batches show a significantly lower relative permittivity than the FR4 substrate, implying a redesign of the matched lines. This low value can probably be justified using a three components model of the substrate: air, flax, and PLA [7]. Meanwhile, the measured loss tangent is not far from the

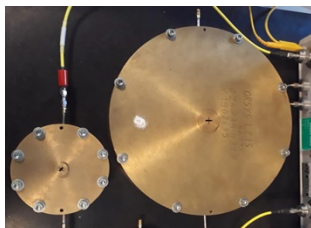


Fig. 3. 2400 MHz (left) and 930 MHz (right) resonant cavities used for characterization.

FR4 one (between 0.02 and 0.03, depending on batches) and should not be much of a problem for the propagation of fast signals.

These results are exploited for the circuit design carried out with ADS and KiCAD software, described in the next section. Because of substrate sample availability, the circuit was realized on a sample from batch #1.

IV. DESIGN AND FABRICATION OF THE CIRCUIT

The block diagram of the circuit is displayed in Fig. 4. It describes a typical electronics architecture of a fast digital electronics circuit, in this case, built around a programmable logic device (FPGA). The FPGA controls a MOS driver integrated circuit with a 1 MHz pulse width modulation (PWM) signal and transfers digital signals through two low voltage differential signal (LVDS) lines. These must allow a minimum throughput of 250 Mbits/s, the value of standards such as gigabit Ethernet 1000BASE-T1. Similarly to standard SD card interfaces, a quad serial peripheral interface (QSPI) was implemented with a typical double data rate (DDR) throughput of 4x160Mbits/s. The FPGA and its peripherals require several power supply levels, which adds complexity to this board, bringing it closer to commercial consumer electronics boards.

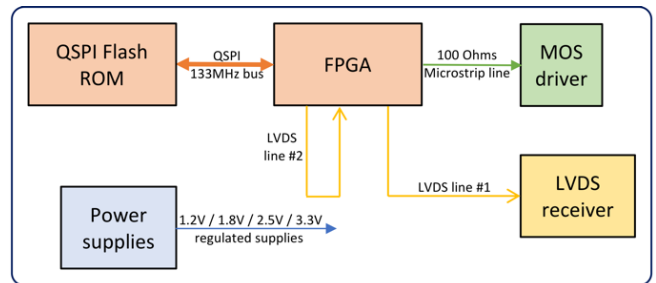


Fig. 4. Fast digital electronics test board (block diagram).

The aim of this experiment is to check that design adaptations for the new biosourced substrate are efficient and lead to similar performance. The PCB layout was realized for the FR4 substrate, and for the PLA/flax one, taking into account the dielectric properties of each substrate. The not well-known mechanical properties of the latter led to limiting the number of vias (24 vias, most of them are a connection to the bottom layer ground plane to keep the ground net impedance as low as possible), and to prefer surface mount connectors to through hole kinds. Choice was made to limit the smaller structures to 150 μm (insulation between tracks, tracks widths) to keep the test PCB design rules around the average of consumer electronics PCBs.

The design of the matched lines was carried out following the state of the art of the layout, by using ADS software to dimension and simulate them:

- The microstrip line carries a PWM signal, with a potential spectral width larger than 250 MHz. Because of the line length (54 mm), it should be matched to the line termination. A standard 100 Ω impedance was chosen. The FPGA's 3.3 V output driving this line must be of lower impedance, low enough to reach transistor to transistor logic (TTL) levels at the input of the target integrated circuit (IC) placed at the end of line.

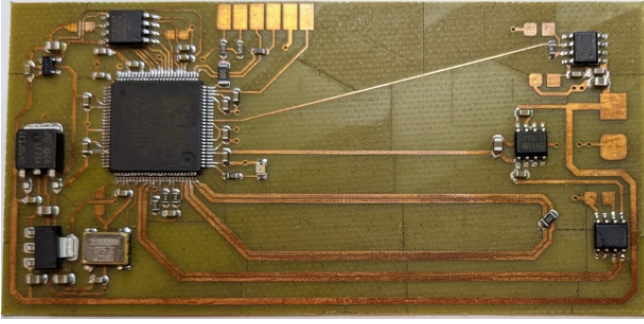


Fig. 5. Assembled FR4 test board (without connectors).

- LVDS lines #1 and #2 are of respective length 85 mm and 124 mm. Their impedance is set to 100Ω , in the range of LVDS electrical standard.

In Fig. 5 and Fig. 6, one can notice that in the end, layout differences are only about matched lines. Please note that

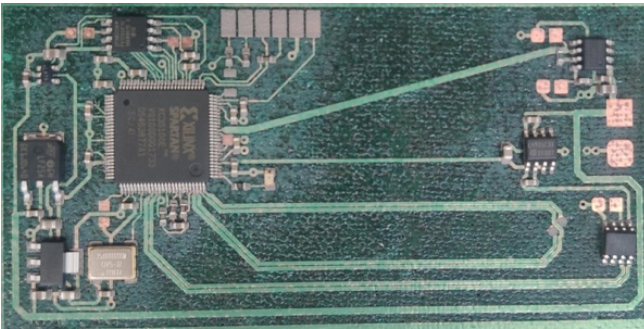


Fig. 6. Assembled PLA/flax test board (without connectors).

solder mask was used to assemble the PLA/flax board, hence the green color visible in Fig. 6. TABLE II. sums up the physical characteristics of substrates and matched lines.

TABLE II. MATCHED LINES CHARACTERISTICS

Caractéristique	FR4	PLA-lin
Substrate (μm)	800	1630
Relative permittivity	4,3	2,4
100 Ω Microstrip line width (μm)	250	1000
LVDS lines width (μm)	600	600
Isolation between lines - LVDS (μm)	150	150
Differential impedance - LVDS (Ω)	100	119

Because of the $150 \mu\text{m}$ minimum structure limit, reaching the LVDS 100Ω target impedance for the PLA/flax PCB was impossible. This is the consequence of an almost twice lower permittivity than FR4, and a twice thicker substrate. On commercial PCBs, LVDS lines are usually laid out on the top or bottom layer of PCBs with four or more layers. A typical $1.55 \text{ mm} / 4$ layers PCB will use a standard stackup with only $370 \mu\text{m}$ of dielectric between the external and first inner layer [8], leading to much narrower LVDS tracks than on our 1.6 mm PLA/flax or 0.8 mm FR4 substrates.

¹ A thorough LCA should be conducted for different technologies of end-of-life copper retrieving to determine whether it is more interesting to remove useless copper during the etching step or at PCB end-of-life recycling.

Both circuits were etched with an LPKF Protolaser ST engraver. Because of the lower fusion temperature of the PLA, the laser beam command parameters were accurately tuned to avoid local melting of the substrate. The LPKF delamination of copper strips technology enables immediate copper retrieving¹ but leaves stuck strips if not correctly set. A few strip residues had to be removed manually. Still, in the end, the adjustment of the processing parameters led to an etching almost as effective as the one obtained on the FR4 reference design.

Because of the low glass transition temperature of the PLA (around $60\text{-}80 \text{ }^\circ\text{C}$), components soldering was carried out by using a vapor phase soldering oven, at the temperature of $170 \text{ }^\circ\text{C}$, with a reflow profile adapted for this material (Fig. 7). Around $160 \text{ }^\circ\text{C}$ peak temperature in vapor phase was obtained by using HT170 Galden. The solder paste used to assemble the PCB is a low melting temperature ($138 \text{ }^\circ\text{C}$) alloy: Sn42/Bi57.6/Ag0.4 from ChipQuik. Solder mask was applied to limit substrate wettability and enhance the quality of the soldering process (roughness of substrate tends to ease adherence of solder paste residues).

This alloy was also functional for manual soldering (connectors assembly), with an iron set to less than $200 \text{ }^\circ\text{C}$, with no visual damage to the substrate.

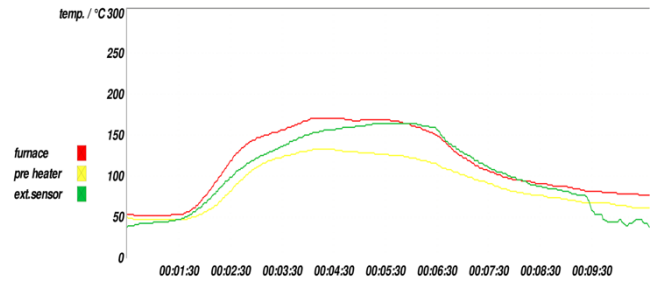


Fig. 7. Vapor phase soldering reflow profile with BiSnAg solder paste.

V. MATCHED LINES CHARACTERIZATION

First, the signal integrity of the matched lines was tested with eye diagrams validation. Then, lines were characterized with the temporal domain reflectometry technique (TDR). Test signals were generated with the FPGA. This allows us to get measurements directly on the application board, on the actual tracks, but does not have the full performance of laboratory TDR equipment. Signals were acquired with a TDS6604B oscilloscope ($6\text{GHz} - 20\text{GS/s}$) and a P7350 high-impedance differential probe (5GHz , $\text{Tr} < 100 \text{ ps}$). The FPGA's output rising time was equal to $200 \text{ ps} \pm 20$. This is 20 times slower than a good TDR analyzer but is acceptable for our sub-GHz signals.

The characteristics of the test signals are:

- For the eye diagram, the signal is a 2048 bits length pseudo-random binary sequence (PRBS) with a minimum symbol duration of 4ns (250 MHz). It is acquired for a duration of 160,000 oscilloscope samples.
- The TDR analysis is conducted from a 4 ns pulse, long enough for the considered line lengths.

Eye diagrams tests are reported on Fig. 8 and Fig. 9. The eye diagram drawn at the end of the microstrip line displays a comfortable height for a TTL-compliant signal, with crossings showing a low jitter.

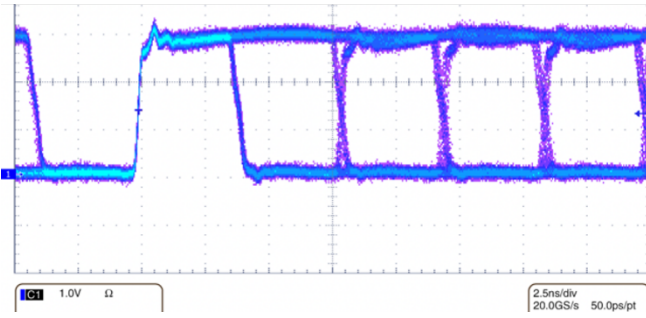


Fig. 8. PLA/flax substrate: eye diagram at the end of the microstrip line.

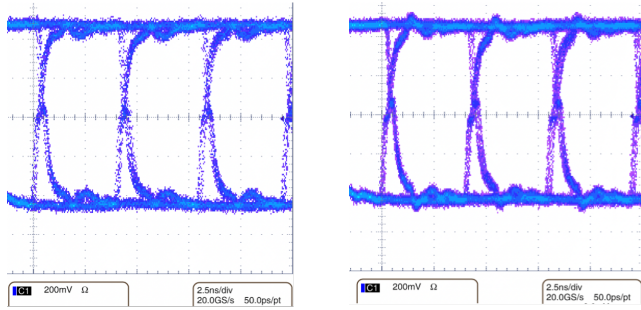


Fig. 9. Respectively FR4 and PLA/flax eye diagrams (LVDS #2 line).

We detail the results of the LVDS #2 line, which is easier to characterize because of its longer length. This line loops from an output to an input of the FPGA. In Fig. 9, the eye diagrams at the input of the FPGA demonstrate comparable performance for both designs. Signal amplitude meets the LVDS standard.

Regarding the TDR analysis of the microstrip line, a transient response simulation was conducted with ADS software. The FPGA output is simulated thanks to its input/output buffer information specification (IBIS) provided by the manufacturer. The end of the microstrip line consists of the termination resistance ($100\ \Omega$) parallel to the MOS driver IC high impedance input, modeled by its capacitance input ($6\ \text{pF}$ typical value). Fig. 10 shows the simulation results for the standard values ($54\ \text{mm}$ line length, $6\ \text{pF}$, $100\ \Omega$ characteristic impedance). By sweeping parameters, additional simulations showed that the oscillating behavior at the output of the FPGA is related to the non-matching between the latter and the microstrip and also to the input capacitor at the end of the line. This is the drawback of driving the line with a low impedance output, which is mandatory to keep

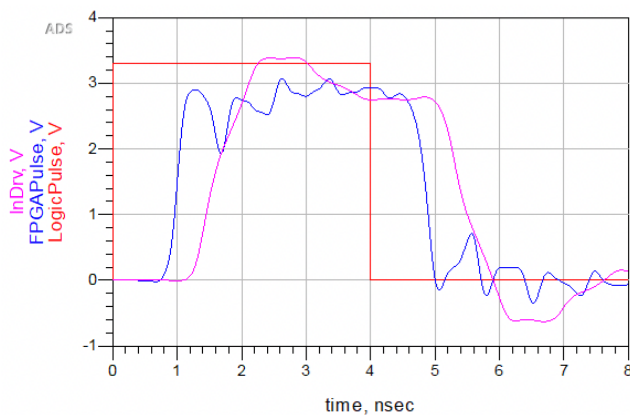


Fig. 10. TDR signal simulation at microstrip line's input (FPGAPulse) and at end of the line (InDrv). LogicPulse is the input of the FPGA's pin buffer.

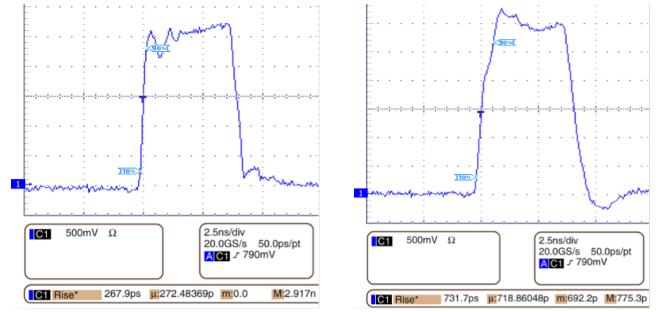


Fig. 11. TDR signal at the microstrip line input and output.

TTL-compatible levels at the end of the line. In Fig. 11, one can see that the TTL 2V trigger level is reached within a short rise time, with a small oscillation, in compliance with the simulations.

The differential pairs were not simulated because of a lack of IBIS model from Xilinx manufacturer. The analysis of the LVDS #2 TDR signal shows that the differential impedance gap between the two PCBs ($100\ \Omega$ versus $119\ \Omega$) has a limited impact (Fig. 12). In fact, the TDR signal is better with the PLA/flax PCB line. This is explained by the Xilinx datasheet: the LVDS inputs of the FPGA are designed in the upper limit of the LVDS norm, with a $120\ \Omega$ line termination impedance, hence better matching with the PLA/flax line also set at the upper limit.

VI. DISCUSSION

The PLA/Flax substrate used for this design does not comply with the current standard of the Association Connecting Electronics Industries (IPC), usually matched by FR4 substrates. Some of its mechanical characteristics were already enhanced by the manufacturer with its second generation (peel strength, evenness). Others may not reach the norm (glass transition temperature), but slight adaptations of the etching process and electronic parts assembly (process, temperature, soldering alloy) will certainly help circumvent these norm deviations.

From the radiofrequency field, it has been shown that this substrate is suitable with good performance for high-frequency applications, like antenna manufacturing [10].

A critical point for the future is controlling the substrate biodegradability during its active life. The characteristics of cellulosic substrates and even FR4 ones significantly fluctuate with humidity [4], [9], with consequences for signal integrity. The same kind of studies should be carried out for this PLA/flax substrate, and a coating with low environmental impact (and its associated removal process) could help solve this issue.

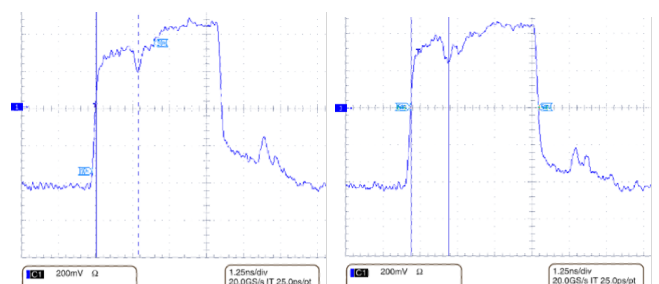


Fig. 12. LVDS #2 TDR signal at the line input, FR4 PCB, and PLA/flax.

Lastly, it is important to note that flax fibers and PLA are low-cost materials from the aspect of production, making the substrate economically competitive with FR4.

VII. CONCLUSION

Among the WEEE, current PCBs made from FR4 substrate share a significant part of the ecological impact of a typical electronic product. The LCA we conducted on our test board confirmed this impact part. Biosourced and/or biodegradable materials are more and more used in electronic products. At very high frequencies, stakes are high because of the major influence of the substrate's physical properties on signal propagation.

Our work showed how a high-speed digital circuit design could be adapted to a new PLA/flax substrate, and then we compared the performance in terms of signal integrity. We also showed how fabrication processes of the PCB circuit and parts soldering could be slightly adapted to manufacture an electronic board with comparable characteristics. Although the product still requires enhancements to comply with more items of the IPC standard, our functional tests and signal integrity characterization demonstrated the credibility of this PCB technology as an alternative to traditional FR4 substrates.

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