



HAL
open science

Jitter Noise Impact on Analog Spiking Neural Networks: STDP Limitations

Zalfa Jouni, Théo Prats Rioufol, Siqi Wang, A. Benlarbi-Delai, Pietro M. Ferreira

► **To cite this version:**

Zalfa Jouni, Théo Prats Rioufol, Siqi Wang, A. Benlarbi-Delai, Pietro M. Ferreira. Jitter Noise Impact on Analog Spiking Neural Networks: STDP Limitations. 36th SBC/SBMicro/IEEE/ACM Symposium on Integrated Circuits and Systems Design (SBCCI), Aug 2023, Rio de Janeiro, Brazil. 10.1109/sbcci60457.2023.10261661 . hal-04193888

HAL Id: hal-04193888

<https://hal.science/hal-04193888v1>

Submitted on 30 Nov 2023

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

AUTHOR VERSION

Jitter Noise Impact on Analog Spiking Neural Networks: STDP Limitations

Zalfa Jouni, Theo P. Rioufol, Siqi Wang, Aziz Benlarbi-Delai, Pietro M. Ferreira

Université Paris-Saclay, CentraleSupélec, CNRS, Lab. de Génie Électrique et Électronique de Paris, 91192, Gif-sur-Yvette, France.

Sorbonne Université, CNRS, Lab. de Génie Électrique et Électronique de Paris, 75252, Paris, France.

Email: zalfa@ieee.org , maris@ieee.org

Abstract—Accurate spike timing of neurons is essential for the temporal learning rules in Spiking Neural Networks (SNNs), such as the spike-timing dependent plasticity (STDP). Implementing these rules in analog SNNs presents a challenge as it would require a reliable spike timing of analog neurons. This paper investigates the impact of jitter noise on the spike timing of various analog neuron models, and highlights trade-offs in training neurons using spike timing. Post-layout simulation results reveal that noise-induced period jitter significantly affects spike occurrence time. Its values are three orders of magnitude higher than the precise spike timing required for an accurate synaptic weight updates. Moreover, the spike timing becomes a random variable with a σ/μ that exceeds 76%. This study shows that the spiking frequency is a more reliable measure of neuronal activity, as it achieves a σ/μ of only 0.2%.

Index Terms—Analog Neurons, STDP, Noise, Spiking Neural Networks, Temporal Learning Rule

I. INTRODUCTION

Artificial Neural Networks (ANNs) are computational models designed to emulate the functions of the neocortex in the human brain. As the second generation of ANNs, deep neural networks (DNNs) are rapidly evolving and widely used in many fields. Despite their tremendous potential, training and inference for DNNs require complex and power-hungry computational algorithms. Thus, their deployments are difficult in low-power devices [1]. Spiking Neural Networks (SNNs), also referred to as the third generation of ANNs, effectively bridge the gap between ANNs and biological neural networks [2]. In an SNN, the energy efficiency is improved through spike coding, where the power is only consumed by the generation or the propagation of spikes.

Many hardware implementations of SNNs have been reported in the literature [3], [4]. Figure 1 depicts the structure of the hardware-based SNN, where an electronic spiking neuron (eNeuron; eN1) is connected to other eNeurons (eN2, eN3, and eN4) through electronic synapses (eSyn1, eSyn2, and eSyn3). Synapse plays a crucial role in the transmission of information between two eNeurons. It converts spikes of the pre-synaptic eNeuron into current (I_{syn}) that will be received by a post-synaptic eNeuron. This current is updated by the synaptic weight (w_{syn}), which determines the strength of the connection between two eNeurons.

One of the main challenges to implement SNNs in analog hardware is to develop efficient and accurate learning tech-

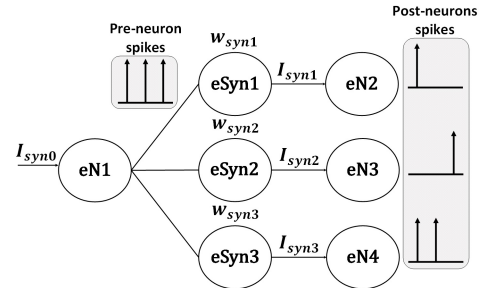


Fig. 1. Structure of a hardware SNN composed of an eNeuron connected to three other eNeurons through synapses. The behavior of spikes is illustrated.

niques [1]. Many researches focused on the backpropagation algorithm to update the synaptic weights. However, it requires complex hardware resources to be fully implemented in analog circuits. One of the biologically plausible learning rule is based on the occurrence time of spikes [5]. Among this category, the spike-timing-dependent plasticity (STDP) is a well-known rule that adjusts the strength of a synapse based on the relative time of pre-synaptic and post-synaptic spikes [6]. Previous studies have demonstrated that STDP is a powerful learning rule for SNNs, as it can be used for on-chip unsupervised learning [7]. However, imprecise spike timing in analog eNeurons may disrupt unsupervised learning when jitter noise occurs. Abidi has proved that jitter noise can introduce variations in signal timing [8]. Thus, it can change the time of the spike occurrence in a spiking eNeuron. To the best of the authors' knowledge, this challenge has not been addressed in the literature, and it can affect the accuracy of analog SNN using time-dependent learning rules.

This paper aims to study the impact of transistor noise on spike timing of different analog spiking eNeurons. Additionally, its order of magnitude is estimated to evaluate if the temporal learning rules can be used in analog SNNs. Previously published eNeurons from [3], [9]–[11] using BiCMOS 55 nm technology and a temporal learning rule as STDP are described in Sec.II. Section III proposes the noise analytical tools. Post-layout simulation (PLS) results are explored in Sec.IV to show the impact of noise on the time and the frequency of spikes for the different eNeurons. Finally, conclusions are drawn in Sec.V.

II. SPIKING NEURAL NETWORKS

Sec. II-A describes the analog eNeurons that are designed in literature and used to study the noise impact in this paper. Sec. II-B presents the STDP learning rule and its implementation for analog SNNs.

A. Analog Spiking eNeurons

Spiking eNeuron models vary in their level of biological inspiration, which affects their complexity and efficiency in hardware. The dynamics behavior of analog spiking eNeurons can be described using generic differential equations represented as [12]

$$\frac{dV_m}{dt} = f(V_m) - g(U_m) + I_{syn} \quad (1)$$

$$\frac{dU_m}{dt} = a(bV_m - h(U_m)) \quad (2)$$

where V_m is the spiking membrane potential and U_m is the membrane recovery variable. $f(V_m)$, $g(U_m)$, and $h(U_m)$ are non-linear functions that depend on the eNeuron model [1]. Due to the I_{syn} integrated into the membrane capacitance C_m , V_m reaches a certain threshold. At this point, the functions are updated, and the eNeuron starts the spiking activity.

Spiking eNeurons are often compared in the state-of-the-art by their energy efficiency (E_{eff} , which is the energy consumption per event), their spiking frequency (f_{spike}), and their silicon area. In this paper, four eNeurons are considered where two eNeurons are based on the Morris-Lecar (ML) model and two others are based on the leaky-integrate-and-fire (LIF) model. ML model is known as a biologically-plausible model, while the LIF model is known as a less complex category.

A biomimetic ML eNeuron (*eNeuron1*) has been designed in [3]. It consists of two charged and discharged capacitors through two transistors. The spike generation is controlled by three inverters, resulting in a total of 8 transistors and 2 capacitors. *eNeuron1* achieves an E_{eff} of 1.95 fJ/spike and a high f_{spike} of 400 kHz. Recently, Takaloo *et al.* have proposed a simplified ML eNeuron (*eNeuron2*) [9]. Its design only includes three inverters (6 transistors), which operate in conjunction through multiple feedback loops. *eNeuron2* achieves an E_{eff} of 1.15 fJ/spike.

Danneville *et al.* have proposed an ultra-low power LIF eNeuron (*eNeuron3*) [10]. It consists of 5 transistors (including two inverters) and a feedback capacitor. This eNeuron achieves an E_{eff} of 2 fJ/spike but with a low f_{spike} of 15 kHz. Besrou *et al.* have designed a LIF eNeuron (*eNeuron4*) [11]. This eNeuron consists of 6 transistors and two capacitors. It achieves a high f_{spike} of 343 kHz in the same silicon surface as [3], and an energy consumption per spike of 1.2 fJ/spike.

B. STDP Learning

STDP learning is one of the learning rule that depends on the spike timing of eNeurons. In this learning method, the synaptic weight exponentially changes according to the arrival time difference between the pre-synaptic eNeuron and the

post-synaptic eNeuron ($\Delta T_s = t_{post} - t_{pre}$). The weight change function, i.e., Δw_{syn} , can be expressed as follow [7]

$$\Delta w_{syn}(\Delta T_s) = \begin{cases} w_+ e^{\frac{\Delta T_s}{\tau_+}} (\Delta T_s > 0), \\ -w_- e^{-\frac{\Delta T_s}{\tau_-}} (\Delta T_s < 0). \end{cases} \quad (3)$$

where w_+ and w_- are the maximum and minimum values of Δw_{syn} , and τ_+ and τ_- are the time windows that determine the weight update rate for long-term potentiation and long-term depression, respectively. As shown in Fig. 2, if the presynaptic spike arrives before the postsynaptic spike ($\Delta T_s > 0$) the synaptic weight increases, otherwise ($\Delta T_s < 0$) it decreases.

Some works have proved an accurate implementation of SNN using the STDP learning [13]. However, very low firing rate (~ 100 Hz) eNeurons with high power consumption ($\sim 2 \mu\text{W}$) are depicted. In SNNs using analog eNeurons with high f_{spike} , STDP learning curve can be illustrated in Fig. 2 [5], [6], [14]. There, a positive ΔT_s less than $1 \mu\text{s}$ leads to a substantial increase in Δw_{syn} , while a negative ΔT_s higher than $-1 \mu\text{s}$ leads to a strong decrease in Δw_{syn} .

A small neural network is implemented in a 28 nm CMOS technology to perform cognitive functions in [6]. It consists of three LIF eNeurons and two synapses. The proposed synapse supports the STDP rule in an energy and area efficient manner. Another SNN designed in a 180 nm CMOS technology is proposed in [14]. It uses the STDP learning to perform heart rate classification. It comprises 21 LIF eNeurons and 90 synapses. In [4], a medium scaled SNN is proposed in 65 nm CMOS technology to achieve oriented edge classification. It consists of 40 LIF eNeurons and 108 ultra-low power synapses, where weights are updated using STDP rule. None of these implementations have demonstrated the SNN robustness over transistor noise when using the STDP learning.

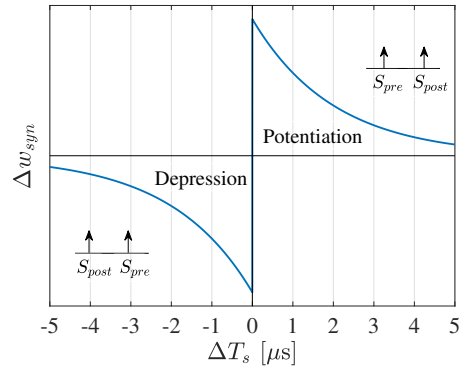


Fig. 2. Curve shape of the synaptic weight update Δw_{syn} in STDP rule and the appropriate mechanism. S_{pre} and S_{post} are the pre and post synaptic spikes, respectively.

III. NOISE ANALYTICAL TOOLS

A noise analytical tool is proposed to investigate the impact of transistor noise on ΔT_s , which is the main factor for the synaptic weight update on STDP seen in (3). As ΔT_s is a

relation based on the spike timing of eNeurons, four spiking eNeurons are implemented from the literature (*eNeurons* 1-4). Thus, variations in the spike timing in these eNeurons caused by the noise are studied.

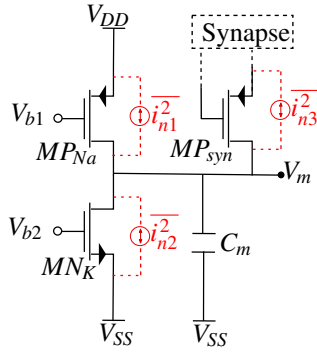


Fig. 3. Noise model of an eNeuron membrane node connected to one synapse

A. eNeuron model

Figure 3 illustrates a noise model for the typical eNeuron membrane node in the state-of-the-art. The eNeuron membrane node is composed mainly of two transistors MP_{Na} and MN_K with a membrane capacitance C_m . These two transistors mimic the activity of ions that enter or leave the neuron membrane. These electronic charge pumps are controlled by positive and negative feedback loops to form a series of inverters for the K (Potassium) and the Na (Sodium) ions. To simplify the circuit, these feedback loops are not represented, and substituted by V_{b1} and V_{b2} supposed to be the voltages coming from both feedback loops.

Whenever the eNeuron receives a synaptic current I_{syn} from the transistor MP_{syn} of an electronic synapse, C_m is charged through MP_{syn} and MP_{Na} (pull-up) and discharged through MN_k (pull-down). These phenomena cause a large but brief change in the membrane potential V_m , and the eNeuron spikes. This eNeuron noise model covers the four implemented eNeurons (*eNeurons* 1-4). As the *eNeuron2* circuit is made of transistors only, C_m is considered as the total parasitic capacitances generated at the eNeuron membrane level.

To implement the non-linear functions (1)-(2) and to reduce power consumption, eNeurons transistors are biased on deep-subthreshold. As a low current I_{syn} enters an eNeuron, it flows through these transistors, causing carrier diffusion to dominate the channel current. This results in a significant variability in the ionic current that flows across V_m . Under weak inversion, the shot noise causes variations in the arrival time of individual electrons and holes on V_m , which can change the spike generation time. Shot noise is dominant over other noises, such as thermal noise, in this operation region [15].

B. Time Deviation due to Noise

To study the impact of the noise, ΔT_n is defined as the deviation of the spike timing of the eNeuron, when noise is considered, from its original position. As illustrated in Fig. 4, the introduction of noise can cause the spike occurrence of

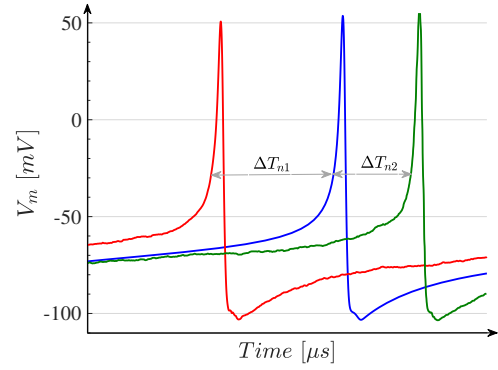


Fig. 4. A spike produced by V_m in a noise-free transient simulation (blue plot) and two trans-noise simulation points (red and green plots).

the eNeuron to shift to the left ($\Delta T_{n1} < 0$) or right ($\Delta T_{n2} > 0$) relative to the spike occurrence without noise (plotted in blue). This produces a random variable ΔT_n .

C. Jitter and Phase Noise

As the studied noise affects the time of the spike occurrence, the period jitter σ_J is defined as the standard deviation of ΔT_n in the spike timing [8]. It is a crucial characteristic as it can affect the stability of the eNeuron response, particularly during the training of analog SNNs [16].

As shown in Fig. 3, period jitter comes from three current noise sources that form two main noise events. One comes from the pull-up branch, where the synapse current of the PMOS transistor MP_{syn} and the drain current of the PMOS transistor MP_{Na} raise V_m as charges enter in C_m . The other one comes from the pull-down branch, where the drain current of the NMOS transistor MN_K decreases V_m as charges leave C_m . Therefore, these two noise events are assumed to be uncorrelated, resulting in two propagation delays jittered by noise. Thus, the variance of period jitter is given by [8]

$$\sigma_J^2 = \sigma_{t_{dN}}^2 + \sigma_{t_{dP}}^2 \quad (4)$$

where $\sigma_{t_{dN}}^2$ and $\sigma_{t_{dP}}^2$ are the jitter noise sources from the two propagation delays of the pull-up and pull-down branches, respectively.

Before the discharge phase begins, PMOS pull-up transistors deposit an initial noise in the capacitance C_m . The mean square voltage noise and the associated jitter are

$$\overline{V_n^2} = \int S_{V_n}(f)df = S_{I_n} \cdot \int Z_{out}^2(f)df \quad (5)$$

$$\sigma_{t_{dN1}}^2 = \frac{\overline{V_n^2}}{(I_D/C_m)^2} \quad (6)$$

where $S_{V_n}(f)$ and S_{I_n} are the spectral densities of the integrated voltage noise and current noise, respectively. In this case, S_{I_n} refers to the shot noise, modeled as $S_{I_n} = 2qI_D$. $Z_{out}(f)$ is the output impedance of the eNeuron circuit and is formed by

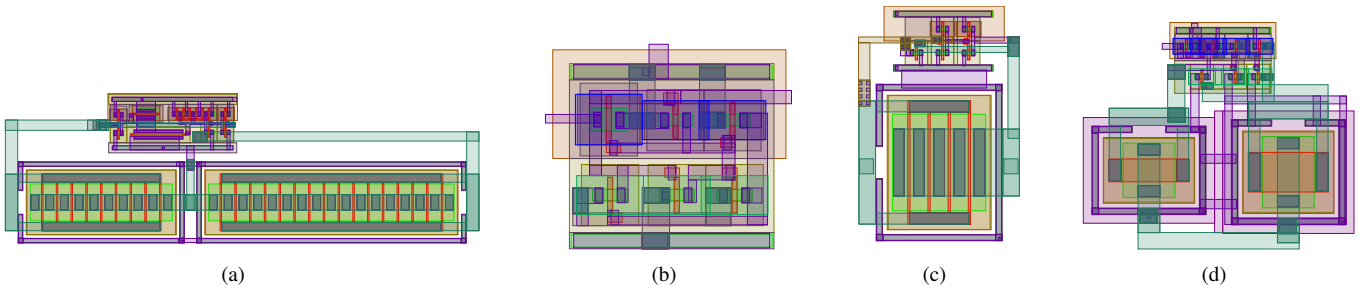


Fig. 5. Proposed layouts for eNeurons under test: (a) *eNeuron1* using $5.7 \times 17.3 \mu\text{m}^2$ [3], (b) *eNeuron2* using $2.3 \times 2.7 \mu\text{m}^2$ [9], *eNeuron3* using $6.6 \times 4.3 \mu\text{m}^2$ [10], and *eNeuron4* using $6.5 \times 7.8 \mu\text{m}^2$ [11].

the parallel combination of C_m and the total output resistances of transistors.

In addition to the jitter noise σ_{N1}^2 , during the discharge phase, the capacitance C_m integrates noise into current over the time window t_{dN} in the transistor MN_k . Thus, the appropriate jitter caused by this noise source is

$$\sigma_{t_{dN2}}^2 = \frac{q \cdot t_{dN}}{I_D} \quad (7)$$

where q is the electronic charge and I_D is the drain current of the transistor MN_k . In this specific case, all currents flowing into eNeuron membrane are considered in the same order of magnitude, i.e. I_D and I_{syn} are supposed to be equal.

Using (4) and the total jitter noise $\sigma_{t_{dN1}}^2 + \sigma_{t_{dN2}}^2$ integrated during the pull-down process, the variance of jitter noise in the eNeuron circuit can be expressed as

$$\sigma_J^2 = \frac{q}{I_{syn}} \left(\frac{1}{f_{spike}} + \frac{r_{ds} \cdot C_m}{\pi} \right) \quad (8)$$

where r_{ds} is the output resistance of a transistor and f_{spike} is the spiking frequency defined in a time-window. As the dynamic behavior of the spiking eNeuron can be approximated to that of an oscillator with a periodic waveform, $f_{spike} = (t_{dN} + 2 \cdot t_{dP})^{-1}$ is considered.

The phase noise can be directly linked to the period jitter as $\mathcal{L}(\Delta f) = \sigma_J^2 \cdot (f_{spike}^3 / \Delta f^2)$ [8], where Δf is the offset frequency relative to the spiking frequency of the eNeuron.

Post-layout simulations (PLS) are conducted to determine the order of magnitude of σ_J and compare it to the ΔT_s of temporal learning rules, like STDP, in analog SNNs. As mentioned in Sec. II-B, the substantial increase or decrease in the synaptic weight is obtained when ΔT_s is between $-1 \mu\text{s}$ and $1 \mu\text{s}$. In order to ensure that noise does not affect the spike timing of the eNeuron, the values of σ_J should be significantly lower than depicted ΔT_s .

For example, if the pre-synaptic spike precedes the post-synaptic spike ($\Delta T_s = 0.8 \mu\text{s}$), the weight of the synapse should strongly increase. However, if the time deviation of the pre-synaptic eNeuron is higher than ΔT_s , due to random jitter contribution, the pre-synaptic spike may occur after the post-synaptic spike. As a result, ΔT_s becomes a negative value that decreases the synaptic weight. Such an update might not be

the correct one, which could consequently impact the accuracy of the analog SNN.

IV. RESULTS AND DISCUSSION

Physical implementations for eNeurons described in Sec. II-A were designed in the BiCMOS SiGe 55 nm technology from ST Microelectronics, and are shown in Fig. 5 [17]. For ML eNeurons, the *eNeuron1* occupies $5.7 \times 17.3 \mu\text{m}^2$, and the *eNeuron2* occupies $2.3 \times 2.7 \mu\text{m}^2$. For LIF eNeurons, the *eNeuron3* occupies $6.6 \times 4.3 \mu\text{m}^2$, and the *eNeuron4* occupies $6.5 \times 7.8 \mu\text{m}^2$. The usage of the same technology and simulator for the four eNeurons will lead to a more equitable comparison between different eNeurons.

A. Phase Noise

The phase noise is obtained from Vistuso Spectre PNOISE and extracted for the four PLS eNeurons. Figure 6 presents the phase noise in function of the offset frequency relative to a $f_{spike} = 40 \text{ kHz}$. This choice is made to obtain the same spiking frequency for the four eNeurons. Thus, each eNeuron is excited with a different I_{syn} to generate this f_{spike} . As seen in this figure, as the offset frequency increases, the phase fluctuations of the eNeuron spikes increases, and the phase noise is then more important.

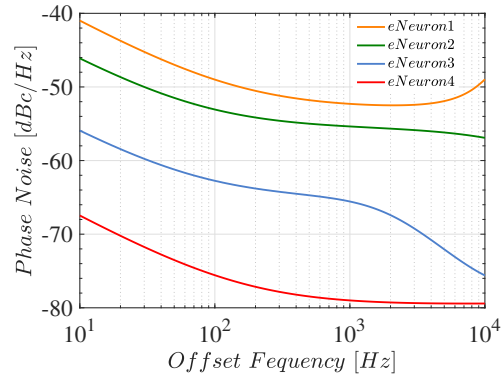


Fig. 6. The phase noise (PN) in function of the offset frequency relative to a $f_{spike} = 40 \text{ kHz}$ for the four designed eNeurons.

As demonstrated in (8), the phase noise $\mathcal{L}(\Delta f)$, which is related to the period jitter, is inversely proportional to the synaptic current I_{syn} and directly proportional to C_m . Figure 6 shows that *eNeuron1* has the highest phase noise in comparison with other eNeurons since it has the biggest C_m on its design [3]. *eNeuron2* has an important phase noise while it does not use a C_m . However, it is excited by a low I_{syn} to generate a $f_{spike} = 40$ kHz. For *eNeuron3* and *eNeuron4*, the phase noise is still important but lower than the one of others, as they are excited by higher values of I_{syn} to obtain this f_{spike} .

TABLE I
INTEGRATED NOISE SUMMARY IN ANALOG ENEURONS

eNeuron	Device	V_n^2 (V)	% of Total Noise
1	MN_k	0.165	53.42
	MP_{Na}	0.102	19.63
	MP_{syn}	0.34	21.94
2	MN_k	0.58	60.65
	MP_{Na}	0.22	57.7
3	MN_k	0.38	26.7
4	MP_{syn}	0.35	23.32

The summary of the integrated noise in the four analog eNeurons is presented in Tab. I. It highlights that the most contributor devices to noise in these eNeurons are the transistors MN_k , MP_{Na} and MP_{syn} , that correspond to the pull-up and pull-down branches, as modeled in Fig. 3. Moreover, it was seen that the integrated noise in these transistors is a shot noise, which validates the hypothesis used in Sec. III to express the jitter and the phase noise.

B. Period Jitter

To obtain the period jitter σ_J , a measure of the standard deviation of random variations in the time of each spike occurrence is calculated. For that, 1k-points PLS trans-noise iterations are extracted in a 1 ms time-window. Figure 7 shows the period jitter obtained for the four eNeurons as a function of spike occurrence. In this case, each eNeuron is excited by the same synaptic current ($I_{syn} = 50$ pA).

As shown in Fig. 7, the four eNeurons exhibit variations in the time of each spike occurrence, and these variations increase as the spikes are generated. For this synaptic current, *eNeuron1* (orange continuous line) and *eNeuron3* (blue continuous line) show a significant σ_J . Their values reach $3 \mu s$, which is three times higher than the order of magnitude of ΔT_s depicted in literature. *eNeuron2* (green continuous line) and *eNeuron4* achieve the lowest σ_J (red continuous line). Their values remain under $1 \mu s$ until the 30th spike occurrence. The reason for this is that *eNeuron2* is designed only using transistors, which reduces the propagation delay caused by current noise integrated into capacitance.

Furthermore, as depicted in (8), the value of σ_J depends on the frequency of the eNeuron. For the chosen synaptic current, *eNeuron3* has the fewest spikes in time compared to the other eNeurons [10], which results in the highest σ_J over spike occurrences. Despite the four types of eNeurons

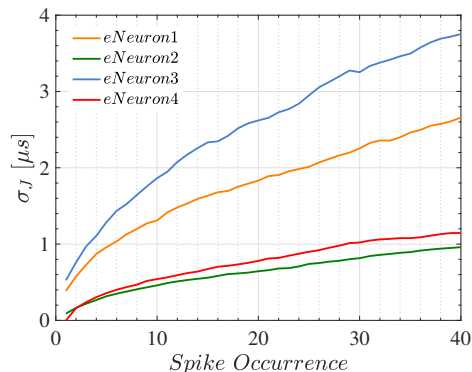


Fig. 7. The period jitter σ_J (in μs) in function of the spike occurrence for the four designed eNeurons.

described in the literature and used for STDP learning [6], [14], the obtained values for σ_J are either of the same order of magnitude or exceed ΔT_s .

C. Time Deviation and Spiking Frequency

In this section, the four eNeurons are excited with different I_{syn} to produce the same number of spikes ($N_{spike} = 40$) within a time interval of 1 ms. This results in the same spiking frequency ($f_{spike} = 40$ kHz). This approach aims to investigate the effect of the time deviation ΔT_n while holding f_{spike} constant, in contrast to the approach taken in Sec. IV-B.

The distribution of the ΔT_n for the first spike occurrence of the four eNeurons is presented in Fig. 8. It depicts the results of 1k iterations of PLS trans-noise. The distribution of ΔT_n for the *eNeuron3* shows a high variation coefficient (σ/μ) of 76% (see Fig. 8(c)), which is the lowest among all the eNeurons studied. In contrast, *eNeuron2* shows the highest variation coefficient at 445% (see Fig. 8(b)). The reason for this is that *eNeuron2* requires the lowest input current I_{syn} among the eNeurons to generate an $f_{spike} = 40$ kHz. According to (8), the jitter noise increases as I_{syn} decreases.

For the four eNeurons, ΔT_n is not negligible compared to ΔT_s (lower than $1 \mu s$) required for the synaptic weight update. Moreover, the distributions of ΔT_n demonstrate that the spike timing becomes a random variable that follows the noise. This produces a random synaptic weight update when these analog eNeurons are considered on an SNN trained using STDP learning.

Figure 9 illustrates the distribution of $f_{spike} = 40$ kHz for the four eNeurons obtained from 1k iterations of PLS trans-noise. Among the eNeurons, *eNeuron3* exhibited the most robust f_{spike} , with a coefficient of variation (σ/μ) of 0.2%, while *eNeuron1* and *eNeuron4* showed a slight variation of 0.5% in f_{spike} . In contrast, *eNeuron2* had a high variation in f_{spike} of 6%. This is due to the lack of C_m in its design, which produces an f_{spike} that depends on the random parasitic capacitances presented in its layout. This phenomenon gets even worse if process variability is considered.

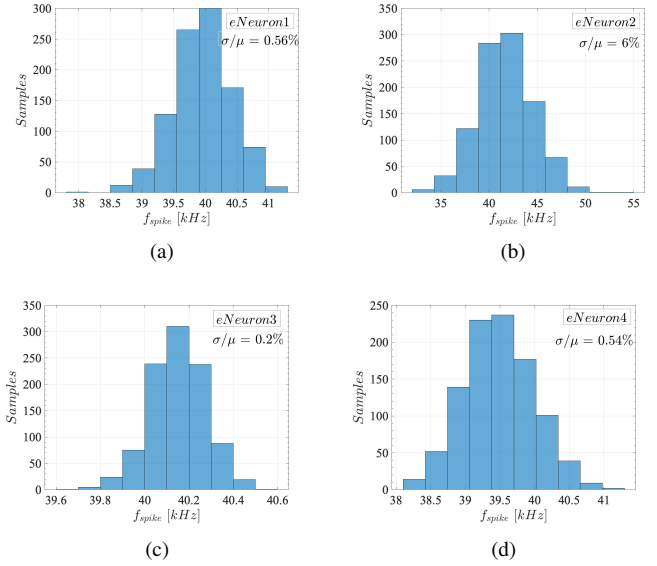
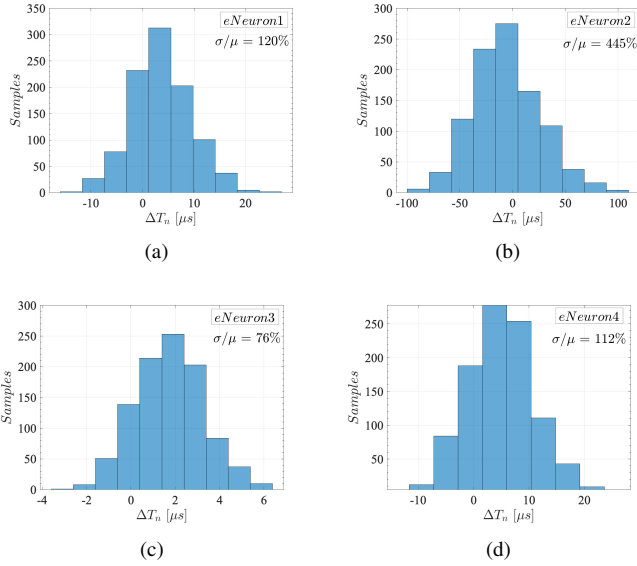


Fig. 8. Distribution of time deviation ΔT_n for 1k iterations of PLS trans-noise for (a) $eNeuron1$, (b) $eNeuron2$, (c) $eNeuron3$ and (d) $eNeuron4$ for the same $N_{spike} = 40$ within a time interval of 1 ms.

Fig. 9. Distribution of spiking frequency f_{spike} for 1k iterations of PLS trans-noise for (a) $eNeuron1$, (b) $eNeuron2$, (c) $eNeuron3$ and (d) $eNeuron4$ within a time interval of 1 ms.

D. Discussion

This study shows that the jitter noise strongly affects the spike timing of the low-power analog eNeurons with high f_{spike} . The synaptic weights may then be randomly updated in response to the noise. Thus, analog SNN, where STDP learning is applied and low-power eNeurons are used, may have a random degradation in the accuracy. However, the f_{spike} of an eNeuron, where C_m is considered in its design, is less affected by jitter noise. The feasibility of using an activation function based on the non-linear relationship between output f_{spike} and input I_{syn} for learning analog SNNs was recently studied in [16].

V. CONCLUSION

This paper presented the impact of noise on the spike timing, which is the critical characteristic for STDP learning, in analog eNeurons. PLS demonstrated that the spike timing is significantly influenced by a random jitter noise, with a variation that exceeds 76%. This result may limit the accuracy of the analog SNN, where low-power high firing rate eNeurons are implemented and the STDP learning rule is used. A learning rule avoiding spiking time and purely based on spiking frequency may be more robust against jitter noise, as it has a variation less than 0.2%.

REFERENCES

- [1] C. D. Schuman *et al.*, “A survey of neuromorphic computing and neural networks in hardware,” 2017. doi: 10.48550/arXiv.1705.06963
- [2] A. Shrestha *et al.*, “A survey on neuromorphic computing: Models and hardware,” *IEEE Circuits and Systems Magazine*, 2022. doi: 10.1109/MCAS.2022.3166331
- [3] P. M. Ferreira *et al.*, “Neuromorphic analog spiking modulator for audio signal processing,” *Analog Integrated Circuits and Signal Processing*, 2021. doi: 10.1007/s10470-020-01729-3

- [4] F. Danneville *et al.*, “Sub-0.3V CMOS neuromorphic technology and its potential application.” 2021. doi: 10.1109/CBMI50038.2021.9461899
- [5] R. Weiss *et al.*, “STDP based online learning for a current-controlled memristive synapse,” *IEEE/MWSCAS 2022* doi: 10.1109/MWSCAS4063.2022.9859294
- [6] B. Joo *et al.*, “Energy and area efficient CMOS synapse and neuron for spiking neural networks with STDP learning,” *IEEE Transactions on Circuits and Systems I: Regular Papers*, 2022. doi: 10.1109/TCSI.2022.3178989
- [7] C. Sun *et al.*, “An energy efficient STDP-based SNN architecture with on-chip learning,” *IEEE Transactions on Circuits and Systems I: Regular Papers*, 2022. doi: 10.1109/TCSI.2022.3204645
- [8] A. Abidi, “Phase noise and jitter in CMOS ring oscillators,” *IEEE Journal of Solid-State Circuits*, 2006. doi: 10.1109/JSSC.2006.876206
- [9] H. Takaloo *et al.*, “Design and analysis of the Morris Lecar spiking neuron in efficient analog implementation,” *IEEE Transactions on Circuits and Systems II: Express Briefs*, 2023. doi: 10.1109/TCSII.2022.3203929
- [10] F. Danneville *et al.*, “A sub-35 pW axon hillock artificial neuron circuit,” *Solid-State Electronics*, 2019. doi: 10.1016/j.sse.2019.01.002
- [11] M. Besrou *et al.*, “Analog spiking neuron in 28 nm CMOS.” *IEEE/NEWCAS*, 2022. doi: 10.1109/NEWCAS52662.2022.9842088
- [12] S. Moriya *et al.*, “A fully analog CMOS implementation of a two-variable spiking neuron in the subthreshold region and its network operation,” *IEEE/IJCNN 2022*. doi: 10.1109/IJCNN55064.2022.9891920
- [13] A. Gautam and T. Kohno, “An adaptive STDP learning rule for neuromorphic systems,” *Frontiers in Neuroscience* 2021, doi: 10.3389/fnins.2021.741116
- [14] S. K. Vohra *et al.*, “CMOS circuit implementation of spiking neural network for pattern recognition using on-chip unsupervised stdp learning,” 2022. doi: 10.48550/arXiv.2204.04430
- [15] T. Grasser, *Noise in Nanoscale Semiconductor Devices, Book*, 2020. doi: 10.1007/978-3-030-37500-3
- [16] T. Soupizet *et al.*, “Analog Spiking Neural Network for the MNIST,” *Journal of Integrated Circuits and Systems* 2023. doi: 10.29292/jics.v18i1.663
- [17] J. R. Raposo *et al.*, “IC-layout render: Image rendering tool for integrated circuit layout in python.”, 2021. doi: 10.5281/zenodo.5618268