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A *G*-Band Packaged Amplified Noise Source Using SiGe BiCMOS 55-nm Technology

Victor Fiorese¹, João Carlos Azevedo Gonçalves¹, Simon Bouvot¹, Sylvie Lépilliet, Daniel Gloria¹,
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Abstract—This article introduces the first BiCMOS SiGe technology-based packaged noise source (NS) operating in the *G*-band (140–220 GHz). An amplified *p-n-j* junction diode has been packaged and biased in avalanche mode to generate excess noise ratios (ENR_{av}) of approximately 25 dB between 140 and 170 GHz at package output for an unbiased low state and a high state corresponding to a 20-mA cathode current. The two-stage amplifier is a cascode cell composed of two BiCMOS 55-nm NPN very high speed (NPNVHS) transistors with an emitter length and a width of 5.56 and 0.2 μm, respectively. An optimal biasing results in a 8.2-mA current consumption for one cascode stage and an overall available power gain (*G*_{av}) better than 12 dB between 140 and 180 GHz. This supports operation in a low state, where the diode is unbiased and the amplifier is biased, which constitutes a scheme that easily validates the minimum detectable signal (MDS) condition while exhibiting a 14-dB ENR_{av} level in the beginning of *G*-band compared to this polarized low state. This NS shows a monitorable *P*_{COLD} and is adaptable to several noise receivers. In addition, the ENR_{av} level flatness is better than 3 dB over the entire frequency range, and the impedance matching, better than −7.5 dB at package output, is not dependent on the NS bias condition. Noise figure (NF) extraction of a WR05-connectorized III–V amplifier [MPA04-1 from Virginia Diodes, Inc. (VDI)] was performed and compared to the ELVA ISSN-05 commercial NS measurement, showing low discrepancy. The same study was performed on-wafer for an NPNVHS transistor on BiCMOS 55-nm technology, showing a maximum discrepancy of 0.8 dB between the two measured NFs. The NF measurement accuracy of the MPA04-1 amplifier was

assessed up to 220 GHz, by varying the chosen high state while keeping the low state completely unbiased. A maximum 0.5-dB variation over 12 obtained NF values is observed up to 200 GHz.

Index Terms—ENR_{av}, *G*-band, NF50, organic substrate, SiGe BiCMOS 55 nm, split block, tunable low state.

I. INTRODUCTION

RECENT years show great interest in the *D*- and *G*-band noise sources (NSs) development to address applications, such as remote sensing instruments based on millimeter-wave (mmW) radiometers used for meteorological forecasting [1], [2], [3], [4], [5] and 6G perspectives. Remote sensors including low-Earth orbit (LEO) remote imagers and sounders and geostationary (GEO) atmospheric sounders need high degree of sensitivity. These systems rely on fundamental building blocks, such as frequency mixers [6], [7], power detectors, low noise amplifier (LNA), switch [8], coupler [9], and NSs [10]. From another use case perspective, upcoming mobile communication networks will have to support applications ranging from immersive reality to haptic sensing and actuation without neglecting the real-time, ultralow latency and reliability requirements for mission critical communications involving, e.g., vehicle traffic control, automated critical process management, assisted, and remote surgery [11]. Beyond the current commercial deployment of 5G, this implies that 6G is bound to continue its relentless expansion into the 100–300-GHz bands, where the aforementioned satellite exploration and radio astronomy applications have already spread at specific frequencies. Obviously, the success of 6G is intimately tied to the performance of transistors and circuits to meet the requirements in terms of frequency rise, available gain, output power, and noise figure (NF) needed to compensate for higher path losses in the millimeter wavebands [12]. From that perspective, recently developed heterojunction bipolar transistors (HBTs) have already demonstrated operating frequencies of 505/720 GHz for f_T/f_{max} [13], and current developments at STMicroelectronics are targeting 400/600 GHz leveraging a SiGe BiCMOS 55-nm technology [14], compatible with industrial 300-mm fabrication lines. To lay the groundwork for 6G development, constant, monitorable, and compact NSs in the frequency bands covering the 100–300-GHz interval are therefore essential to enable silicon devices and circuits noise characterization and modeling in that frequency range. Several published contributions demonstrated noise generation with solid-state NS using diodes biased in avalanche

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regime [15], [16], [17], [18], [19], while others show promising performance when using BiCMOS amplifiers [20]. An accurate and comprehensive state-of-the-art of mmW, sub-mmW, and THz NS is proposed in [2]. Commercially available NSs are mainly based on IMPATT diodes biased under 28 V exhibiting an impressive excess noise ratio (ENR) of 50 dB [21]. However, ENR flatness is worse than 20 dB of variation within a 25-GHz frequency range [21]. This may lead to noise receiver saturation or to insufficient noise power injection to validate the minimum detectable signal (MDS) condition [16] in some parts of the targeted frequency spectrum. In this work, SiGe BiCMOS 55-nm packaged NSs are described. While having the advantage of sufficient ENR_{av} of up to 25 dB in the 140–170-GHz frequency range, the developed packaged NS is monitorable and shows a constant output matching, regardless of the biasing condition, which is a key feature for noise measurement accuracy [22]. Moreover, the presence of an amplifier at p-n diode output enables a low-state biased operating mode, facilitating the MDS condition validation by choosing a biased low state, where the NS itself is unbiased and the amplifier is biased. The result is a lowered ENR_{av} , due to a decrease in the difference in generated noise powers between low state and high states, but this technique allows to adapt the noise power injected at the noise receiver input, depending on the device under test (DUT) available power gain $G_{\text{av,DUT}}$, DUT NF NF_{DUT} , and receiver NF NF_{RCV} . To the best of our knowledge, this is the first packaged NS based on SiGe technology with such performance in the G -band (140–220 GHz). To place this development beyond the simple feasibility standpoint, repeatability and robustness studies have been conducted on several packaged NS specimens, through multiple assemblies/disassemblies. In detail, this article is organized as follows. Section II is the description of the SiGe BiCMOS circuits used as an NS. Section III covers the packaging technique and the electromechanical structures of the assembled NS. Section IV shows the main characterization results obtained in G -band in terms of S -parameters and ENR_{av} , including the detailed description of the methodology for its extraction. In order to validate the NS hardware and the associated methodological approach, the NF50 extraction of a III–V amplifier (WR4.3AMP, denoted MPA04-1 in this article) from Virginia Diodes, Inc. (VDI) [23] and an on-wafer NPN very high speed (NPNVHS) B55 bipolar transistor in the G -band is detailed. The NF extraction method is described, and the obtained results are compared with those from measured noise powers generated by a commercially available NS. Section V gives measurements repeatability assessment for S -parameters and ENR_{av} of such packaged NS. Over ten NS packages were assembled and measured to assess S -parameters and noise performance reproducibility. An innovative packaging technique, allowing multiple assembly and disassembly based on graphene paper and low-cost organic substrates, is proposed. Finally, Section VI provides a synthesis of the main results and gives an overview of the available solutions and perspectives of this work.

II. SiGe BiCMOS 55-NM NS DESCRIPTION

The used NS active component is a SiGe BiCMOS 55-nm p-n diode, whose ENR level is monitorable up to 17 dB at

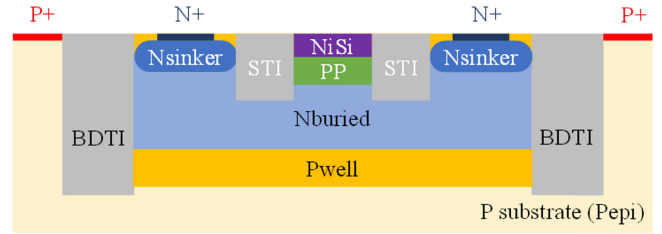


Fig. 1. Cross-sectional schematic view of a SiGe BiCMOS 55-nm p-n diode used as an NS. The p-doped region under anode is created with the PP implant, while the n-doped region is provided by the Nburied region [17].

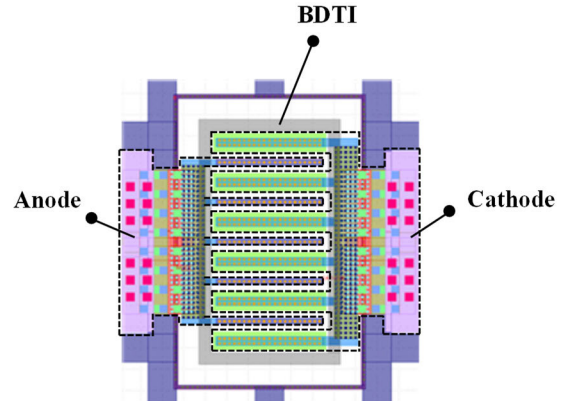


Fig. 2. Top layout view of SiGe BiCMOS 55-nm p-n diode (front-end view with back-end interconnections). Anode surface is $6.25 \mu\text{m}^2$.

260 GHz depending on the reverse bias current level in the avalanche regime [17]. Cross-sectional and top views of this diode are shown in Figs. 1 and 2, respectively.

The p-n junction is present between the PP (p-doped silicon) and N-buried ion implantations below the anode access. Shallow trench isolation (STI) provides electrical isolation between the anode and the cathode. The NS has been designed to achieve the correct tradeoff between cutoff frequency, front-end footprint, and noise generation. Therefore, the adopted geometry is a five-fingers anode, each finger being $5 \mu\text{m}$ long. The resulting anode surface is $6.25 \mu\text{m}^2$, allowing a maximum cathode current of approximately 25 mA before p-n junction breakdown. In this study, the maximum applied biasing current is limited to 20 mA to preserve samples.

To comply with package insertion losses (ILs) described in Section III, a LNA is used as a buffer stage, enhancing the generated noise power of the p-n diode. A layout view of the amplified NS is given in Fig. 3. It consists of a conventional two-stage cascode structure, each of which is composed of two NPN HBTs with an emitter width and a length of 0.2 and $5.56 \mu\text{m}$, respectively.

Fig. 4 shows a 15-dB gain between 130 and 160 GHz, relatively flat on this frequency band. LNA design and characterization are more detailed in [24]. Fig. 5 gives the schematic of this LNA. This gain is obtained for a bias of 1 and 2.2 V applied on the transistors base of each cascode stage and a 3-V collector supply voltage. The resulting current consumption of each cascode stage is 8.2 mA. The NS itself is the p-n junction diode previously shown in Figs. 1 and 2, with a matching network stage composed of an nMOS transistor in

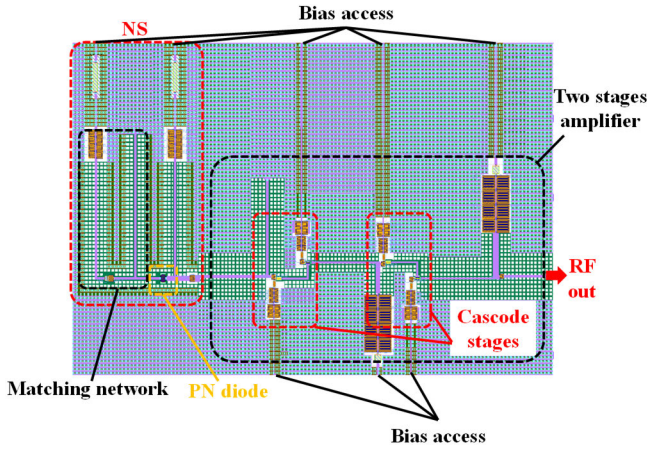


Fig. 3. Layout view of the on-wafer amplified NS. The p-n diode is in series with the two-stage LNA used as a buffer stage. A matching network is present both at p-n diode anode and at the two-stage amplifier input [24].

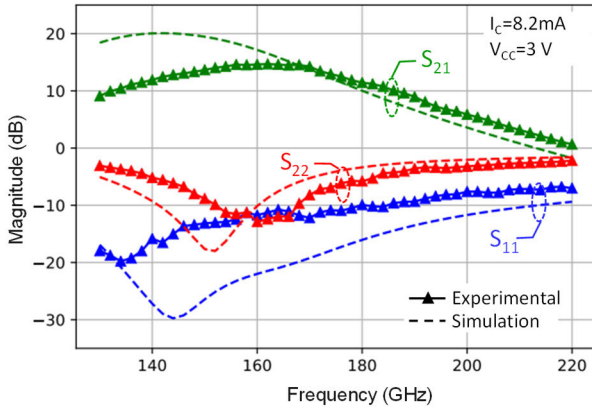


Fig. 4. Measured and simulated S parameters of the two-stage amplifier under a 3-V collector supply voltage and 1- and 2.2-V base voltages bias. The corresponding current consumption of one cascode stage is 8.2 mA [24].

linear regime and a stub. The nMOS transistor gate voltage can be tuned to control the matching impedance.

III. PACKAGING TECHNIQUE AND MECHANICAL STRUCTURE DESCRIPTION

A. Organic Substrate Design and Die Reporting

With regard to the substrate hosting the semiconductor chip, the literature contains many reports, where, for the frequency range under consideration, a quartz substrate is used for its very low-loss properties [25], [26]. Although quartz is an excellent material choice from the standpoint of dielectric properties, it is traditionally used as a thin substrate, around $50 \mu\text{m}$, for die housing. This makes it very fragile and costly, as well as not compatible with industrial assembly line tools. This study aims not only to develop the packaging of a tunable active NS but also to demonstrate the invariance and robustness of performance following multiple assemblies. To minimize the substrate cost and to be able to perform flip-chip (FC) assemblies of several dies, the chosen platform is a multilayer organic substrate, leveraging usual process-controlled materials. The six metallic layers organic substrate stack is described in Table I with a total thickness of $318 \mu\text{m}$

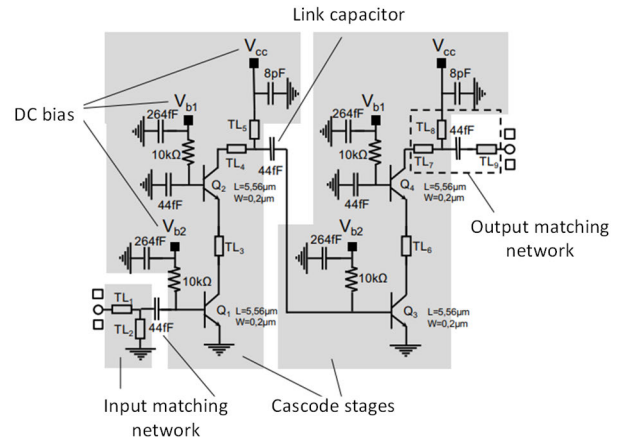


Fig. 5. LNA electrical schematic [24].

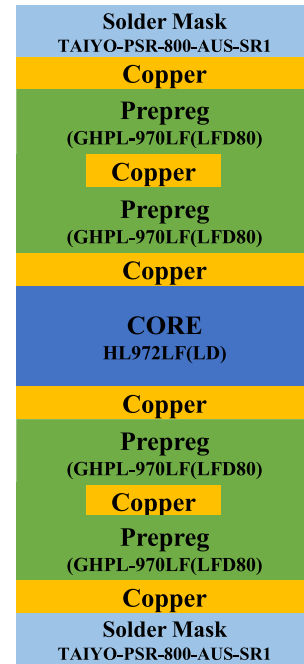


Fig. 6. Schematic cross section of the six metallic layers organic substrate designed and manufactured for flip-chipping the BiCMOS 55-nm die.

and a cumulative thickness tolerance of $30 \mu\text{m}$. A schematic cross section of this organic substrate is shown in Fig. 6. The substrate core is made of HL972LF(LD) [27], a low transmission loss nonhalogenated laminate material showing $3.4/0.004$ for Dk/Df constants at 10 GHz. The chosen prepreg material associated with this core is GHPL-970LF(LFD80) for manufacturing reasons. The values for Dk/Df were extrapolated from those measured up to 110 GHz and used for HFSS simulations.

Organic substrates are singulated by femtosecond laser cutting. This technique holds the distinctive advantage of excellent alignment accuracy and precise control of the kerf line by controlling several process parameters, such as average laser source power, pulse frequency and width, scan speed, and beam tilt angle. Following this process, an accuracy of $\pm 3 \mu\text{m}$ is obtained on the position and width of the

TABLE I
MATERIAL STACK-UP OF ORGANIC SUBSTRATE USED FOR
BiCMOS 55-NM FC ASSEMBLIES

Organic substrate stack		
Layer	Thickness (mm)	Material
Top Soldermask	0.015 ± 0.005	TAIYO-PSR-800-AUS-SR1
M1	Cu plating	Copper
	Cu foil	
ABF or Prepreg	0.03 ± 0.006	MITSUBISHI-GHPL-970LF(LFD80)
P1	Cu plating	Copper
	Cu foil	
ABF or Prepreg	0.03 ± 0.006	MITSUBISHI-GHPL-970LF(LFD80)
P2	Cu plating	Copper
	Cu foil	
Core	0.08 ± 0.008	MITSUBISHI-HL972LF(LD)
P3	Cu plating	Copper
	Cu foil	
ABF or Prepreg	0.03 ± 0.006	MITSUBISHI-GHPL-970LF(LFD80)
P4	Cu plating	Copper
	Cu foil	
ABF or Prepreg	0.03 ± 0.006	MITSUBISHI-GHPL-970LF(LFD80)
M2	Cu plating	Copper
	Cu foil	
Bottom Soldermask	0.015 ± 0.005	TAIYO-PSR-800-AUS-SR1
Total thickness	0.318 ± 0.03	

kerf line. The substrate surface finish is full organic solder preservative (OSP) with the addition of 15- μm -thick solder mask (SM). Some SM openings (SMOs) are performed on substrate top and bottom surfaces, where the chip is attached and for taking ground contacts. These SMOs have a dimension of $650 \times 850 \mu\text{m}^2$ with horizontal and vertical pitches of 650 and 450 μm , respectively. A substrate layout view is given in Fig. 7.

SMOs are filled with solder balls with a height of 30 μm extending beyond the SM outer face. The process sequence applied for solder application and FC die assembly on organic substrate is as follows: 1) solder dispensing on the substrate top surface, followed by chip attachment and reflow, and 2) solder dispensing on the substrate bottom surface followed by a second low-temperature reflow step. These reflow steps have been devised to prevent any degradation of the OSP FC pads. Fig. 8 is a view of solder pads dispensed after completion of the process. Several consecutive low-temperature reflow can be performed to monitor the solder height in excess of SM by changing its surface spreading on SMO.

On the semiconductor die side, the FC pad surface is a 30- μm -radius disk and consists of a 20- μm high copper pillar (CuPi). The under bump metallization (UBM) is circular

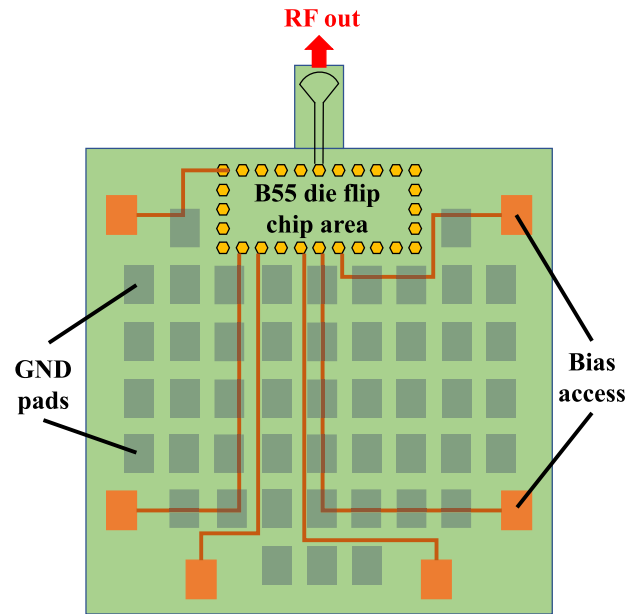


Fig. 7. Organic substrate layout detailing main features for B55 die packaging: dc signal routing, RF access, and SMO for GND reporting [28].

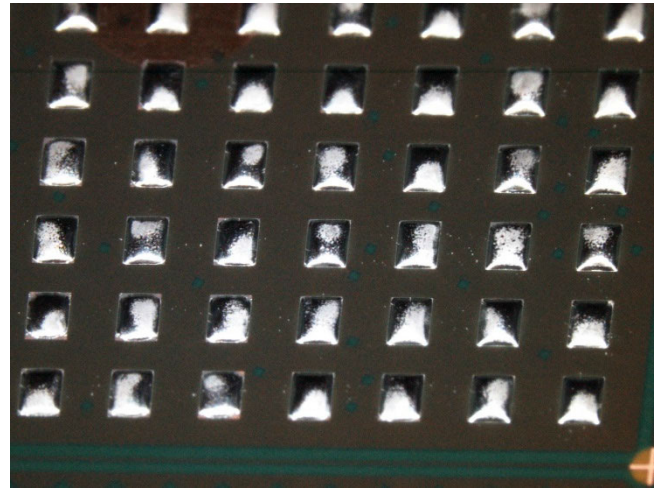


Fig. 8. Dispensed matrix of solder pads on bottom organic substrate surface after low-temperature reflow [28].

in shape with a 60 μm diameter and the FC pads pitch is 99 μm . This UBM is composed of a 0.15- μm -thick Ti/Cu alloy layer. The technique used to manufacture such bump is called “bump on pad.” This process consists in seven main steps. UBM sputtering is performed to improve conductivity at pad surface.

Then, UBM plating is done selectively due to a resist patterning before the bump plating step, where the SnAg alloy is deposited on the UBM plated zone. Some resist and UBM removals are performed afterward, combined with a thermal bump shaping step. The bump material is a Cu/SnAg alloy. A polyimide passivation step is required to protect bumps against the potential impact of moisture over the long term.

A complete BiCMOS B55 wafer was processed according to the specifications of this bumping process and cut to singulate 64 chips, on which the NSs comprising a single diode and its

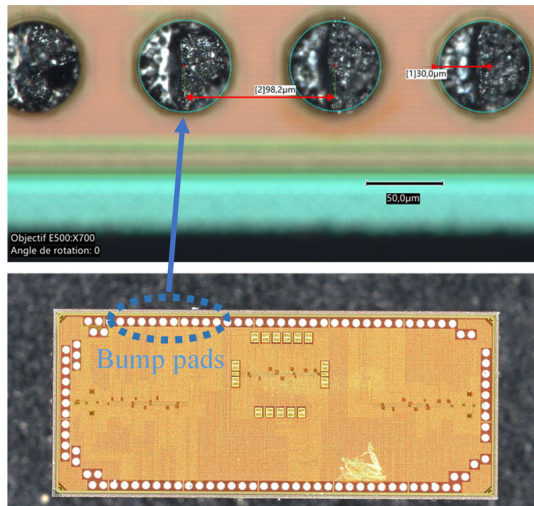


Fig. 9. Singulated SiGe BiCMOS 55-nm chip with CuP is grown on bump pads for FC assembly. CuPis have a 30 μm radius and 99 μm pitch [28].

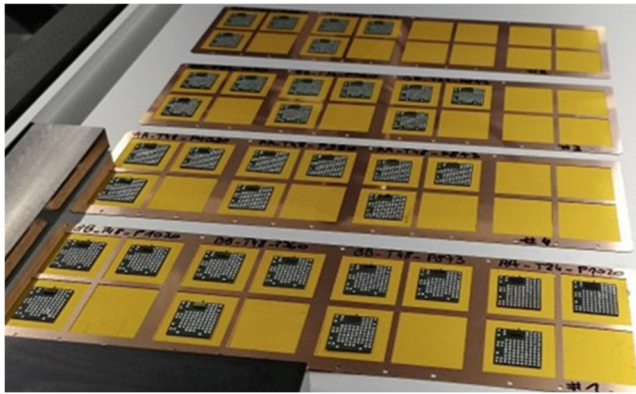


Fig. 10. Samples of substrates with reported B55 dies [28].

amplified version were embedded. A view of such a singulated die with CuPi grown on bump pads is shown in Fig. 9.

Finally, diced dies were flip-chipped onto the pre-cut organic substrates following the process sequence described above. Fig. 10 is a view of the final 36 pieces of B55 dies assembled on organic substrates. At this stage, an X-ray check was performed to verify the quality of the internal dc routing tracks and the FC transfer-bonding step, without showing any defectivity. Fig. 11 is a zoom on one of the singulated and flip-chipped BiCMOS 55-nm die on a cut organic substrate.

B. Split-Block Package Design

The NS substrates have been packaged into a two-parts mechanical split-block fabricated using a classical computer numerical control (CNC) machining process in a brass alloy with gold plating on surfaces to enhance the guiding of the mmW signal. At such frequencies, surface roughness may have a significant impact on ILs. A 7- μm -thick Ni/Au surface finishing has therefore been applied to minimize surface roughness and improve surface conductivity along the walls of the WR5 rectangular waveguide. Two split-block packages have been manufactured to assess the reproducibility of the

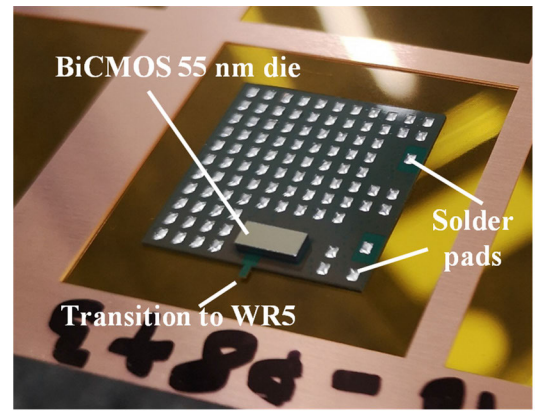


Fig. 11. BiCMOS 55-nm SiGe die containing the NS and amplified NS, flip-chipped on a singulated six metallic layers organic substrate. Solder pads have been deposited on substrate for homogeneous ground contact [28].

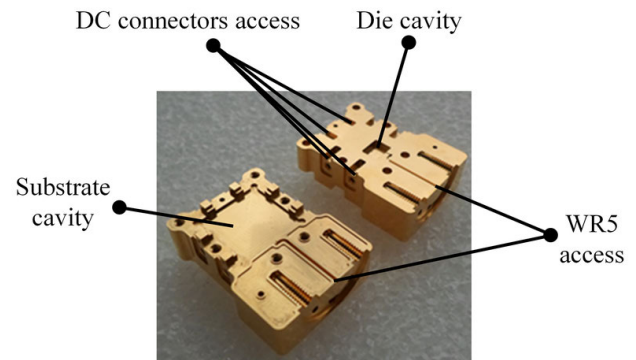


Fig. 12. CNC manufactured brass split-block after NiAu surface finishing [28].

package and its mechanical integrity. An open view of one of the two split-block packages is shown in Fig. 12.

To place this study in an industrial development context, the ease of use and variation of performance in relation to substrate assembly and disassembly have been investigated. To bring dc bias to NS dies, optimized routing metal tracks have been designed within the organic substrate. Specific solder pads have been placed on the top surface of the substrate. For ground contact, the idea is to reduce the parasitic resistance of ground feedback currents by applying as homogeneous as possible a substrate ground to all surfaces of the substrate. The mechanical split-block itself is used as a ground as well. The aim is to avoid additional soldering or wire-bonding during assembly for reasons of time saving and mechanical robustness. The conductive glue option was rejected due to the difficulty in controlling its thickness and the need to clean the surfaces on which it was dispensed afterward. For packaging, sheets of 120- μm -thick graphene paper were placed in split-block cavities below and above the substrate. When the split-block is closed and the mechanical assembly is tightened, solder pads arranged on the substrate surfaces induce a partial deformation of graphene paper. This layer is then in contact between the substrate ground signal and the split-block parts, which guarantees a homogenous ground contact between the substrate and the split-block. The depth of each split-block cavity was adjusted to ensure a partial deformation of the

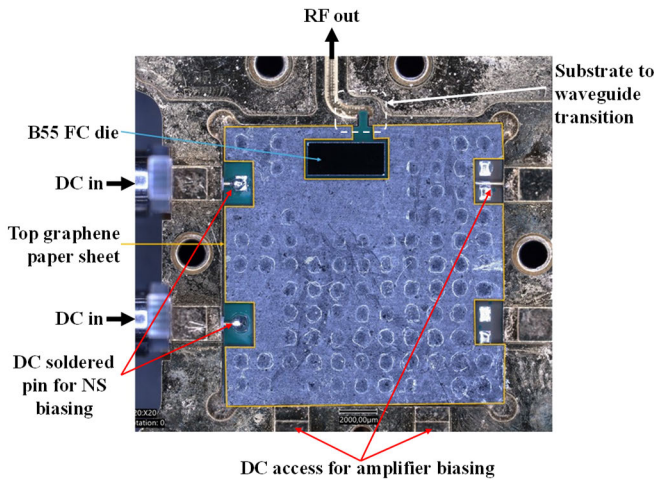


Fig. 13. Opened split-block package after assembly and tightening of an organic substrate with graphene sheets. In this case, the standalone NS is packaged. Three additional dc bias voltages are needed for the amplified version [28].

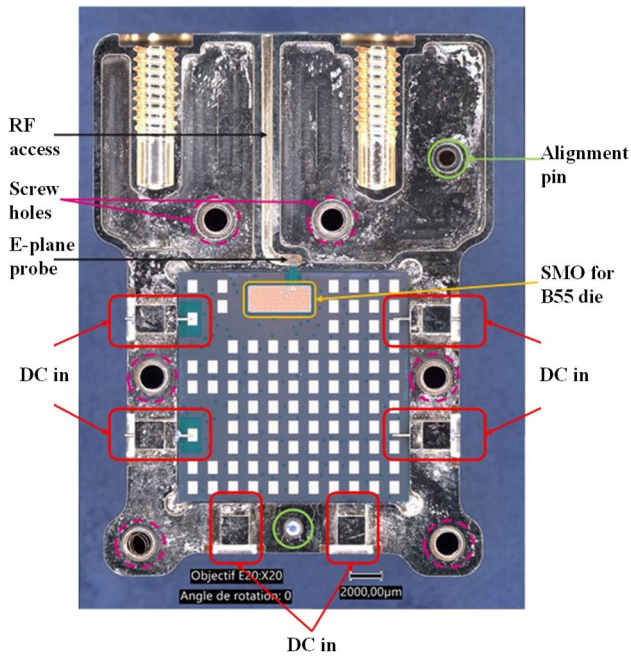


Fig. 14. Open brass split-block package with an organic substrate inserted into the cavity also showing the positioning of the *E*-plane transition in the rectangular hollow half waveguide [28].

top and bottom graphene sheets when tightening the package, thereby improving self-placement and locking of the substrate position.

Fig. 13 gives a view of the opened split-block after assembly and tightening of an organic substrate. The top graphene sheet is visible and partial deformation at solder pads positions is noticeable.

An additional view of the opened split-block is proposed in Fig. 14. In this case, neither the chip has yet been assembled nor solder pads distributed. Six screws are used for tightening and two alignment pins ensure that the split-blocks are correctly positioned with respect to each other. Once assembled, the split-block package features a WR5 mmW flange

termination, allowing interconnection with an external mmW probe or DUT. The overall split-block size is approximately $40 \times 27 \text{ mm}^2$ and is 30 mm thick.

The rectangular SMOs for ground contact and dc biasing are clearly visible in Fig. 14. Ground contacts have been arranged as evenly as possible on the substrate surface to ensure a consistent ground contact quality. With this split-block housing, up to six dc bias signals can be fed to the NS die independently. dc male connectors are fixed by screws to external faces of the split-block. The central pin of the connector penetrates the metal body of the split-block through a cylindrical hole. The hole is filled with a hollow cylindrical Teflon tube to provide electrical insulation. The central metal pin can then slide, so that its end lands on a pad where it can be soldered with the addition of an alloy ball. Room for dc decoupling capacitance has been reserved in the split-block, but measurements showed that this provision was not necessary. In this study, the same silicon chip integrates both the simple NS based on an avalanche diode and its amplifier-augmented version. By imposing the constraint that the split-block can accommodate both types of NS, two types of substrates were designed with different routings of the interconnect traces. The NS circuit needs a cathode bias current to control the avalanche effect and a bias voltage for an impedance matching stage on the anode side. Fig. 14 corresponds to this nonamplified NS configuration showing the die assembled with two dedicated dc bias terminals. The other NS configuration is the same p-n diode with the addition of the two-stage amplifier shown in Fig. 3, which requires three additional dc bias voltages for NPN transistors base biasing and supplying the collector of the cascode stages.

The key transition for RF performance is the one between the organic substrate and the WR5 waveguide. This transition relies on an *E*-plane probe transforming a stripline propagation mode toward the TE₁₀ one of the rectangular waveguide cavities. The key parameters of such transition that determine the ILs and phase shift are the amount of dielectric material in waveguide cavity, the probe position, and back-short length. Fig. 15 shows the precise positioning of the *E*-plane transition resulting from the insertion of the organic substrate into the split-block cavity.

To place this study in a context of a potential industrial scale-up, a design of experiment (DOE) was carried out on the cutting and thinning of the organic substrate to assess the impact of the assembly tolerances on the dispersion of mmW performance.

The thickness and length of the dielectric beam under the *E*-plane bow tie were modified using several cutting and surface machining variants using a femtosecond laser. Two dielectric thicknesses and three different lengths of the dielectric beam have been selected as summarized in Table II. The DOE parameters are identified in Fig. 16 on the microscopy image showing the substrate in profile view with the dielectric beam supporting the *E*-plane transition and the flip-chipped silicon die. Each option corresponding to a given variant of laser cutting and thinning was produced in triplicate for the purpose of evaluating the repeatability of measurements.

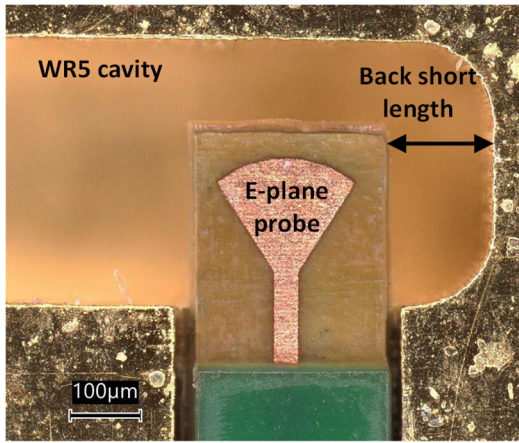


Fig. 15. *E*-plane probe transition between organic substrate and WR5 waveguide. Back short length is the distance between substrate edge and waveguide cavity edge [28].

TABLE II
FEMTOSECOND LASER DOE PARAMETERS VALUES

Thickness of dielectric below E plane probe T (µm)	Length of E-plane probe in WR5 cavity L (µm)
24	873
	960
	1020
48	873
	960
	1020

IV. MEASUREMENT RESULTS IN *G*-BAND

To confirm the functionality of the chips integrated into the packaged NS prior to making RF measurements, the bias current levels were systematically checked for an applied dc voltage bias, and additionally, the consistency of the avalanche diode voltage was checked for an applied dc current bias level. All the chips assembled on substrates were found to be functional, making the *S*-parameters and noise measurements in *G*-band possible. Results shown in this section mainly focus on the amplified packaged NS since it presents the most remarkable performance in terms of *S*-parameters, ENR levels, and MDS condition validation.

A. *S*-Parameters Measurements

One-port *S*-parameters measurements have been performed with a vector network analyzer (VNA) and Rohde & Schwarz mmW frequency extension heads in the *G*-band (ZC220 type). A setup view is proposed in Fig. 17. First, measurements were performed on packaged standalone NS to validate the packaging process on the simplest configuration. Then, the amplified NS version was characterized.

This setup allows to characterize the output matching of the amplified packaged NS for several bias conditions. A key aspect regarding the accuracy of noise measurement using the *Y*-factor method (see Section IV-B for more information) is to guarantee a constant NS output matching regardless of bias in order to avoid indistinguishable losses due to standing waves between the NS and the DUT. More specifically, when

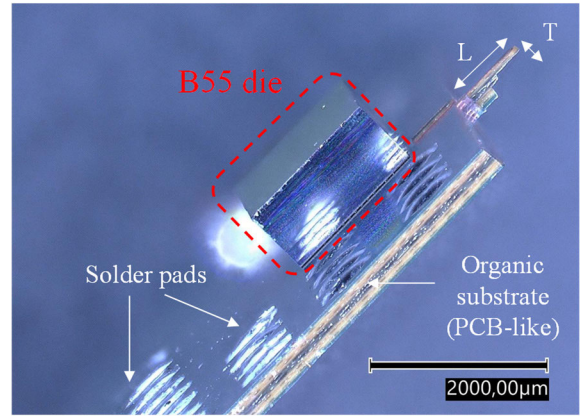


Fig. 16. Side view of a B55 die assembled on organic substrate showing DOE laser cutting parameters *L* and *T* [28].

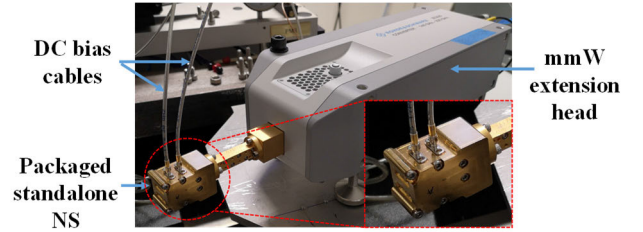


Fig. 17. One-port *G*-band *S*-parameters test setup of standalone packaged NS. The same setup was employed for the amplified packaged NS, with more dc cables to bias the buffer stage.

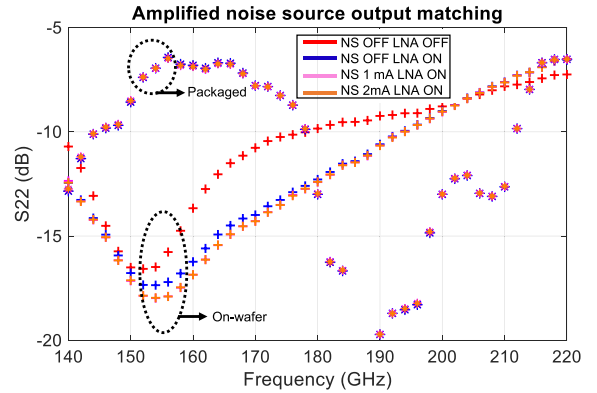


Fig. 18. Comparison of the amplified NS output matching (S_{22}) from measurements on-wafer and in packaged form output over the *G*-band for several bias conditions. Packaged configuration shows superimposed curves for various NS and LNA biasing.

measuring the *Y*-factor, the amplified NS is used in the OFF and ON states, OFF corresponding to an unbiased NS and ON corresponding to a biased NS. Fig. 18 shows the matching at the package output and provides a comparison with S_{22} of the NS measured on-wafer, i.e., without package. On-wafer impedance matching extraction plane is at FC pad input. Regarding the packaged configuration, impedance matching extraction plane is at package output.

The change in NS biasing has very little influence on the output matching due to the package losses. Superimposed curves at various NS and LNA biases and states are observed in Fig. 18 for the packaged version of amplified NS. The package losses have been extracted using short structures at several

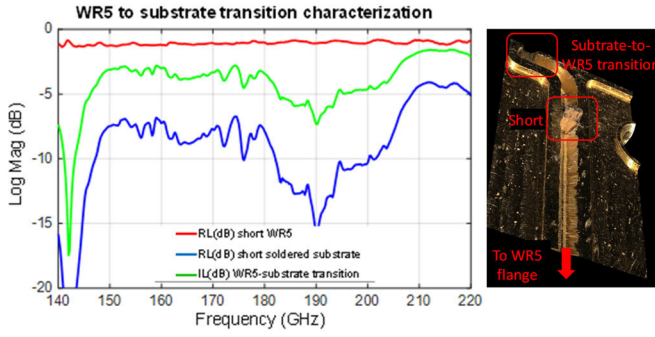


Fig. 19. Organic substrate to WR5 waveguide transition characterization. Measurement results of short structures and transition IL calculus [28].

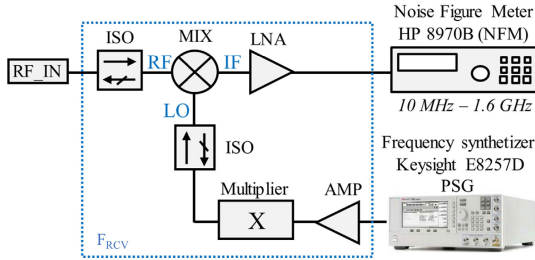


Fig. 20. Noise receiver architecture. This architecture is common to the two receivers used in the study, covering, respectively, 130–170- and 170–220-GHz frequency ranges [17].

reference planes to infer the IL of the substrate to waveguide transition, as shown in Fig. 19. A first short structure was made with an iron sheet placed in waveguide cavity. A second short structure was emulated on a substrate without die by soldering RF line to adjacent ground. With these two structures, it was possible to extract substrate to waveguide transition IL. Fig. 19 displays the characterization results of the shorts. Transition IL [$IL_{\text{transition}}(\text{dB})$] was calculated from measured return loss of short structures [$RL_{\text{shortWR5}}(\text{dB})$, $RL_{\text{shortsolder}}(\text{dB})$] as explained in the following:

$$IL_{\text{transition}}(\text{dB}) = \left| \frac{RL_{\text{shortWR5}}(\text{dB}) - RL_{\text{shortsolder}}(\text{dB})}{2} \right|. \quad (1)$$

One can infer from Fig. 19 that substrate to waveguide transition dictates the IL (dB) observed in Fig. 18 for the packaged NS configuration. These losses have been estimated to be 4 dB in average in the 140–220-GHz frequency range. One key feature is the constant output matching observed regardless of amplified NS biasing. This aspect is particularly important when operating in the two temperatures method for noise measurement accuracy concerns. The observed shape in S_{22} is due to transition IL, showing a notch at 190 GHz and approximately -7 dB around 160 GHz. This behavior is also depicted in Fig. 31, where $S_{22}(\text{dB})$ has been measured over three consecutive assemblies of an NS.

B. Available ENR (ENR_{av}) Extractions

Considering the mismatch between the packaged NS and the DUT, the ENR level (dB) has been extracted with the knowledge of packaged NS output matching in the G-band. The effective uncalibrated noise power was measured for

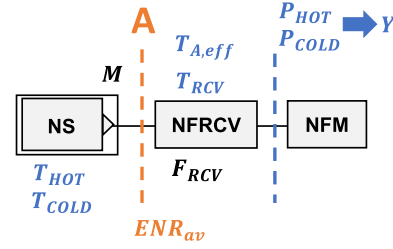


Fig. 21. Block diagram of the setup used for ENR_{av} (dB) extraction of amplified packaged NS.

several NS bias states and transposed to available noise power in the input plane of the noise receiver with the knowledge of its noise factor (F_{RCV}), characterized in previous works with the Y-factor method. Reference planes are shown in Fig. 21. Plane A corresponds to the noise receiver input plane. P_{HOT} and P_{COLD} are measured at NF meter (NFM) input plane, since NFRCV down converts and amplifies measured RF signal to NFM frequency range. Fig. 20 gives more details regarding NFRCV architecture.

Using (2), one can deduce T_{RCV} from F_{RCV} and T_0 . It is the first step leading to $ENR_{av}(\text{dB})$ extraction

$$T_{RCV} = T_0(F_{RCV} - 1) \quad (2)$$

with T_{RCV} the equivalent noise temperature of the noise receiver and $T_0 = 290$ K. Using the NS in low and high states, the Y-factor is defined as in the following:

$$Y = \frac{P_{HOT}}{P_{COLD}} \quad (3)$$

with P_{HOT} and P_{COLD} being the measured noise powers at the input of the NFM for a high state and low state of the amplified NS, respectively. As a result, the effective hot noise temperature in the input plane of the noise receiver is given by the following:

$$T_{A,eff} = T_{RCV}(Y - 1) + Y \frac{T_{cold}}{M} \quad (4)$$

with M being the impedance mismatch coefficient between the packaged NS and the noise receiver, and T_{cold} the NS equivalent noise temperature when the NS and the amplifier are unbiased and supposed known close to 290 K. T_{RCV} is deduced from the measured value of F_{RCV} and provides calculation of $T_{A,eff}$. In our case, the noise receiver features an isolator at its input and is therefore considered as a $50\text{-}\Omega$ load. With this knowledge, M can be expressed as shown in (5). Due to amplifier isolation and package losses, the resulting mismatch coefficient is close to 1 in the entire frequency range

$$M = \frac{1}{(1 - |\Gamma_{OUT, PackagedNS}|^2)}. \quad (5)$$

The available hot noise temperature in the input plane of the noise receiver can be subsequently deduced from $T_{A,eff}^{HOT}$ and M by the following:

$$T_{An,av}^{HOT} = M \cdot T_{A,eff}^{HOT}. \quad (6)$$

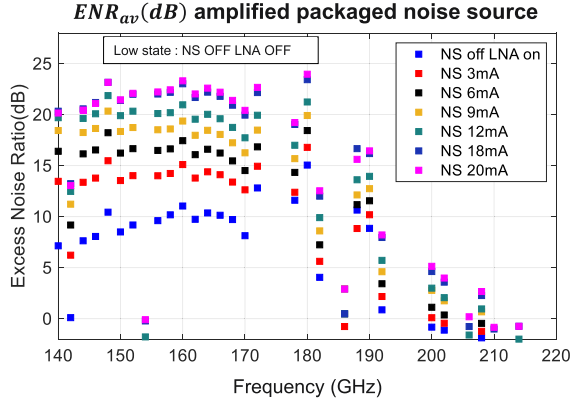


Fig. 22. Extracted ENR_{av} (dB) in G -band from the developed amplified packaged NS under several bias conditions [28].

While ENR_{av} (dB) can be deduced by the following:

$$ENR_{av}(\text{dB}) = 10 \log \left(\frac{T_{HOT}^{A,av} - T_{COLD}^{A,av}}{T_0} \right) \quad (7)$$

where $T_{HOT}^{A,av}$ and $T_{COLD}^{A,av}$ correspond to $T_{A,av}$ when the amplified NS is biased and unbiased, respectively. T_A describes the noise equivalent temperature at A plane shown in Fig. 21. Note that one key feature of the present packaged NS is that it can be monitored. Thus, multiple ENR_{av} values can be generated, making this NS adaptable to a wide selection of noise receivers and DUTs. The extracted ENR_{av} values are represented in Fig. 22, for a low state of the NS for which both the avalanche diode and the amplifier are not biased, i.e., NS OFF and LNA OFF. Some ENR values are missing or showing divergences regarding other ENR values measured at adjacent frequency points due to noise receiver frequency response. More specifically, the noise receiver mixer shows some limitation in gain conversion at specific frequency points. This results in a reduced noise receiver sensitivity and can be observed on the extracted ENR_{av} levels at 154 and 178 GHz, as shown in Fig. 22.

These results demonstrate a distinctive feature of the greatest interest of this NS in that ENR_{av} is monitorable to levels up to 24 dB with a 2-dB flatness between 140 and 170 GHz. Table III gives an overview of the mmW NSs state of the art. The proposed solution shows available ENR levels in line with the existing commercial solutions, while leveraging SiGe technology, compatible with high volume packaging. The key feature is the ability to monitor these ENR levels by adjusting the NS biasing to the noise receiver sensitivity. Moreover, ENR flatness is among one of the best reported in literature. This is an important aspect since high ENR-level frequency variations can induce either noise receiver saturation of insufficient injected noise powers with regard to the MDS condition.

C. Noise Figure Measurement in G -Band

The developed packaged NS has been used to extract the NF of several DUTs, using a set of two noise receivers [140–170 GHz (Rx1) and 170–260 GHz (Rx2)]. The first

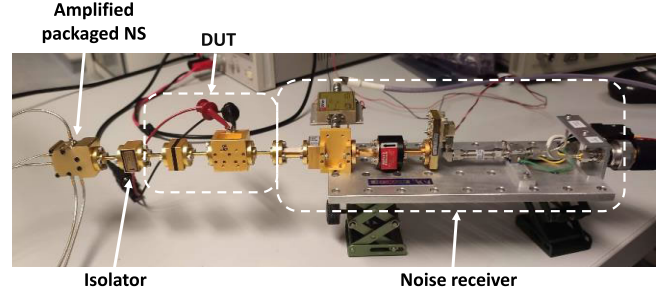


Fig. 23. Setup for NF measurements of MPA04-1 MPA amplifier with the developed SiGe packaged NS between 140 and 170 GHz.

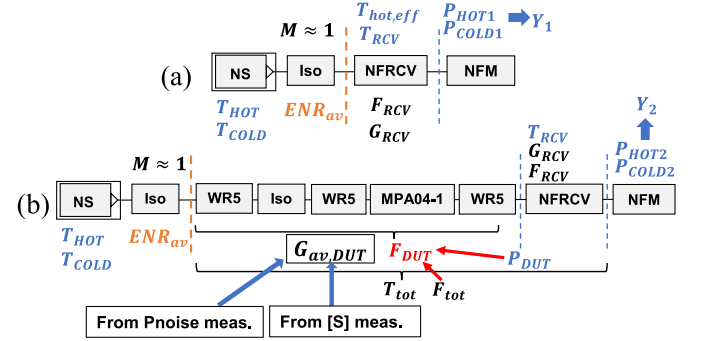


Fig. 24. Schematic setups for F_{DUT} extraction methodology. (a) Noise receiver calibration step with the amplified packaged NS, using the Y -factor method. An isolator ensures a constant 50Ω match for high and low bias states of NS. (b) NF measurement with the DUT in place between packaged NS and noise receiver.

DUT tested is a WR5 connectorized medium-power amplifier (MPA) MPA04-1 from VDI. This PA, initially designed for operation in 170–260 GHz, has an average G_{av} of 17 dB between 140 and 170 GHz. We want to stress that this band was chosen according to the availability of the noise receiver and solid-state NS, thus enabling the comparisons of NF extraction using different NSs and the same DUT. In this frequency range, the packaged NS has approximately 23 dB of ENR_{av} and the associated noise receiver has a 10-dB NF, making this setup relevant for NF extraction. Measurements were also performed with a commercially available NS solution to serve as a base reference. A setup view is shown in Fig. 23.

Fig. 24 illustrates the methodology employed to extract the NF of the MPA04-1 MPA. The NS is either the ELVA commercial solution or the developed packaged NS described in this article. The considered DUT is a group of elements consisting of a WR5 access flange, an isolator, another WR5 access flange, the MPA04-1 amplifier, and a third WR5 access line. The Y -factor method is employed by using the NS in several bias states. The first step consists in connecting the NS directly to the noise receiver and measuring two noise powers corresponding to OFF and ON states, hereafter referred to as P_{COLD1} and P_{HOT1} , respectively. This enables the calculation of a first Y -factor called Y_1 and the equivalent noise temperature at the receiver input T_{RCV} as described in the following:

$$T_{RCV} = \frac{T_{HOT} - Y_1 T_{COLD}}{Y_1 - 1} \quad (8)$$

TABLE III
MMW NSS STATE OF THE ART

Monitorable low state (P_{COLD})	$ENR_{av}(dB)$	Packaged	Technology	Monitorable	$ENR_{av}(dB)$ flatness	Frequency (GHz)	Constant output matching	Reference
No	45	Yes	IMPATT Diode	No	± 15	140-220	NA	ELVA ISSN-05 [21]
No	50	Yes	IMPATT Diode	No	± 20	220-330	NA	ELVA ISSN-03 [21]
No	10	Yes	NA	No	± 2	110-170	NA	VDI WR6.5NS [29]
No	8,5	Yes	NA	No	± 2	140-220	NA	VDI WR5.1NS [29]
No	25	Yes	NR Noisecom Process	No	± 2	18	No	NC346D Precision [30]
Yes	9	Yes	GaAs	Yes	± 2	170-200	NA	[19]
Yes	15-27	No	SiGe BiCMOS 130nm	Yes	± 5	90-270	Yes	[20]
Yes	<20 & 28	No	SiGe BiCMOS & UTC-PD	Yes	± 7	120-325	Yes <-10	[18]
Yes	37	No	SiGe BiCMOS 55nm	Yes	± 2	140-170	Yes <-7,5	[16]
Yes	24	Yes	SiGe BiCMOS 55nm	Yes	± 2	140-170	Yes <-7,5	This work

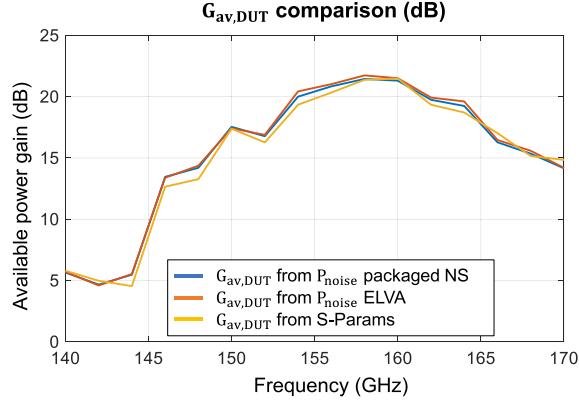


Fig. 25. DUT available power gain extractions based on S -parameters and measured noise powers from the present amplified packaged NS and the commercial ELVA NS [28].

where T_{HOT} and T_{COLD} are the noise equivalent temperatures associated with NS ON and OFF states, respectively.

The second step consists in measuring the noise powers in the same NS OFF and ON states in order to calculate a second Y -factor noted Y_2 with the DUT inserted in the measurement chain. The available power gain of the DUT $G_{av,DUT}$ can be calculated from these noise powers with the following:

$$G_{av,DUT} = \frac{P_{HOT2} - P_{COLD2}}{P_{HOT1} - P_{COLD1}}. \quad (9)$$

A comparison of $G_{av,DUT}$ extracted from S -parameters and noise powers is given in Fig. 25, where it can be observed that the maximum discrepancy is lower than 0.4 dB between 140 and 170 GHz.

These two steps allow the calculation of the noise receiver gain G_{RCV} , which is necessary for the calculation of the

NF at the input plane of the noise receiver, as detailed in the following:

$$G_{RCV} = \frac{P_{HOT1} - P_{COLD1}}{(T_{HOT} - T_{COLD})k\Delta_f} \quad (10)$$

where k is the Boltzmann constant, T_{HOT} and T_{COLD} are the equivalent noise temperatures of the NS in high and low states, respectively, and Δ_f is the noise receiver bandwidth. The knowledge of these parameters gives the expression of the available noise power P_{DUT} at the DUT output expressed by the following:

$$P_{DUT} = \frac{P_{COLD2}}{G_{RCV}} - kT_{RCV}\Delta_f. \quad (11)$$

Finally, the DUT linear noise factor (F_{DUT}) is given by the following:

$$F_{DUT} = \frac{P_{DUT}}{G_{av,DUT}kT_{COLD}\Delta_f}. \quad (12)$$

The extraction results are shown in Fig. 26. The packaged NS has the advantage to be controllable in terms of bias and was therefore used in three different ON states in order to assess the variability of measurements. The ELVA NS can be used to measure either calibrated or uncalibrated noise powers using a calibration algorithm corresponding to the associated 140–170-GHz noise receiver. For a fair and relevant comparison, one should consider in priority extractions made from uncalibrated noise powers with both NS. In this context, measurements show a maximum discrepancy between the packaged NS and ELVA NS of 0.3 dB at 146 GHz. P_{uncal} refers to NF extracted from uncalibrated noise powers. This is the only available technique with the proposed packaged NS since the calibration algorithm is only compatible with the ELVA commercial NS. One development axis could be to develop such algorithm associated with the introduced

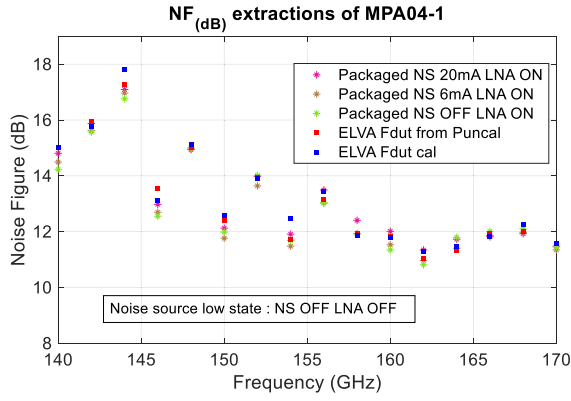


Fig. 26. Extracted NF of MPA04-1 using commercial ELVA NS and package NS with different bias conditions between 140 and 170 GHz [28].

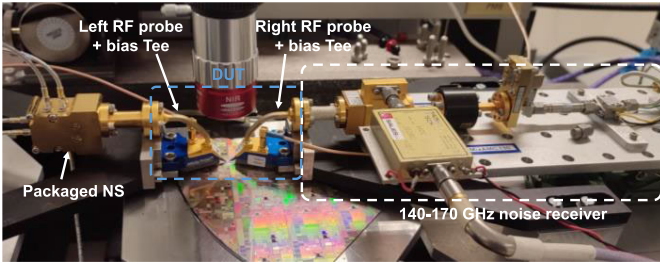


Fig. 27. On-wafer NPNVHS NF test setup with packaged NS between 140 and 170 GHz [28].

NS based on its available ENR levels. The three distinct NF measurements performed with the packaged NS under three bias conditions give a maximum dispersion of 0.4 dB at 140 GHz. These results prove the relevance of using the developed packaged NS compared with commercial NS solutions. In this variable bias measurement scenario, it is important to note that the waveguide flange assembly induces a typical variability of ± 0.2 dB at such frequencies, which contributes to the measurement dispersion mentioned above.

To further consolidate previous results, a bipolar transistor NPNVHS HBT in SiGe B55 technology has also been characterized on wafer with the packaged NS and commercial ELVA NS between 140 and 170 GHz. A picture of the setup is given in Fig. 27. The considered DUT is the group of elements consisting in the left RF probe, the B55 NPNVHS bipolar transistor, and the right RF probe. The NPNVHS bipolar transistor has $5.56 \times 0.2 \mu\text{m}^2$ emitter length and width, respectively. It is biased under a collector current of 7.8 mA. A similar NF extraction methodology to that used previously was employed, using two measurement steps, with and without the DUT. Extraction results are represented in Fig. 28. A comparison is also made between the ELVA calibrated and uncalibrated noise powers and packaged NS noise powers. The discrepancy between the packaged amplified NS and the ELVA extractions is less than 0.8 dB in the 140–170 GHz range. This gap tends to be larger as the available power gain of the DUT decreases.

Finally, an assessment of the accuracy of NF extraction has been performed between 170 and 220 GHz based on the measurements of the MPA04-1 MPA. By using the packaged NS under several bias conditions, it is possible to monitor its

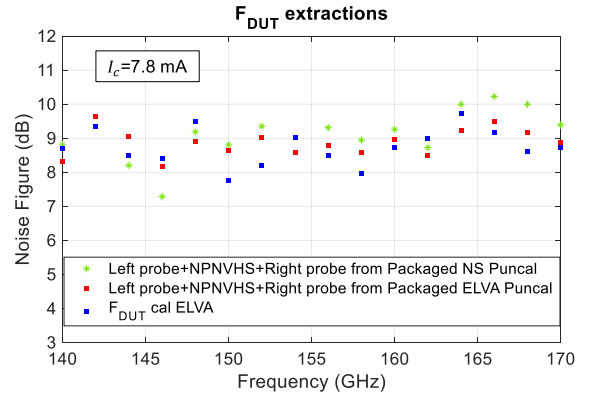


Fig. 28. On-wafer NPNVHS NF extraction results with packaged amplified NS and ELVA NS between 140 and 170 GHz [28].

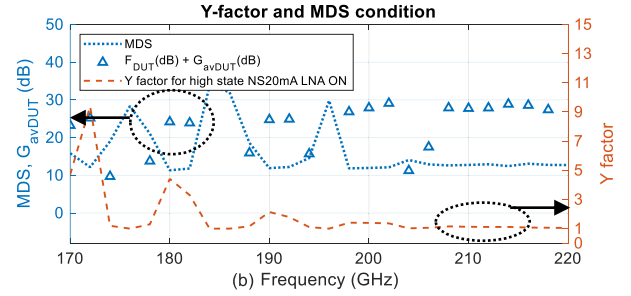
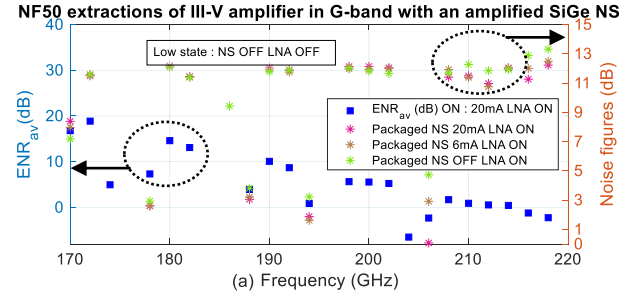


Fig. 29. NF extraction accuracy assessment of MPA04-1 between 170 and 220 GHz. (a) Available ENR and NF values obtained for several biasing conditions. (b) Associated noise measurement validity indicators (MDS condition, Y-factor) [28].

ENR_{av} levels and place the setup at the limit of validation of the MDS condition. The resulting ENR_{av} values are all referred to an unbiased low state and three biased high states. To evaluate the tradeoff between a sufficient ENR_{av} value and the MDS condition with regard to the NF extraction accuracy, MDS condition and ENR_{av} are shown in Fig. 29(a) and (b). As a reminder, the MDS condition can be expressed as in the following, depending on DUT available power gain ($G_{av,DUT}$) and NF (NF_{DUT}) and noise receiver NF (NF_{RCV}):

$$NF_{DUT} + G_{av,DUT} \geq NF_{RCV} + 3 \text{ dB}. \quad (13)$$

The MDS condition validation limit is naturally reached since the ENR_{av} level of the packaged NS decreases beyond 180 GHz due to the two-stages LNA bandwidth, as shown in Fig. 4. The maximum ENR_{av} level is reached in the configuration, where the high state corresponds to a 20-mA biased NS and LNA turned ON. The Y-factor has been plotted in the 170–220-GHz frequency range for this operating mode in Fig. 26(b). It shows decreasing values down to 1, which

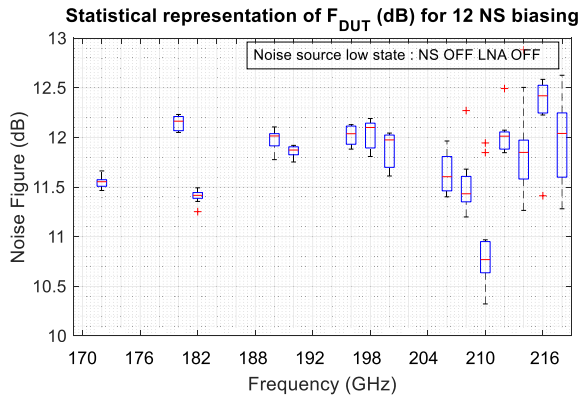


Fig. 30. Statistical representation of MPA04-1 NF extracted values between 170 and 220 GHz for 12 bias states of the packaged amplified NS [28].

means that the difference between noise powers in high and low states of the amplified NS tends to 0. In such condition, the NF extraction accuracy is decreasing, showing discrepancies of more than 2 dB above 200 GHz between the different high states amplified NS biasing. However, the MDS condition is validated in the entire frequency range: the MDS curve refers to the NF_{RCV} increased by a 3-dB margin. Some frequency points show discontinuities in the MDS condition. This is due to the noise receiver input mixer having a gain conversion dropping at specific frequency points. One can infer from Fig. 29(b) that the MDS condition is validated with more than 10-dB margin. It is important to note that at such frequencies, a commercial NS for the purpose of comparison was not available within our measurement platform. Moreover, the DUT considered here is quite favorable to perform an NF extraction since its available power gain is wideband. To the best of our knowledge, it is the first time a III-V amplifier has been characterized with a SiGe packaged NS at these frequencies.

To further investigate the accuracy of NF extraction with the setup comprising the MPA04-1 MPA amplifier, the packaged NS, and the 170–220 GHz noise receiver, a statistical approach to measure NF as a function of the choice of amplified NS high-state biasing was conducted. Since the MDS condition is easily validated even when operating in the low-state operating mode (NS OFF and LNA OFF), this biasing has been chosen as a lower reference for ENR values. Fig. 27 provides the illustration of the impact that the bias state of the NS can have on the dispersion of the NF. Twelve different high states biases were considered, between 0.5 and 20 mA for the p-n diode cathode current and the LNA turned on. The extraction results reveal an NF dispersion better than 0.5 dB at frequencies up to 200 GHz over these various bias conditions. Above this frequency, significant dispersion can be observed, marked by the red crosses in Fig. 30. To the best of our knowledge, it is the first time a statistical approach regarding NF extraction has been conducted in this frequency range.

V. MEASUREMENTS REPEATABILITY ASSESSMENT IN *G*-BAND

This part aims to illustrate the reproducibility work carried out on *S*-parameters and ENR_{av} extractions on several

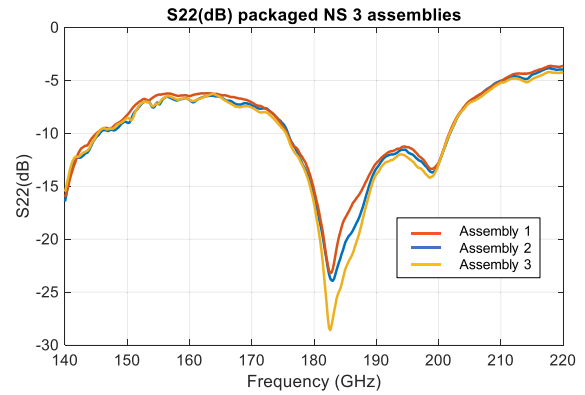


Fig. 31. *S*-parameters repeatability measurements in *G*-band of one sample assembled three consecutive times in the same split-block package [28].

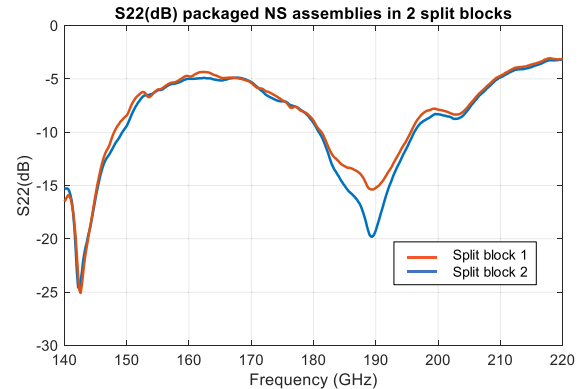


Fig. 32. *S*-parameters repeatability measurements in *G*-band of one sample assembled in two available split-block packages [28].

amplified NS as a function of sensitivity to the package assembly/disassembly steps and for two different split-block units.

A. *S*-Parameters Measurement Repeatability

To place this study beyond the proof-of-concept stage, several repeatability measurements have been performed over multiple assemblies. More specifically, one-port *S*-parameters measurements have been performed on a sample mounted and dismantled three consecutive times in the same split-block package. The results given in Fig. 31 exhibit an excellent reproducibility between several assemblies, which consolidates the packaging approach implemented.

Moreover, the same substrate has been packaged in the two available split-block units to assess the overall manufacturing quality. Results are given in Fig. 32 and show a high degree of repeatability, validating the assembly strategy as well as the robustness of the split-block and organic substrates fabrication scheme.

B. ENR_{av} Measurement Repeatability

An assessment of generated ENR_{av} variability over several assemblies has also been conducted between 140 and 170 GHz. In order to study the impact of multiple packaging steps on ENR_{av} variability, one sample has been mounted and dismantled three times and measured at

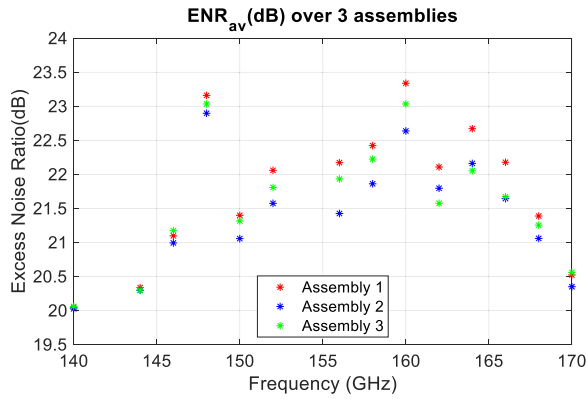


Fig. 33. ENR_{av} repeatability measurements of one sample over three consecutive assemblies in the same package [28].

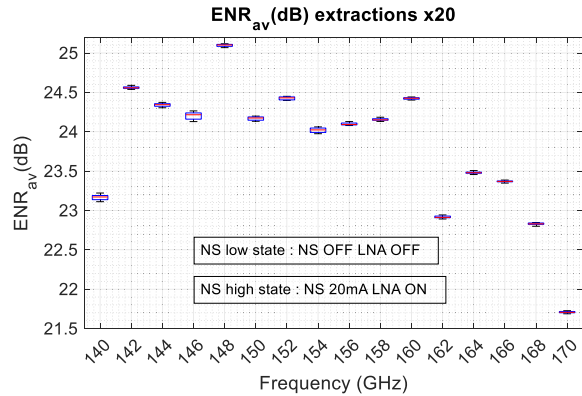


Fig. 34. ENR_{av} repeatability measurements of a packaged NS over 20 consecutive extractions by switching from low (NS OFF/LNA OFF) to high (NS 20 mA/LNA ON) states [28].

each assembly/disassembly stage. Results given in Fig. 33 show a maximum ENR_{av} variability between two assemblies of 0.7 dB.

Moreover, the packaged NS has been used in the low state and high state to extract consecutively 20 ENR_{av} values by directly switching the bias from NS OFF/LNA OFF to NS 20 mA/LNA ON in order to check the robustness of the packaged circuit with respect to bias switchovers and to evaluate the variations of generated noise powers. As shown in Fig. 34, this experiment revealed a maximum change in ENR_{av} of 0.13 dB at a given frequency, confirming the robustness of the packaged NS.

VI. CONCLUSION AND PROSPECTS

For the first time, a packaged NS based on a SiGe BiCMOS 55-nm technology operating between 140 and 220 GHz has been fabricated, packaged, and measured. The chip packaging strategy based on low-cost organic substrates and compatible with multiple assemblies has been detailed. S -parameters and ENR_{av} have been measured in G -band, showing unprecedented levels for a packaged SiGe NS at such frequencies. ENR_{av} up to 24 dB, with the capability of ENR_{av} level monitoring between 140 and 170 GHz, has been demonstrated. One can consider a 14 dB range of ENR_{av} levels at a given frequency between low state (NS OFF LNA ON) and high state (NS 20-mA LNA ON). This NS can generate up to 5 dB of

ENR_{av} at 200 GHz. One of the key aspects of NF extraction accuracy using the Y -factor method is to guarantee a constant NS output matching. This is the case with the developed packaged NS owing to the amplifier stage isolation. This amplification stage brings the distinctive asset of being able to work with a biased low state, ensuring sufficient noise power generation to comply with the MDS condition validation.

This is a differentiating advantage compared to existing commercial NS solutions at these frequencies. To assess NS validity, it has been used for NF measurements of two DUTs. The first one is a WR5-connectorized III–V MPA amplifier from VDI (MPA04-1). NF extractions have been performed concurrently with a commercial ELVA NS to compare and validate extraction with a reference standard. The maximum NF discrepancy observed between the two NSs is 0.3 dB, which proves the quality of the developed packaged NS. In addition, the NF extraction of an on-wafer SiGe BiCMOS 55-nm NPNVHS bipolar transistor has been performed, showing a maximum discrepancy of 0.8 dB between the packaged NS and ELVA NS in the 140–170-GHz frequency range. In another respect, many measurements repeatability regarding S -parameters and ENR_{av} results have been discussed and demonstrate the robustness and quality of the developed packaged NS. The developed package can be kept for a future upgrade that could embed a multi-impedance tuner, offering the possibility of four noise parameters measurements up to 220 GHz for multiple wafer technologies.

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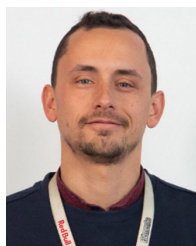
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