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# Analysis of Airgaps for Off-State Capacitance Reduction in SOI-CMOS RF Switches

Daniel Gheysens, Alain Fleury, Stéphane Monfray, Frédéric Giancesello, Philippe Cathelin, David Troadec, Jean François Robillard, *and* Emmanuel Dubois

**Abstract**—This article analyses the introduction of airgaps in the interconnect network of SOI-CMOS based RF switches to significantly reduce the off-state capacitance  $C_{OFF}$  without degrading the on-state resistance  $R_{ON}$ . Based on the 130 nm node of an existing RF-SOI-CMOS technology, an accurate  $C_{OFF}$  evaluation is performed by calculating the respective contributions of the interconnects and the intrinsic transistor separately. The impact of the relative airgap volume is simulated and results in an ultimate  $C_{OFF}$  reduction of 24.6% when the intermetal dielectric is completely replaced by air. It is shown that most of the reduction in  $C_{OFF}$  is achieved by introducing airgap at the first metal level. The airgap approach is verified experimentally by partially eliminating the interconnect dielectric of RF switches in post-process etching steps. A measured  $C_{OFF}$  improvement of 21.7 fF/mm (7.2%) and 18.3 fF/mm (6.3%) is demonstrated for 0.14 and 0.16  $\mu\text{m}$  gate length transistors for which the airgap volume is only partial.

**Index Terms**— RF switches, Airgap, CMOS, SOI, RF, Off-state capacitance, On-state resistance

## I. INTRODUCTION

THE demand for secure, reliable, low-latency, high data rate and massive connectivity is driving the increasingly stringent specifications on the front-end modules of mobile communication systems [1] [2]. As more switches add to the link budget loss, it is of utmost importance that they offer the lowest possible insertion loss in the on-state while keeping the best isolation in the off-state. These two distinctive requirements are reflected in the minimisation of the  $R_{ON} \times C_{OFF}$  time constant which is a well-established figure of merit (FoM) for benchmarking switch technologies. Currently, the partially depleted silicon-on-insulator (PDSOI) CMOS technology is extremely successful in the RF front-end market [3][4]. To further improve the FoM of PDSOI CMOS switches, a difficulty inevitably arises because efforts to reduce  $R_{ON}$  by  $L_G$  downscaling entails an increase of  $C_{OFF}$  by reducing the distance between source/drain terminals. The introduction of airgaps in the interconnection network, also referred to as back-end-of-line (BEOL), allows to partially solve this antagonistic

relationship, thus reducing  $R_{ON}$  without altering  $C_{OFF}$ . Over the last two decades, the introduction of airgaps in interconnects has been widely studied as a solution to overcome the bottleneck of RC delay, power consumption and cross-talk in dense CMOS digital circuits [5]. The literature reports two main approaches for creating airgaps in the BEOL: i) the first one is based on the use of a sacrificial oxide or template of decomposable polymers to define air cavities [6][7][8][9] and ii) the second version involves a non conformal deposition of a dielectric layer over a cavity that pinches and closes at its the top, thus creating a teardrop shaped airgap [10][11][12][13] [14]. More recently, a third approach has been demonstrated using a 2D material, namely h-BN for its exceptional mechanical properties, in order to seal the airgaps which eliminates the need for a sacrificial material [15]. Although the concept of airgaps in BEOL is not new, very few papers have addressed its benefit in the context of RF applications. Following the third integration approach mentioned above, Prawoto *et al.* [16] demonstrated the interest of lateral airgaps embedded only in the ultra-thick topmost metal layer to mitigate the parasitic capacitance associated to integrated inductances, but without providing a significant advantage on the quality factor. Finally, two patents take advantage of airgaps in RF switches by integrating them above the gate of MOS transistors and with a vertical extension only limited to the first dielectric and metal level [17][18]. This article proposes to evaluate new aspects of air-gapped interconnects applied to RF switches that have not yet been addressed in the literature: (i) how  $C_{OFF}$  reduction margin evolves as the airgap extends vertically across the entire BEOL stack, (ii) the feasibility of complete intermetal dielectric (IMD) removal in apertures spanning the deep submicron scale at the first contact level of the transistor to the micrometer range on the uppermost metal layers and (iii) the simulation of  $C_{OFF}$  variations with the airgap volume that captures the 3D complexity of the BEOL layout and the charge dynamics within the transistor. Depending on the RF switch circuit layout and the gate pitch, the relative contribution of the BEOL to the total  $C_{OFF}$  can reach up to 40% [4][19]. To appreciate the potential gain margin, it is easy to understand that replacing the oxide-like ( $\epsilon_r \sim 4$ ) IMD by air ( $\epsilon_r \sim 1$ ) means  $C_{OFF}$  could theoretically be lowered to 70% of the

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D. Gheysens, A. Fleury, S. Monfray, F. Giancesello and P. Cathelin are with STMicroelectronics, 850 rue Jean Monnet 38920 Crolles France (e-mail: daniel.gheysens@externe.junior.com). D. Troadec, J.-F. Robillard and E. Dubois are with Univ. Lille, CNRS, Centrale Lille, Univ. Polytechnique Hauts de France, JUNIA, UMR 8520 -IEMN, F-59000 Lille, France (e-mail: emmanuel.dubois@iemn.fr).

original figure. To confirm the above expectation, this article first proposes a simulation-based accurate calculation of  $C_{OFF}$ . In a second part, we discuss the creation of airgaps in the BEOL of a CMOS PDSOI technology using post-process etching steps. Finally, RF measurement performed on partially hollowed-out switches confirm that  $C_{OFF}$  can be lowered at no extra penalty on  $R_{ON}$ .

## II. TEST STRUCTURE AND SIMULATION MODEL

The considered 200 nm RF SOI-CMOS technology is based on a previous 130 nm technology node [4]. The test structure consists of an array of 25 MOS transistors in parallel with a unitary gate finger width of 10  $\mu\text{m}$  as shown in Fig. 1(a). Several polysilicon gate lengths were considered in the experimental plan ( $L_G=0.14, 0.16, 0.18, 0.22 \mu\text{m}$ ) with two gate pitches of 0.86 and 0.92  $\mu\text{m}$ . This structure is optimized for  $C_{OFF}$  and  $R_{ON}$  extraction in the series and shunt branches of an RF switch [20]. It is worth noting that both the gate and body of the transistor are biased through a 200 k $\Omega$  resistor to accommodate high RF input power, thus mitigating the electric field that the gate dielectric and junctions must experience to prevent breakdown. The gate and body voltage are both set to 3.3 V to extract  $R_{ON}$  in the on-state and -2.5 V to extract  $C_{OFF}$  in the off-state. The total  $C_{OFF}$  capacitance can be partitioned into two components, the first being associated to the interconnection network (BEOL) above the silicon surface while the front-end of the line (FEOL) contribution is related to the intrinsic MOS transistor where the source/drain coupling in the off-state is essentially induced by the source/body and drain/body junctions in series. Due to the highly 3D nature of the interconnection network, the BEOL contribution to  $C_{OFF}$  is well appreciated by solving the Maxwell equations (ADS-Momentum [21]) on a 3D simulation geometry extracted from the circuit layout as illustrated in Fig. 1. Conversely, the intrinsic MOS transistor is well captured by a 2D cross-section as the geometry is invariant along the transistor width. A drift-diffusion simulation code (IMPACT [22]) is therefore used to simulate the small-signal response of the FEOL source/drain two-port system.

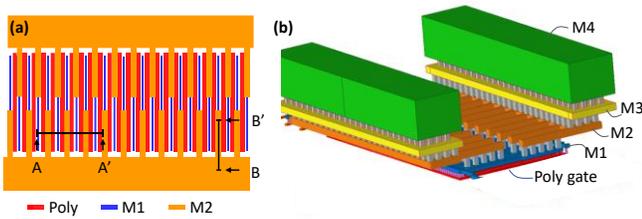


Fig. 1. (a) Layout of the RF switch test structure comprising 25 MOS transistors in parallel (b) 3D view of the BEOL interconnect network showing 4 metal layers M1 to M4.

In both simulation cases,  $C_{OFF}$  is extracted from S-parameters which are converted into Y-parameters used to identify the elements of a  $\pi$ -type lumped equivalent circuit [23]. In a first step, simulations were calibrated for a gate length and pitch of 0.14 and 0.92  $\mu\text{m}$ , respectively. This yields the two components of the off-state capacitance as  $C_{OFF-BEOL}=111.7 \text{ fF/mm}$  and  $C_{OFF-FEOL}=190.1 \text{ fF/mm}$ , the sum of which is 301.8 fF/mm in

excellent agreement with the measurement performed on the initial switch test structure (301.6 fF/mm). In a second step, we have evaluated the impact of a selective removal of the intermetal oxide as the etching front penetrates into the BEOL stack. This front is assumed to be uniform and the dielectric volume above it is replaced by air. Fig. 2 shows the variations of  $C_{OFF}$  as the etching front moves deeper into the BEOL and ultimately reach the contact etch-stop layer (CESL) just above the active silicon layer of the transistor. The sharpest gradient of  $C_{OFF}$  reduction is achieved when the dielectric removal front falls below the first metal level. In the fully hollowed-out configuration, the minimum simulated  $C_{OFF}$  reaches 227.4 fF/mm which represents a significant reduction of 24.6 %. This corresponds to an improvement of the  $R_{ON} \times C_{OFF}$  FoM from 101 fs to 76 fs when airgaps with total IMD removal are implemented.

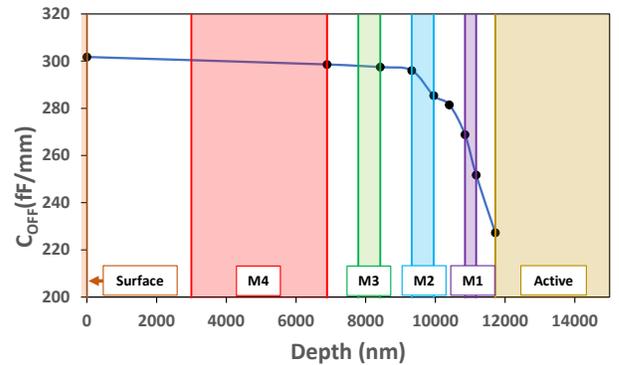


Fig. 2. Simulated off-state capacitance  $C_{OFF}$  as a function of the airgap etching front for gate length and pitch of 0.14 and 0.92  $\mu\text{m}$ , respectively. M1-M4 correspond to the metal interconnect layers.

## III. POST-PROCESS AIRGAP PROCESS

For proof of concept purposes, an etching sequence was developed using 3 focused ion beam (FIB) steps and a final reactive ion etching (RIE) step.

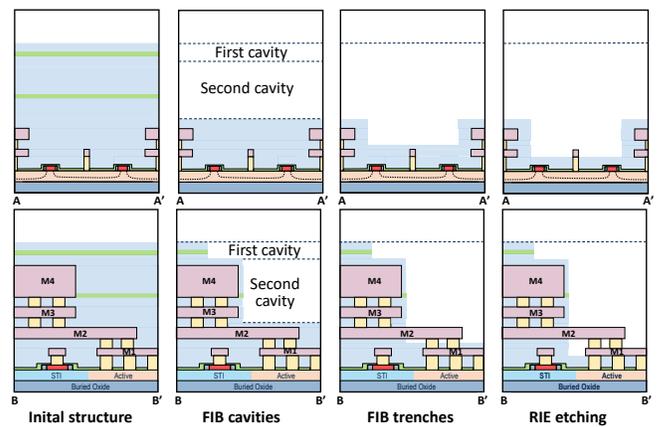


Fig. 3. Airgap etching process step illustrated by schematic cross-sections along A-A' and B-B' directions as outlined in Fig. 1.

The post process steps are detailed in Fig. 3 which presents schematic cross-sections taken along the A-A' and B-B' directions shown in Fig. 1, perpendicular and parallel to the polysilicon gate fingers, respectively. The first two steps consist of FIB etching concentric cavities above the active area of the

switch from which the IMD is removed over  $\sim 9.32 \mu\text{m}$  down to the top level of the M2 metal layer. This 2-step procedure is used to recalibrate the alignment of the second cavity from the M4 metal layer that is uncovered after etching the first cavity. The third FIB step consists in etching rectangular narrow trenches above the gate fingers, i.e., between the M1 lines alternatively connected to the transistor source/drain extensions. The final RIE step is based on  $\text{CF}_4/\text{Ar}$  chemistry to gently remove as much oxide as possible from both sides of the poly gates without altering it. Fig. 4 shows the etching results at different stages and highlights that dielectric removal is achieved imperfectly (Fig. 4(d)) due to the anisotropy of the last RIE step. It is however sufficient to demonstrate the reduction in capacitive coupling by the airgaps as detailed in next section.

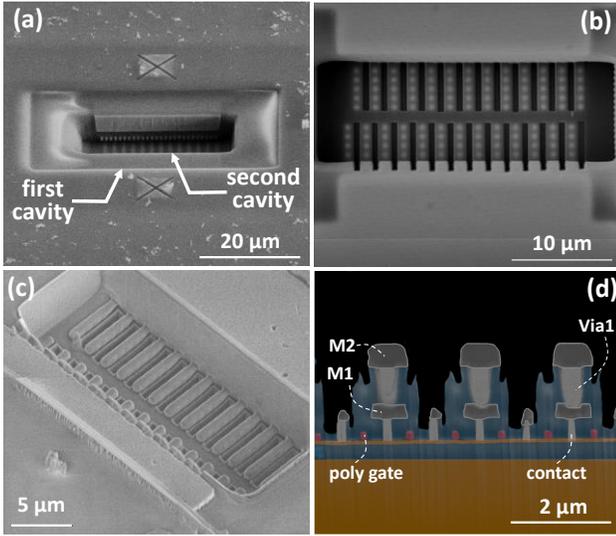


Fig. 4. SEM images at various stages of the airgap etching process: (a) Tilted view of first two FIB cavities. (b) Top view of FIB trenches. (c) Tilted view final structure. (d) Cross section view showing partial dielectric etching after final RIE step.

#### IV. EXPERIMENTAL VALIDATION

S-parameter measurements were first performed on all non-post-processed switches of the above-mentioned experimental plan. The results are reported under markers [A] to [D] in Fig. 5, which summarizes the  $R_{\text{ON}}\text{-}C_{\text{OFF}}$  figure of merit in clouds of data points corresponding to measurements on 4 devices with the same gate length and pitch in order to capture the variability. This figure also includes experimental points labelled [A'] and [B'] on devices subjected to the incomplete BEOL airgap process illustrated in Fig. 4. The obtained  $C_{\text{OFF}}$  are 279.8 and 274.3 fF/mm for  $L_G = 0.14$  and  $0.16 \mu\text{m}$ , respectively, both with a  $0.92 \mu\text{m}$  polysilicon gate pitch. This corresponds to a  $C_{\text{OFF}}$  improvement by 21.7 fF/mm (7.2%) and 18.3 fF/mm (6.3%), respectively. Finally, data points with marker [A''] and [B''] correspond to the best achievable  $C_{\text{OFF}}$  of 227 and 218 fF/mm, respectively, as obtained by simulations when the intermetal oxide is completely removed. Although the experimental  $C_{\text{OFF}}$  reduction observed in [A'] et [B'] do not reach the best achievable simulated figures given by [A''] and [B''], the mitigation of capacitive coupling is significant. Fig. 5 also

shows that airgaps with total IMD removal reduces  $R_{\text{ON}} \times C_{\text{OFF}}$  from 109 fs (marker [A], measured) to 81 fs (marker [A''], simulated) as obtained from simulations. This last figure is very close to the performance of 78 fs recently measured in [19] for a PDSOI technology that has been deeply redesigned at the intrinsic transistor level. It can be anticipated that the application of the same airgap principle on an optimized technology [19] would result in a FoM of 50-53 fs.

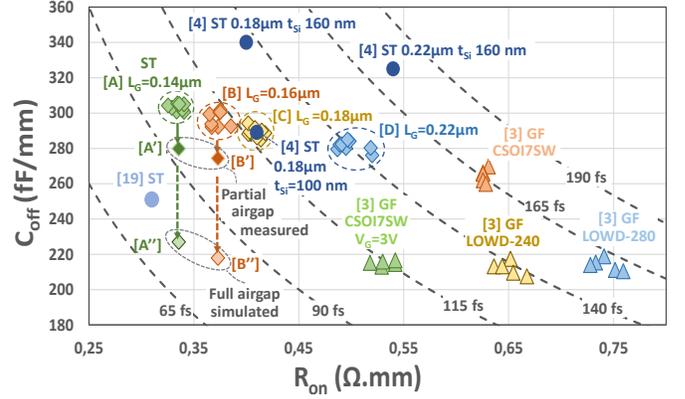


Fig. 5.  $C_{\text{OFF}}$  versus  $R_{\text{ON}}$  showing the impact of experimental partial and full simulated airgaps.

The reduction in capacitance associated with incomplete etching of the airgap corresponding to marker [A'] can be precisely captured by the retro-simulation of the partially etched BEOL structure. As shown in Fig. 6, an effective dielectric permittivity can be assigned to each layer as a function of the remaining oxide surface and the airgap surface introduced, according to the following weighting formula:

$$\epsilon_{eq} = \left( \frac{S_{etched}}{S_{layer}} \right) \cdot \epsilon_{air} + \left( 1 - \frac{S_{etched}}{S_{layer}} \right) \cdot \epsilon_{oxide} \quad (1)$$

where  $S_{etched}$  is the surface of etched dielectric while  $S_{layer}$  is the surface of the initial oxide layer before etching. Table I shows the calculated effective permittivity values associated with the partitioning shown in Fig. 6, which have been fed back into Momentum to assess the impact of partial etching.

TABLE I  
EFFECTIVE DIELECTRIC PERMITTIVITY OF STACK LAYER

Layer	Dielectric permittivity of unprocessed layer	Effective permittivity of partially etched layer
Contact		3.82
Metal 1	4.1	3.56
Via 1		2.89

The corrected  $C_{\text{OFF}}$  value amounts to 274 fF/mm in excellent agreement with the measurement at 279.8 fF/mm. This result demonstrates the consistency of the measurements obtained in the case of an incomplete airgap, and clearly opens up the prospect that the results represented by markers [A''] and [B''] are achievable.

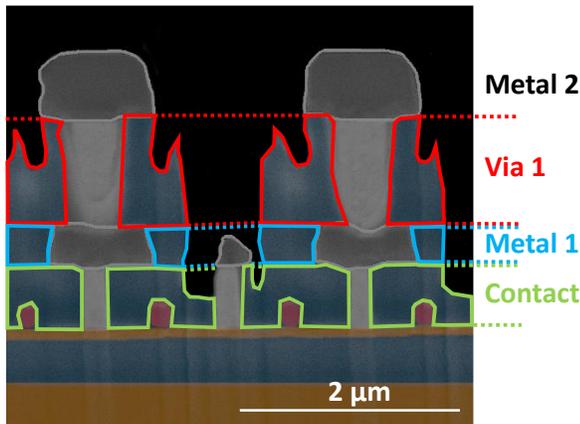


Fig. 6. Cross section obtained by SEM images at the end of the airgap etching process showing partial surface of oxide and air.

Finally, it is interesting to consider the role of fringing capacitances in the  $C_{OFF}$  reduction mechanism. Referring to Fig. 7, the components of fringing capacitances that are potentially affected by the airgaps are the parallel plate and top components,  $C_{pp}$  and  $C_{top}$ , respectively. However, most of the electric field lines starting from the gate are guided laterally into the medium with the highest dielectric constant, i.e., the multilayer spacer and the CESL nitride layer, thus contributing to the side capacitance  $C_{side}$ . The relative weight of  $C_{pp}$  and  $C_{top}$  with respect to  $C_{side}$  remains low for this reason.

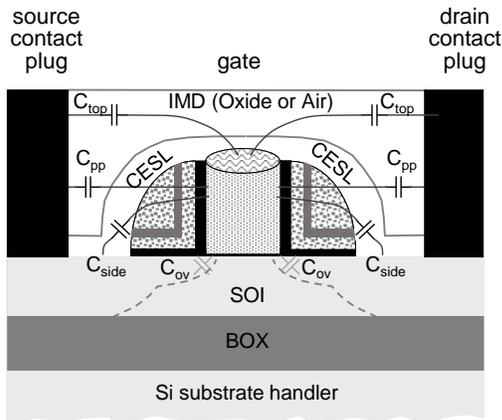


Fig. 7. Schematic representation of a unitary transistor showing the various components of fringing capacitances

In summary, the substitution of the IMD oxide with air leads to a reduction of the  $C_{pp}$  and  $C_{top}$  components and, in turn, the total fringing capacitance. These slight variations of fringing capacitances are expected to have a minor impact on the reduction of  $C_{OFF}$  because the surface of gate electrode involved in the electrostatic coupling effect remains small compared to the surface of electrodes offered between the source and drain contact plugs. The reduction in dielectric permittivity resulting from the introduction of airgaps is therefore considered to be the predominant mechanism for  $C_{OFF}$  reduction. This result is further supported by the retro-simulation results presented

above, based solely on the reduction in capacitive coupling through the introduction of effective dielectric permittivities.

## V. CONCLUSION

In summary, the impact of airgaps extending over the entire interconnection stack of RF switches has been analyzed in detail. A partial validation has been proposed using post process etching steps. The obtained experimental results can be analyzed by realizing that the substantial reduction in  $R_{ON}$  from 0.50 to 0.33  $\Omega \cdot \text{mm}$  obtained by scaling  $L_G$  from 0.22 to 0.14  $\mu\text{m}$  comes at the cost of an increase in  $C_{OFF}$  from 279.0 to 301.6 fF/mm. This penalty is here fully compensated by the airgaps that we introduced using post-process etching of the BEOL, even though complete oxide removal is not achieved. While  $L_G$  downscaling from 0.22 to 0.14  $\mu\text{m}$  results in a significant reduction of  $R_{ON} \times C_{OFF}$  from 141 fs to 101 fs without airgaps, their introduction, as illustrated in Fig.4, further improve this FoM to 94 fs. To demonstrate the full potential of BEOL airgaps for RF switch applications, future work will focus on the introduction of a thin liner on the sidewalls of airgaps as a passivation layer and implementing an isotropic and selective vapor phase etching (e.g. vapor HF) strategy to hollow out the oxide at the M1 level down to the CESL.

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