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## Impacts of low voltage distribution grid resilience constraints on AC/DC converter sizing

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### ABSTRACT

*In a context of increasing DC applications and energy savings, LVDC technologies could be a key technology towards more efficient distribution grids. However, the specific behavior of DC short circuits and the selectivity constraints of existing installations must be taken into account when sizing the converter that interfaces the AC and DC grids. This article details these requirements, proposes a sizing method by electrothermal simulation and highlights the consequences on the converter sizing.*

### INTRODUCTION

Over the past few decades, the development of distributed electricity generation and energy storage systems, as well as the increase in the number of native direct current (DC) consumers, has led to an increasing focus on low voltage direct current (LVDC) distribution grids or at least dedicated DC feeders. Such a grid would allow better interaction between applications [1], but also, and more importantly, greater efficiency. First, because the resistance of a DC cable could be lower than that of an AC cable. Second, the current absence of standards could allow for voltages up to 1500 V, resulting in lower transmission losses [2]. Finally, a DC distribution system would centralize and standardize the AC/DC conversion step, which is currently performed by each user. Due to the large number of transformer substations, the use of an electronic transformer would not be relevant, due to its cost, size, and high losses. In this context, the preferred solution is to keep the existing LVAC transformer and to implement a centralized AC/DC converter on its secondary on a limited number of feeders [3].

Despite a large number of commercially available converters, electrical safety remains an obstacle to the deployment of these solutions. This is because the behavior of a DC short circuit is very different from that of an AC short circuit, due to the presence of capacitors on the DC link. In the event of a fault, these capacitors discharge almost instantaneously, before the grid current flows through the converter [4]. The absence of zero-crossing of the current requires the generation of an opposite voltage to force the decrease of the DC current

and interrupt the fault [5], which slows down traditional protections. Combined with the limited overcurrent capabilities of semiconductor components, these factors have encouraged manufacturers to look for fast protective devices. Many different proposals can be found in the literature, such as hybrid or electronic circuit breakers [6], which can achieve response times of 2 to 0.1 ms. Another solution is to use fuses, already used in distribution grids, which are cheaper but offer unpredictable response time [7]-[9].

However, fast protection is not sufficient in the case of a DC distribution grid. In fact, to ensure the selectivity of the protection, the grid operator requires that the protection closest to the fault reacts first. Therefore, the further away a protection is from a consumer, the later the interruption should be. In the absence of national or international standards, this constraint is mostly omitted by manufacturers. AC/DC converters may then have a time to reach the maximal thermal stress that is lower than the maximum protection cut-off time (Figure 1). To ensure a safe operation, the maximum cut-off time must be lower than the maximum module thermal stress time for the whole fault current range.

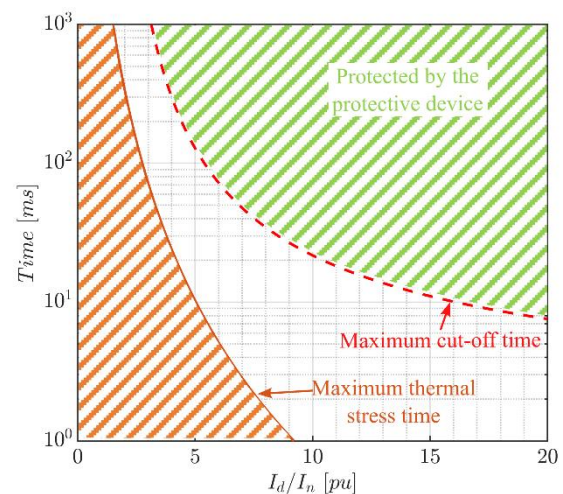


Figure 1 : Example of protection not coordinated with the admissible module thermal stress of the converter.

This paper proposes to address this issue by presenting a

method for sizing 2-level voltage source converters (VSC), taking into account the operating constraints of the distribution grid. Firstly, these constraints are detailed. Then the sizing method is presented. Finally, the results are discussed.

## CONSTRAINTS AND ASSUMPTIONS

### Grid requirement

Table 1: Harmonic current constraints in relation to the magnitude of the fundamental current at rated power

Harmonics	Odd	Even
$h < 11$	4 %	1 %
$11 \leq h < 17$	2 %	0.5 %
$17 \leq h < 23$	1.5 %	0.375 %
$23 \leq h < 35$	0.6 %	0.15 %
$35 \leq h$	0.3 %	0.075 %

There are 3 constraints for the grid-connection of a power electronic converter: power quality, efficiency, and selectivity.

The *power quality* on the DC side of a converter is still debated in the literature. The only consensus parameter is the voltage ripple, but its exact value is still undefined. Similarly to the accepted voltage deviation on the LVAC grid [10], we select a ripple whose peak-to-peak value is less than 5% of the nominal DC voltage. For the AC side, an overall harmonic content  $THD_i \leq 8\%$  at rated power, with the constraints per current harmonic specified in Table 1, is recommended [11].

An *efficiency*  $\eta_{min}$  of at least 97 % is required [3], including semiconductors and passive components. This efficiency should be bi-directional and calculated for 100 %, 75 %, 50 % and 25 % of the rated power.

For *selectivity*, existing fuses in electrical substations have a response time of a few seconds to hundreds of milliseconds [6] which is too slow for their use with power electronics. Therefore, we assume here that a dedicated protection device is implemented, with a maximum cut-off time given by,

$$t_{trip,max} = e^{15.38 \left(\frac{I_d}{I_n} - 1\right)^{-0.5309}} \quad (1)$$

where  $I_d$  [A] is the estimated fault current in steady state and  $I_n$  [A] the nominal current. Due to the specific behavior of a VSC during a short circuit [4], [12], the steady state fault current is almost perfectly sinusoidal. Its RMS value  $I_d$  can be estimated by,

$$I_d = \frac{V}{\sqrt{\left(\frac{2}{3}(2r_{DC}l_{fault} + R_d) + R_L\right)^2 + \left(\frac{4}{3}x_{DC}l_{fault} + X\right)^2}} \quad (2)$$

where  $V$  is the phase to neutral RMS voltage,  $r_{DC}$  is the cable resistance per unit length,  $l_{fault}$  is the fault distance from the feeder,  $R_d$  is the fault resistance,  $R_L$  is the tie reactor resistance,  $x_{DC}$  is the cable reactance per unit length, and  $X$  is the tie reactor reactance.

Table 2: LVAC and LVDC grid parameters

Transformer	
Primary voltage	20 kV L-L RMS
Secondary voltage	400 V L-L RMS
Short-circuit voltage	4 %
DC Cable [22]	
Resistance per unit length $r_{DC}$	0.124 $\Omega$ /km
Reactance per unit length $x_{DC}$	0.071 $\Omega$ /km
Length	600 m
Fault	
Location $l_{fault}$	0 – 600 m
Starting time $t_{fault}$	0 – 20 ms

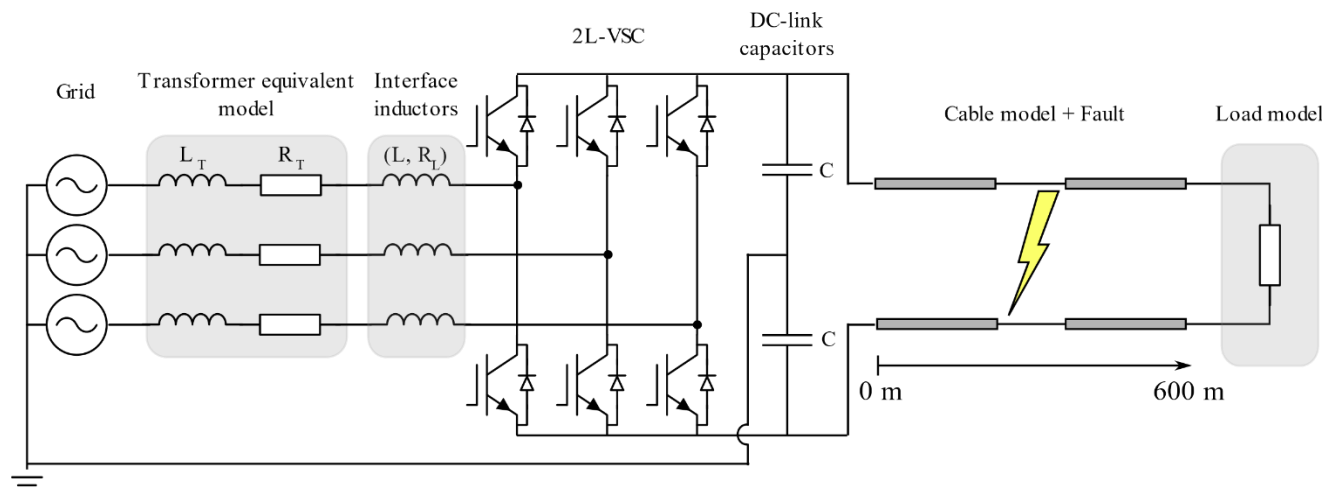


Figure 2 : Circuit under study: grid, step-down transformer of the substation, 2-level voltage source converter with its tie reactor and DC-link capacitors and the DC grid.

<b>Impedance</b>	1 mΩ
<b>Resistive Load</b>	
<b>Power</b>	20 kW

### Grid definition

The parameters of the studied distribution grid are summarized in Table 2. It is assumed that existing LVAC cables are reused [13] with a TN-S configuration for the LVDC grid. The DC-link mid-point is grounded at the same point as the star coupled transformer, due to space limitations in a substation.

### Converter definition

Because of its low number of semiconductors and simplicity, a two-level converter (2L-VSC) is considered. It is interfaced to the LVAC grid with a tie reactor, as illustrated in Figure 2. The DC-link capacitors consist of two capacitors in series.

## SIZING METHODOLOGY

The following paragraphs detail the different steps of the converter sizing process.

### Module selection

Due to the large number of available products, we focus on fully integrated 2L-VSCs, also referred to as “sixpack” which are cheaper for the same function.

For each reference, we extract the module cost and its datasheet parameters: diode and IGBT switching losses and conduction losses, junction thermal model, diode voltage threshold, diode conduction resistance, diode thermal stress  $i^2 t_{max}$  and maximum steady-state junction temperature  $T_{j,max}$ . The commutation losses depend on the driver gate resistance. For modules under 150 A, there is usually no integrated driver. In that case, the gate resistance is assumed to be equal to 10 Ω. For modules over 150 A, we use the resistance value of the integrated driver. The selection of the switching frequency is left to the user’s discretion but must stay within the range of the driver and module capabilities.

### Capacitor selection

The pole-to-pole short circuit is the most critical fault for a LVDC grid: it results in a sharp increase in current and a drop in DC voltage. However, the voltage can become negative [4], [7] and damage electrolytic capacitors, which can only accept a voltage reversal of 1 to 1.5 V [14]. To overcome this issue, film capacitors should be used. The capacitors are chosen from the C44U 900 V series. For each reference, the capacitance and equivalent series resistance (ESR) are extracted.

### Inductance selection

With large fault currents, the magnetic core of the coil could saturate, decreasing its inductance. This behavior leads to a further increase in the fault current from the grid,

as illustrated by equation (2). To avoid this, air-core coils are used.

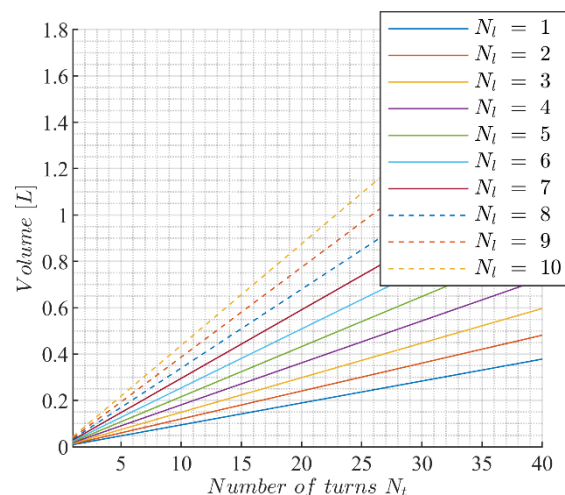
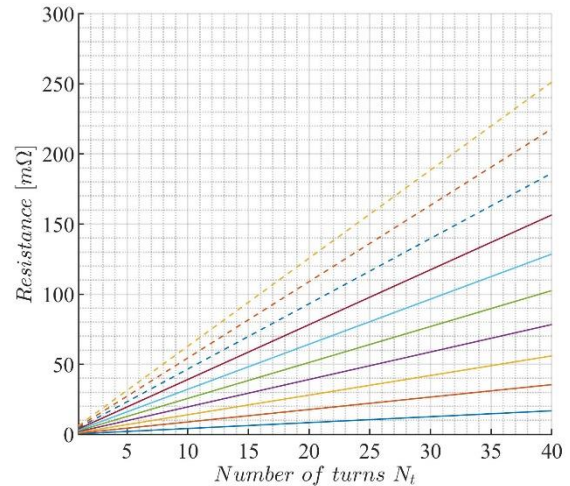
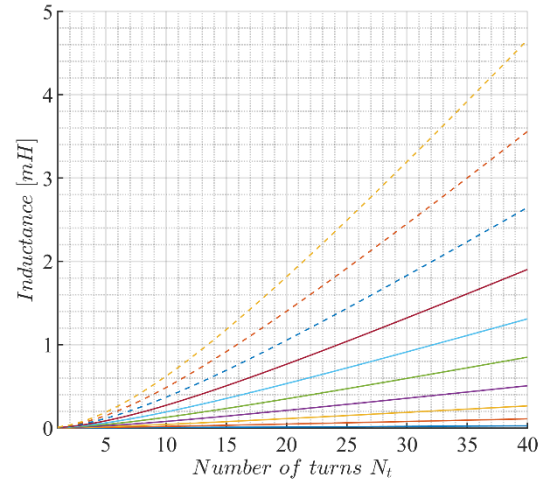


Figure 3: Evolution of inductance, resistance and volume of a circular air core coil according to the number of turns and layers, assuming the use of a AWG 7 wire and an internal diameter of 50 mm.

We consider a circular dry-type air-core copper coil. To

choose the wire diameter, a first estimation can be made based on the steady-state current. Based on the American Wire Gauge (AWG) recommendations, a wire of 3.6 mm [16], accepting 30 A RMS, should be chosen to avoid overheating at the rated current. This conductor, and in particular its insulation, must also be able to withstand transient short circuit currents. To validate the selection of the conductor, the empirical equation (3) must be validated [17].

$$I_d \leq A \sqrt{\frac{0.0297}{\Delta t} \log\left(\frac{T_2 + 234}{T_1 + 234}\right)} \quad (3)$$

where  $T_1$  [°C] is the initial temperature of the wire,  $T_2$  [°C] is the maximal temperature acceptable by the insulation,  $\Delta t$  [s] is the duration of the fault and  $A$  [m<sup>2</sup>] is the section of the wire. These parameters are set to 70 °C, 150 °C, 1 s and 10 mm<sup>2</sup>, respectively. The maximal temperature is due to the use of varnished conductors [17]. By defining the number of turns  $N_t$ , the number of layers  $N_l$ , the internal diameter of the coil  $D_{int}$  and the wire diameter  $d_w$ , we calculate its parameters using the equations of [15]: inductance  $L$ , resistance  $R_L$  and volume. The Figure 3 shows the result of this sizing process, considering an internal diameter of 50 mm. For a given inductance value, the duplet  $(N_t, N_l)$  that minimizes the volume is selected chosen.

Such air-core inductors are usually custom-made, so there is no cost data available. Based on our experience, we assume that the cost  $C_L$  is expressed as,

$$C_L = 4.22 X_L I_n^2 \quad (4)$$

where  $X_L$  [Ω] is the inductor reactance at 50 Hz and  $I_n$  [A] is the inductor nominal current.

### Validation

To validate the chosen sizing according to the above constraints, two PLECS simulation sequences are performed. The first one simulates the steady state operation of the converter. It aims to validate the power quality and efficiency criteria. Note that we consider open-loop operation to speed up the computing time, while considering that closed-loop could further improve the performance. The temperature of each diode and each IGBT is monitored and must remain below  $0.8T_{j,max}$ .

The second sequence simulates the transient operation of the converter feeding a DC load, during a pole-to-pole short circuit. It aims to validate the selectivity criterion. For each diode, the thermal stress  $i_D^2 t$  is calculated for different fault locations and starting times, and compared to its datasheet value  $i_D^2 t_{max}$ . The sizing is deemed correct when,

$$\int_0^{t_{trip,max}} i_D(t, l_{fault}, t_{fault})^2 dt \leq i_D^2 t_{max} \quad (5)$$

## RESULTS & DISCUSSION

Using the methodology described above, a first sizing of the converter is carried out. First considering only the

power quality and efficiency criteria. The resulting sizing #A is summarized in the first column of Table 2. Then considering the selectivity criterion too. The resulting sizing #B is summarized in the second column of Table 2.

For the sizing #A, a module having a nominal current of  $1.7I_n$  is necessary in order to respect the efficiency criteria. Note that the tie reactor can handle large currents (Eq. (3) is satisfied) but the modules cannot (Eq. (5) is not satisfied). Therefore, the tie reactor is oversized. An iron-core tie reactor could be used instead, which could result in an even less expensive alternative [18].

For the sizing #B, in order to meet the selectivity criteria, it is necessary to select the module having the largest nominal current, corresponding to  $15I_n$ . This represents an 800% increase compared to #A, resulting in a ~700% increase in the module cost. However, this modification is not sufficient to meet the selectivity criterion. This is illustrated in Figure 4: for an inductance of 1.56 mH, even for a 450 A module, the maximum thermal stress time can be smaller than the protection cut-off time when the fault is located near the feeder. To meet the selectivity criterion, one needs to increase the inductance to 2.08 mH. This modification results in higher losses which are nevertheless compensated by a reduction of the switching frequency. At the end, the selectivity constraint results in a 66% increase in the total cost of the converter.

Table 3: Summary of the sizings of 2L-VSC for LVDC grids

	#A	#B	#C
<b>Power quality</b>	✓	✓	✓
<b>Efficiency</b>	✓	✓	✓
<b>Selectivity</b>	✗	✓	✓
<b>Topology</b>	Sixpack	Sixpack	Dual
<b>Module</b>	FS50R12K T3G	FS450R12 OE4	IFF600B12 ME4P
<b><math>I_n</math> [A]</b>	50	450	600
<b><math>C_{module}</math> [€]</b>	117	803	3×388
<b><math>f_{sw}</math> [kHz]</b>	12	8	11
<b>THD<sub>i</sub> [%]</b>	7.04	5.16	7.8
<b><math>\eta_{min}</math> [%]</b>	97.06	97.1	97.06
<b>Capacitor</b>	C44UOGT7450M34K		
<b><math>L</math> [mH]</b>	1.56	2.08	1.56
<b><math>R_L</math> [mΩ]</b>	78	95	78
<b><math>C_L</math> [€]</b>	1861	2481	1861
<b><math>C_{tot}</math> [€]</b>	1978	3284	3025

In order to keep the sizing #A inductance value, while meeting the selectivity criteria, it is necessary to use “dual” modules, i.e., modules containing only one arm of the converter. In contrast to the “sixpack” topologies, these modules have a higher current rating (up to 900 A) and use newer semiconductor technologies. The resulting sizing #C is summarized in the third column of Table 2. This

results in an increase of 45% in the cost of the modules compared to the sizing #B. Compared to sizing #B and #A, the total cost is decreased by 8 % and augmented by 35 % respectively.

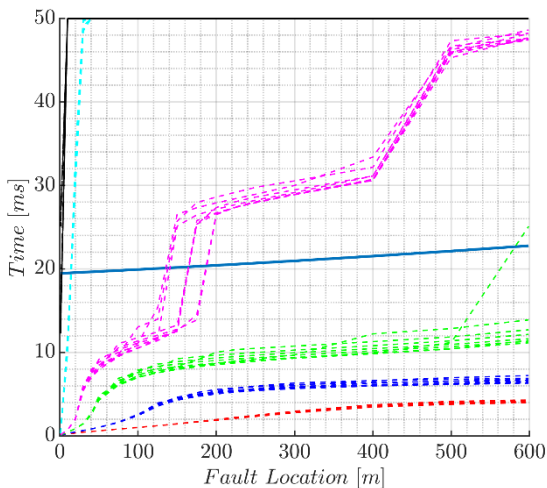


Figure 4 : Simulation results for 2L-VSC with a 1.56 mH tie reactor. Maximum module thermal stress time as a function of the fault location, for different starting times. The dotted lines correspond to modules of 50 A (red), 100 A (blue), 150 A (green), 200 A (magenta), 300 A (cyan) and 450 A module (black). The continuous line represents the maximum protection cut-off time.

## CONCLUSION

This paper highlights the need to take into account the grid constraints, especially selectivity, when sizing interface converters for LVDC grids. First, because of the DC short-circuit behavior, it is required to use specific passive components, such as film capacitors and air-core inductors. Then, because the thermal stresses are severe, the converter must be strongly oversized (at least 15 times the nominal current for the modules). These results may prompt converter manufacturers to increase the thermal stress of their module or to propose new resilient topologies.

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