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A Very Low Power 12 bit 64-MS/s 2 step SAR Assisted Bidirectional Digital Slope ADC

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Abstract— This paper presents a novel architecture of a SAR assisted 2 step ADC where the SAR residue is quantized with a bidirectional digital slope time-based converter. The bidirectional slope halves the conversion time of the second stage. Furthermore, the redundancy requirements in the second stage are considerably reduced through a unified global calibration scheme. A practical example is given for a 12-bit 64 MS/s ADC with 67 dB SNDR and 208 μ W estimated power consumption targeted at ultra-low power RF receivers. The complete architecture including calibration has been validated with VerilogA models including capacitor mismatch, comparator offsets and noise.

Keywords—Analog to Digital Converter (ADC) – Successive approximation register (SAR) – Digital slope – SAR assisted ADC – Offset cancellation.

I. INTRODUCTION

The Successive Approximation Register (SAR) ADC has become the dominant architecture in the state of the art for low power applications with several MHz bandwidth and mid resolutions ($8 \sim 10$ bits) [1][2]. They are particularly well adapted to RF receiver circuits where the ADC performance is a major contributor to the overall performance. High resolution and wide bandwidth ADCs relax constraints on other blocs in the Rx chain [1].

Power consumption in SAR ADCSs at low supply voltages and high resolution is dominated by the comparator [3] because of low noise requirements. 2-stage pipelined SAR ADCs with an interstage residue amplifier [4]-[5] can relax these requirements. However, the interstage amplifier becomes critical because of gain and noise constraints.

Alternative architectures of SAR-assisted 2-stage ADCs without the need for a residue amplifier have been proposed. M. Zang et al. proposed in [6] a Voltage-to-time converter (VTC) that transforms the SAR conversion residue in a time window which is then discretized by a delay line-based timeto-digital converter. The voltage-to-time conversion is achieved by discharging the node holding the residue with a constant current. The VTC is fundamentally linear, and the resolution is only limited by the various noise sources. However, precise matching between then VTC and Time to digital converter (TDC) time constants is needed in such an approach. Conceptually similar architectures [7]-[8] propose to use a delay-line driven digital slope (DS) with 1-LSB steps as second stage, combining the discharge of the residue and the time-to-digital conversion into a single operation. The state of the delay-line at zero crossing of the digital slope represents the output code in thermometric representation. The resolution of this approach is limited by the discretized



Figure 1 - SAR-Assisted Two stages differential DS

voltage steps of the digital slope. Both implementations apply the digital slope on the positive branch only of the differential circuit in monotonic switching, requiring to first level shift the SAR residue to the positive domain. Limiting the bandwidth of the comparator has the effect of time interpolation between consecutive steps which can increase the achievable resolution by up to 3 bits [8].

This paper presents a 2 step SAR Assisted ADC with a pseudo-differential approach allowing a bidirectional digital slope. It also proposes a unified calibration scheme for comparator offsets and the digital-slope delay. Key advantages of the proposed architecture are a reduced number of capacitors, minimized cross-point voltage variations and reduced conversion time. Target specifications for the ADC architecture have been derived from the needs of a low power receiver aimed at connectivity applications such as Bluetooth., i.e. a 12 bit 64 MS/s ADC with 68 dB SNR. These specifications are used for dimensioning a reference implementation of the proposed architecture.

II. SAR-ASSISTED DIGITAL SLOPE ARCHITECTURE

Figure 1 shows a block diagram of the proposed architecture. The first stage is a 9-bit CDAC based SAR ADC with an additional bit because of built-in redundancy. The residue voltage of the SAR ADC is further quantized by a digital slope time-domain ADC. An inverter-based delay line connected to an array of unit capacitors generates the digital slope. The latched comparator (D-CMP) for the SAR and the continuous time comparator (CT-CMP) of the time-domain ADC share the same input signal. However, they are only active during respective conversion operations. The remaining part of the CDAC (CDAC_{Calib}) is binary weighted and used for foreground calibration of the comparators.



Figure 2 - CDAC Implementation for differential DS with redundancy & calibration

Figure 2 shows a detailed diagram of the global CDAC. C denotes the unit capacitor of the array. Top plate sampling combined with a split monotonic switching scheme is used in the presented architecture. The common-mode signal on the $Vx_n \& Vx_p$ internal nodes is set by the input signal to half the supply voltage. Capacitors appear as pairs with bottom electrodes connected respectively to V_{refN} and V_{refP} . In this architecture no common-mode reference is needed so parasitic sources are reduced [8]-[9].

The 9-bit SAR ADC has 8+1 switched capacitor pairs on both positive and negative branches. The MSB capacitor is only 480 * C, and an additional 32 * C capacitor is added to the array. This introduces redundancy allowing correction of errors occurring over the first 5 steps of the conversion.

At the end of the SAR conversion, the residue equal to the difference between the input sample and the value represented by the 8 most significant SAR bits remains in the CDAC. The 9th bit of the SAR indicates the sign of the residue voltage. The second stage then discharges the remaining differential voltage V_{Xp} - V_{Xn} with a bidirectional digital slope generated by 6 pairs of unit-capacitors. An inverter-base delay line generates the control signals, and the CT-CMP latches the state of the delay line when the zero-crossing



Figure 3 -Operation of a monotonic 2nd stage digital slope

is detected. The state of the delay line at zero-crossing represents the quantized value of the residue in a thermometric binary representation.

 $CDAC_{Calib}$ adds an appropriate voltage during SAR and continuous time conversion to the internal differential node to compensate respectively the offset of the discrete-time and continuous-time comparator. The value of the correction for each comparator is determined in a foreground calibration phase described in section III.

The total capacitance in each branch is theoretically equal to 2048*C. The digital slope adds 4 additional unit capacitors, while the calibration CDAC adds a total of 32 unit capacitors. This does not impair the performance other than reducing the LSB voltage step and full-scale input voltage by 1,5% with respect to the theoretical value.

III. PSEUDO-DIFFERENTIAL DIGITAL SLOPE STAGE

A. Unidirectional Digital Slope

SAR-Assisted digital slope ADCs in prior art use a monotonic switching scheme on a single branch, the other branch remaining at a fixed voltage [7]-[8]. Consequently, the discharging operation is always in the same direction. Assuming a negative direction, the initial residue voltage must be positive to reach the zero-crossing. A sufficiently large positive offset is therefore added to the residue voltage prior to the conversion to meet this requirement regardless of the actual sign of the residue voltage. Figure 3 represents the dynamic of residue at the end of the SAR conversion, which is equal to twice the LSB voltage of the SAR. In practice an additional margin is needed to consider errors induced by various sources during the SAR conversion. Under the assumption that an additional bit is needed for redundancy, the range to be quantified can be as large as 4 times the SAR LSB voltage. To produce 3 additional bits with the continuous time digital slope ADC, 5 bits are needed for the continuous time ADC.

The advantage of the monotonic one-sided slope is the robustness and simplicity of implementation. However, the sign-bit of the SAR is not used and the conversion time is higher than theoretically necessary. Finally, the voltage corresponding to the zero-crossing depends on the residue voltage on the opposite node and is signal dependant. This could potentially cause non-linear distorsion.



Figure 4 - Operation of a bidirectional 2nd stage digital slope (a) for positive residue - (b) for negative residue

B. Pseudo-differential bidirectional digital slope

The proposed pseudo differential bidirectional Digital Slope consists in switching alternatively capacitors on the positive and negative branches. Alternate switching of the unit capacitors on both positive and negative branches increases the step resolution by 1 bit (C instead of 2C changing state at a given time) and keeps the common-mode voltage at zero-crossing within a 1 CT-ADC LSB window. Furthermore, slopes in the positive or negative direction can easily be created thanks to the split switching scheme adopted in this CDAC architecture. This allows conversion of positive or negative residue voltages with the sign bit of the SAR ADC determining the direction which halves the range that needs to be covered by the digital slope. A small level shift voltage is however still required to correct any residual offset and noise errors of the SAR comparator. Figure 4 presents examples of the proposed approach for residues of positive and negative signs. As shown, a small level shift is first applied for redundancy purposes only. Fig. 5 shows the proposed implementation of the 3 bits pseudo differential DS. The capacitor array is composed of 6 capacitors pairs on each



Figure 5 - 2nd stage: 3 bits Digital Slope implementation



Figure 6 - 3 bits Pseudo differential Digital Slope with redundancy a) for positive residue – (b) for negative residue

side. When sampling the input signal, half of the Figure 6 shows the detailed switching scheme for positive and negative slopes with examples of negative and positive residues. For negative residues, first capacitors C1, C2, C13 and C14 are switched simultaneously to create a 4 LSB offset. Then the conversion starts on the rising edge of T_{st} and C12 to C7 on positive side and C24 to C19 on negative side are alternatively switched to generate the digital slope creating 12 LSB steps. The final 4 LSB steps are created by switching C2, C14, C1 and C13 successively to their original state. The zero-crossing point depends on the value of the residue, but it always occurs within a $\pm 0.5 LSB$ window around the common mode voltage. Operation for positive residues is similar, but slopes are inverted. The detailed logic function to control capacitors generation the level shifts can be seen on Figure 5. The remaining capacitors are directly switched by the appropriate outputs of the delay line.

This pseudo differential implementation speeds up the overall conversion while reducing the number of capacitances used for redundancy. Bidirectional slopes are generated without reducing the size of unit capacitors. Furthermore, the common mode variation [9]-[10] for the comparator switching point is limited to one LSB voltage step.

C. Foreground calibration

Capacitor mismatch, incomplete settling and comparator offset and noise are the major impairments limiting the performance of the SAR ADC. Redundancy in the second stage can correct these impairments. The remaining critical parameters are the noise and offset of the continuous-time comparator. Foreground calibration allows to reduce the impact of the comparator offset. The foreground calibration has been extended to the discrete-time comparator of the SAR to relax the redundancy requirements of the second stage. A common way to correct the comparator offset is to add calibration circuitry into the pre-amplifier of the comparator [8]-[11]. We propose an alternative approach by extending the CDAC for calibration purposes. It allows to independently calibrate both comparators and to implement the calibration algorithm on-chip. The CDAC_{Calib} part of the CDAC is dimensioned in powers of 2 (Figure 2). In the foreground phase the offset of each comparator is determined

by a successive approximation algorithm. Averaging is used to filter out the comparator noise contribution over multiple measurements. In the normal mode, the respective corrections are applied when using the SAR and DS mode.

In foreground phase, the comparator delay is also calibrated once offset compensation is applied. By applying a zero differential input voltage to the 2^{nd} stage the corresponding output represents the delay with a $\pm 0.5 \tau$ accuracy. By extending the delay line with a few extra unit delay cells (not represented in Figure 5) the comparator's delay can be perfectly compensated [7]. By this unified calibration scheme the nonidealities of the critical blocks could be self-corrected with sufficient precision without extra circuitry nor consumption.

D. Redundancy sizing

The conversion time and consequently the power consumption of the 2nd stage is proportional to its input range. The input range of the second stage has been extended by 50% with respect to the maximum theoretical residue of the first stage. This introduces redundancy in the second stage allowing error correction in a range of $\pm 4 LSB$ [12]. As shown in III.C the offset is calibrated within a $\pm 0.5 LSB$ range so D-CMP noise is the major error source. With $\pm 4 LSB$ of redundancy between stages and 430 µV CT-ADC LSB and 5 σ margin, input-referred noise (IRN) of the D-CMP needs be less than $300\mu V_{RMS}$.



Figure 7 - Simulated 8192 points FFT of the proposed ADC with noise, offset and mismatch models

IV. ADC DIMENSIONING AND SIMULATION RESULTS

The proposed ADC has been scaled to the needs of a low power RF receiver with 12 bits resolution, 64MS/s sampling rate and 68dB SNR. The target process is 28nm CMOS with 0.9V power supply. The sampling noise budget has been set equal to the quantization noise to keep low power consumption and area. The resulting C_{sample} is equal to 0.615pF with units capacitors of $C_{\mu} = 0.3fF$. The remaining major noise contributor is the CT-CMP. To reach the noise requirement of 68 dB SNR its noise specifications is an IRN $< 157.7 \mu V_{RMS}$. In the simulation an IRN of $157 \mu V_{RMS}$ has been used. To reduce the impact of capacitor's mismatch the 3 MSB capacitors (480C, 256C & 128C) are thermometrically split in groups of 128C. Mismatch is simulated with an overestimated value of $\frac{\delta_u}{c_u} = 1.25\%$ compared to technology performances. Simulations with VerilogA models validate the concept of the architecture, the performance of the self-calibrated scheme and the impact of the major noise contributors. Figure 7 presents the simulated FFT of the architecture including mismatch and noise contributions. DC offsets are put on both comparators and corrected by the foreground calibration phase. The unit delay of 2^{nd} stage is 50ps. The simulated SNDR reaches 67.15dB.

Table 1 compares the simulated performances of the proposed architecture with references of the state of the art. By extrapolation from measurements of a similar architecture implemented in 28nm CMOS [7] the power consumption of the different blocs has been estimated. The proposed 2nd stage resolution is 3 bits versus 5 bits in [7] with identical unit delays. The conversion time is reduced by a factor 4, resulting in 4 times lower power consumption. Our estimate includes a 30% margin, so the 2nd stage power consumption is estimated as one third of the power consumption reported in [7]. Conversely the proposed SAR has 2 additional steps compared to [7], increasing the SAR power consumption by 25%. For an identical sampling rate of 100MS/s, the estimated power consumption would be 318.75 µW. The power consumption also scales with the sampling rate leading to a final estimate of 204µW power consumption. This leads to a FOM_{schreier} of 179.1 dB considering an SNDR of 67.12 dB. This places the proposed architecture in a favorable position compared to other digital slope implementations. There still is a margin with continuous slope implementations [6]. However continuous slope implementations suffer from high PVT sensitivity and longer conversion time.

Table 1
Performance Summary and Comparison with the State-of-the-Art

	This Work	[6]	[7]	[8]
Resolution [bits]	12	13	12	12
Sample rate [MS/s]	64	20	100	260
SNDR [dB]	67.12*	71.5 [‡]	65.67 [‡]	63.48 [‡]
Csample [pF]	0.615	4	0.9	1.2
Noise CT-CMP [µV _{RMS}]	157	45.6	150	
Consumption [µW]	204**	82 [†]	350 *	970 [‡]
2 nd stage common mode variation	± 0.5 LSB		$\geq -64LSB$	$\geq -64LSB$
FOM _{Schreier} [dB]	179.1**	182.4 [‡]	177.2 [‡]	171.8 [‡]

Heasured from silicon
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* Simulated on VerilogA modelisation with noise, offset and mismatch ** Extrapolated from [7] measurements

V. CONCLUSION

This paper proposes a novel approach to implement a bidirectional digital slope time-based converter resulting in faster conversion time and lower power consumption. The concept has been modeled in a 2 step SAR assisted ADC architecture, targeted on 12 bits resolution and sample rate of 64MS/s. The VerilogA model includes careful estimations of error sources and predicts an SNDR of 67.12 dB. Based on measured data from [7] power consumption is estimated at 204μ W yielding to FOM_S of 179.1 dB which compares favorably to the state of the art.

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