From dissolution to controlled macrostepping of 4H-SiC during liquid Si-induced structuring in a sandwich configuration

Yann Jousseaume, François Cauwet, Bruno Gardiola, Gabriel Ferro

From dissolution to controlled macrostepping of 4H-SiC during liquid Si-induced structuring in a sandwich configuration

Yann Jousseaume[1], François Cauwet[1], Bruno Gardiola[1], and Gabriel Ferro[1*]

[1]Laboratoire des Multimatériaux et Interfaces, UMR-CNRS 5615, Université Claude Bernard Lyon1, 6 rue Victor Grignard, 69622 Villeurbanne, France

Keywords: B1. Silicon carbide, A1. Surface structure, A.3 Liquid phase epitaxy, A.1 Dissolution, A.1 Step bunching, A1. Thermal simulation

Abstract. The structuring of Si face 4°off 4H-SiC surfaces was investigated using Si melting in a SiC/Si/SiC sandwich configuration. The stacks were treated at 1550-1600°C under H_2 in a RF-heated cold-wall reactor. By fixing the liquid Si thickness to 30 µm, the vertical thermal gradient inside the stack generates carbon transport from the bottom to the top SiC wafer. The constant dissolution of the bottom SiC wafer (1.7 µm/h at 1550°C) leads to surface structuring in macrosteps. The regularity of these macrosteps can be reproducibly controlled when performing the process on an epitaxial layer thanks to the pre-structuration in parallel microsteps of such kind of surfaces. The best regularity of the steps was obtained after a structuring process of 2h, with an average terrace width of ~3-5 µm.

Introduction

Despite the attractive properties of4H-SiC and its already wide use for power electronics, the performances of SiC metal-oxide-semiconductor field effect transistors (MOSFETs),which are the most fostered switches used in electric conversion systems[1], remain limited essentially due to low channel mobility [1,2]. This is mainly attributed to electrically active defects at the SiO_2/SiC. While the origin of these interface defect states is still under debate, there is a conjunction of experimental observations correlating them to the micro-stepped morphology of the 4°off epitaxial surfaces used [3,4]. Such morphology is expected to directly impact the creation of the SiO_2/SiC interface by eventually initiating non-ideal oxidations and non stoichiometric near-interface regions [5]. It was shown that, by using a macrostepped surface with few µm wide terraces, the interface traps density decreased by a factor of 10-15% on the fabricated MOS capacitors [6].In addition to the potential use of such surfaces for MOS devices, being able to control the regularity of the step bunching can be also useful to the researchers working on top seeded solution growth (TSSG) of SiC since in this case mastering the step bunched morphology is also critical [7,8].The difficulty is now to be able of producing such macrostepping in a reproducible way so as to be able to go further in this direction up to the fabrication of MOSFETs with improved channel mobility.

For creating such large terraces, the literature suggests the interaction of 4°off 4H-SiC crystal with liquid Si[9,10]. But this was essentially demonstrated using a sessile drop configuration. Such approach does not allow the processing of surfaces > ~ 0.5 cm^2 so that it cannot be seriously considered as a device processing step. To solve this problem, a SiC/Si/SiC sandwich configuration, virtually allowing the possible processing of larger 4H-SiC areas, is being investigated by the authors [11,12]. The preliminary experiments were successful in terms of uniform spreading of the liquid Si and formation of highly step-bunched surfaces. But difficulties were encountered for obtaining homogeneously distributed regular and parallel macrosteps, in relation with some complex carbon transport phenomena inside the liquid Si. The present work reports on the control

of mass-transport inside the stack and on the optimization of the sandwich approach for regular macrostepping.

Experimental

The SiC/Si/SiC sandwich setup used in this work for surface structuring of 4H-SiC is schematized in Figure 1. A piece of n-type Si wafer is positioned between two 4H-SiC (0001) 4°off Si-face wafers (250 µm thick) from SK Siltron company. The Si faces of both SiC wafers were placed in contact with the molten Siin order to undergo surface structuring upon Si melting. The SiC-top wafer mainly had the role of homogeneously spreading the liquid by a combination of pressing and wetting. The lateral size of the SiC-bottom wafer was larger than the top one (i.e. 2x2cm^2 and 1.2x1.2 cm^2, respectively) to avoid any Si loss from the 4H-SiC wafers sides upon melting. The experiments were carried out inside a vertical cold-wall reactor dedicated to chemical vapour deposition (CVD) of SiC. The stacks were placed on a SiC-coated graphite susceptor and RF-heated under 12 slmofH_2, with a ramp up rate of ~400°C/min up to 1550-1600°C. The targeted temperature was kept for 15-120 min. Such configuration leads to natural and homogeneous spreading of the liquid Si which perfectly wets both SiC pieces (no evidence of any gas trapping can be seen). After the treatments, the samples were wet etched in concentrated HF/HNO_3 for removing the Si and thus separating both wafers. In this work, we compare the use of different types of surfaces for the SiC-bottom wafer: as-received commercial n+ doped surface, re-polished surface (by Novasic company) and as-grown epitaxial surfaces (the epitaxial layers were grown in the same CVD reactor and using the conditions described in [13]).

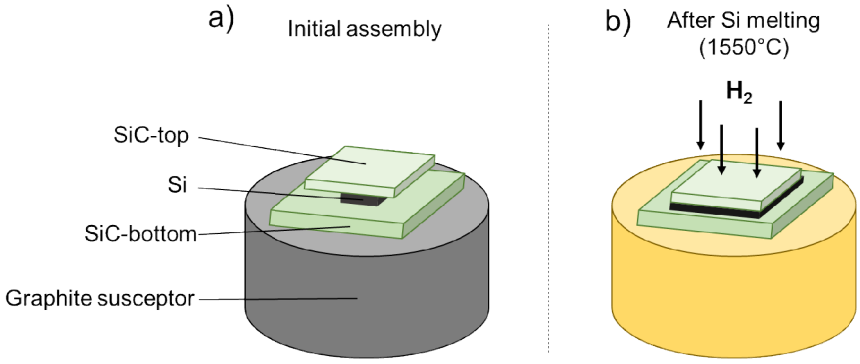

Figure 1. Schematic drawings of the investigated sandwich setup a) before and b) after Si melting;

We will thus assume that the area occupied by the liquid Si is equal to the surface of the SiC-top wafer, with no significant liquid overflow (as confirmed experimentally). Each Si piece is weighed before the experiment so that, from this mass m_{Si} and the area S occupied upon melting, one can calculate the Si thickness th_{Si} between the two SiC pieces using the following equation:

$$th_{si(\mu m)} = \frac{m_{Si(g)}}{d_{Si} \times S} \times 10^4$$

with d_{si} the Si density (in g.cm^{-3}), and S the area of the SiC-top wafer (1.44 cm^2). In this work, th_{Si} was set to 30 µm since this was found to be the best condition for controlling the homogeneity of the process [11]. It was previously proposed that the experimental conditions should generate a vertical thermal gradient inside the stack, leading to continuous carbon transport from the hotter

SiC-bottom wafer to the cooler top one, similarly as in classical liquid phase epitaxy experiments. In the present study, we will perform thermal simulation of the system in order to validate this hypothesis. Towards this end, the "Thermal transfer" module of COMSOL Multiphysics v.6.1 software was used. Details of the calculations are given in the annexes. Briefly, the unique heat source of the SiC/Si/SiC stack is the graphite below the SiC-bottom while the cooling (mainly on the top side) is simulated through both radiative and H_2 conduction losses. Note that a thermal resistance was inserted between the graphite susceptor and the bottom SiC wafer to simulate that such solid-solid interface is never perfect (see annexes). It leads to 15°C drop when passing from graphite to SiC-bottom wafer (see Figure 2).

Note that, as will be discussed below, some epitaxial growth is suspected to occur on the SiC-top wafer without any control of the doping level of this epitaxial deposit. According to the targeted MOSFET application, the control of the doping level at the SiC/SiO_2 interface is essential so that we will only focus in this work on the SiC-bottom wafer surface which undergoes only some slight dissolution (no growth).

The obtained structured surfaces of both SiC-top and -bottom wafers were characterized by various means: Nomarski differential interference contrast optical microscopy (NDIC), scanning electron microscopy (SEM, FEI Quanta 250 FEG) and atomic force microscopy (AFM) using Nano-Observer apparatus in resonant mode (CSI nstruments). For each sample, the average terraces width was measured on NDIC and SEM pictures, over a population of 100 to 300 terraces. In some cases, Multiple Images Alignment (MIA), involving the assembly of 20 to 40 NDIC images, was used for characterizing the entire structured areas. For specific samples, mechanical profilometry (Veeco Dektak 150) was performed on the areas of interest.

Results and discussion

Transport phenomena.

Result of thermal simulation of the system for a fixed susceptor temperature of 1550°C is shown in Figure 2. One can see that the SiC-top wafer is effectively cooler than the SiC-bottom one though the difference between the two surfaces in contact with liquid Si is rather small (1°C). This may look too small for triggering any C transport but when calculating the associated thermal gradient, a value as high as 333°C/cm is obtained. This is more than one order of magnitude higher than the usual values in TSSG experiments [14,15]. This thermal gradient seems thus sufficiently high for generating a C transport from the SiC-bottom (dissolution) to the -top (epitaxial growth).As a matter of fact, mechanical profiling of the SiC-bottom wafer after thermal treatment at 1600°C displays some matter loss (~0.4 µm) in the structured area (Figure 3). This confirms the hypothesis of thermal gradient driven C transport from the SiC-bottom to the -top, with a dissolution rate of ~ 0.8 µm/h. The deep depressions at the periphery of the wetted zone in Figure 3 are attributed to H_2 preferential etching of C atoms, as discussed in [11].

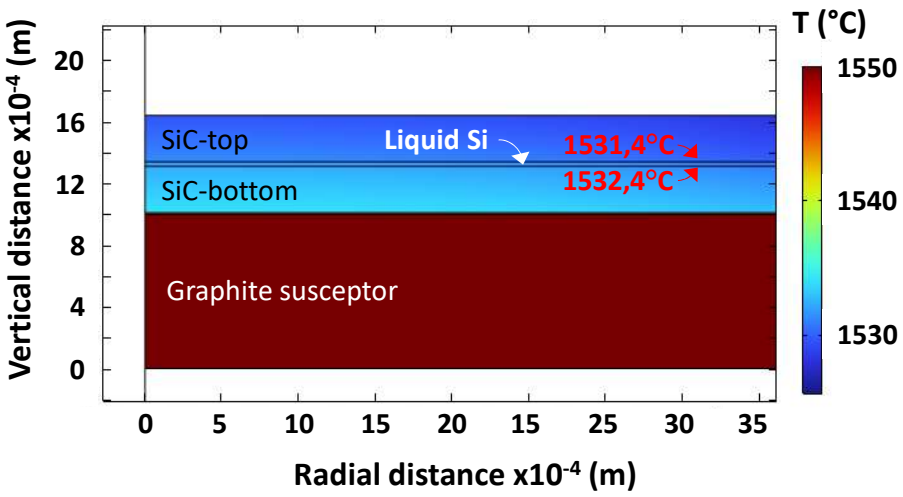

Figure 2. Thermal simulation of the SiC/Si/SiC stack for a susceptor heated at 1550°C.

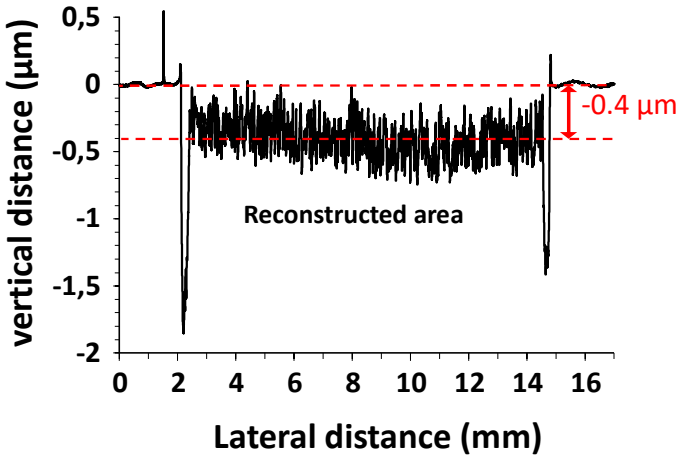

Figure 3. Linear mechanical profile obtained on a SiC-bottom wafer after structuration treatment at 1600°C for 30 min.

However, one should consider with care the determined value of dissolution rate because it was calculated by taking as zero reference the wafer level outside of the liquid. Since SiC is known to be thermally etched by H_2 under moderate rate (1-2 µm/h in the temperature range of the present study according to [16]), the 4H-SiC crystal outside the liquid undergoes probably the same H_2etching. Consequently, the surface level outside of the structured area is not the one of the initial substrate surface before the thermal treatment. In other words, the previously-estimated dissolution rate of 0.8 µm/h at the center of the sample is probably underestimated and one should add the H_2 etching rate of SiC to this value.

Since this etching rate depends on the experimental conditions (type of reactor, pressure, temperature, H_2 flow rate…) we have performed specific experiments in order to determine it for our operating conditions. Toward this end, a SiC wafer partially capped with a smaller piece of sapphire wafer was thermally treated under H_2. Below this cap, SiC loss by H_2 etching should be drastically reduced as compared to outside the cap, allowing thus some estimation of the etching rate by mechanical profiling measurement (Figure4). One can see that this simple capping

configuration was effective in protecting the SiC wafer from H_2 etching, leading toan etching rate estimation of ~2.5 µm/h outside the cap at 1600°C. If we then correct the dissolution rate of the bottom-SiC wafer by this value of H_2 etching rate outside the liquid, we obtain now a dissolution rate of 3.3 µm/h at 1600°C. Using the same process, the H_2 etching rate at 1550°C was found to be 1.7 µm/h, which leads to a dissolution rate of the same value at this temperature (since the zero level outside the liquid was found at the same altitude below the liquid).

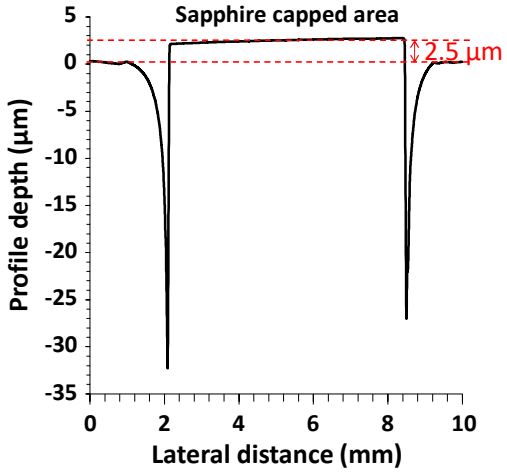

Figure 4. Linear mechanical profile obtained on a SiC wafer capped with a piece of sapphire wafer and treated under H_2 at 1600°C for 1h.

Assuming that all the C-dissolved atoms from the bottom wafer are transferred to the top-wafer, driven by the vertical thermal gradient, the dissolution rates determined above should represent the SiC epitaxial growth rate on the SiC-top wafer. Of course, one cannot exclude the occurrence of some slow etching of SiC under the sapphire piece so that the H_2 etching rates and thus the dissolution rates determined here are probably slightly underestimated. Note that the presence of extra Si atoms in the gas phase, coming from the edge evaporation of the liquid Si, could lower this etching rate as compared to H_2 only [17]. Altogether, both effects may somewhat counterbalance each other so that the estimated value are probably not so far from reality.

Coming back to Figure 4, deep trenches (down to 32 µm) can be seen on the SiC wafer at the edges of the area occupied by the sapphire piece. We believe that this over-etching could be linked to the lateral H_2 etching of the sapphire which is rather high at such temperature (≈ 40 µm/h) and is known to generate O-containing gaseous species such as H_2O [18]. Locally, the high generation of H_2O could significantly increase SiC etching rate and create these deep trenches.

Step bunched morphology

Figure5compares the morphology of the different SiC-bottom surfaces of this study, before (Fig. 5a) and after (Fig. 5b) structuring treatments using the same experimental parameters (1550°C for 2h). One can clearly see from the MIA that the steps are very parallel and continuously crossing the entire structured area for both re-polished and epilayer surface cases. On the contrary, when using as-received wafers, no pattern is distinguishable from the MIA. When looking closer to the step morphology by AFM (inserts in Fig. 5b), step edges on the as-received wafer are wavy and intersect with each other, while they are much straighter and parallel in the two other cases. The same morphologies were observed by performing several AFM scans on different zones of each sample.

The divergence in the obtained macrosteps structuring (using the same experimental conditions except for the type of surface) can thus be attributed to the initial morphology of these three different surfaces. As a matter of fact, the AFM images (Fig. 5a) of the epilayer and re-polished wafers both show an organized structure with microsteps at the nanometer scale though this structure is much fainter in the re-polished case. No specific microstructure is discernable in the case of the as-received wafer. Note that despite these morphological differences, these three starting surfaces display almost the same value of root mean square (RMS) roughness (~0.15 nm). These observations suggest that the Si-induced step-bunching mechanism may be strongly dependent on the initial surface morphology: disordered meandering of the step edges is obtained when the starting surface is undefined while a regular step and terrace structure is generated when starting from already formed microsteps.

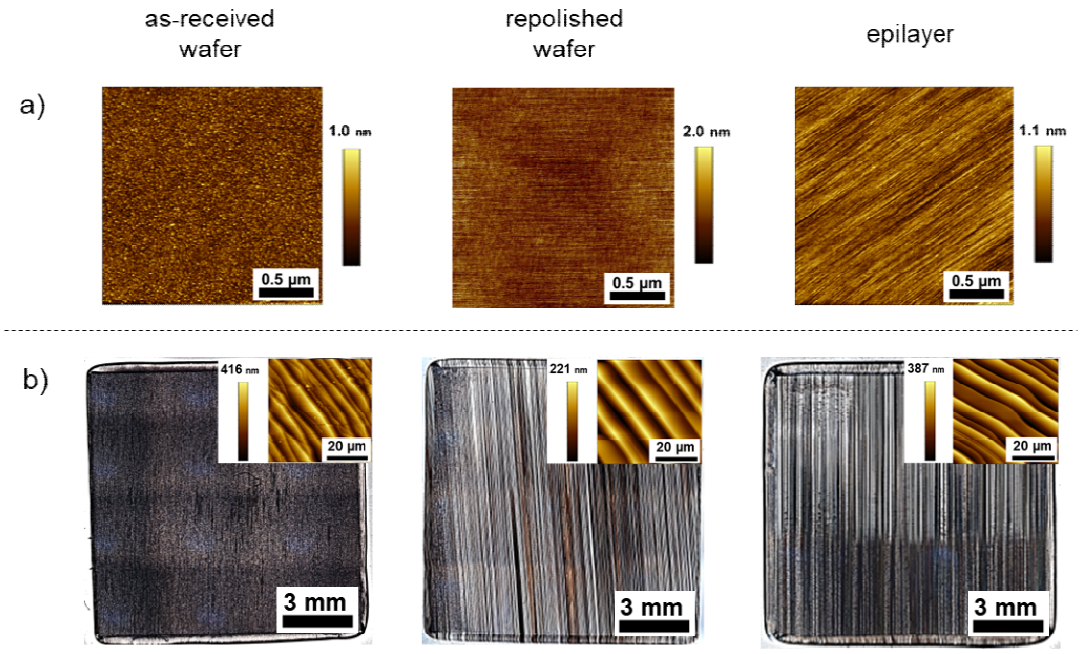

Figure 5. Morphology characterization of the different SiC-bottom wafers of this study a) before Si interaction (AFM images, 2x2 µm scans), and b) after Si interaction for 2h at 1550°C (MIA of the structured areas using optical microscopy with x25 objective). Insertsin b) show the corresponding AFM images (50x50 µm scans)obtained at the center of each structured area.

Regarding the reproducibility of these results, it was experimentally observed that, whatever the structuration duration(up to 2h),using as-received wafers systematically led to step meandering, whereas only parallel macrosteps were observed when using epilayers. The case of the repolished wafers was less straightforward as only half of these samples presented parallel macrosteps without meandering after surface structuring. The other half was rather similar to the as-received wafer case with high meandering of the steps. These experimental occurrences are summarized in Table 1. It can be reasonably argued that the occurrence of parallel steps after surface structuring is linked to the presence of these steps before the structuring: a sharper initial step structure increases the probability of obtaining straighter macrosteps after surface structuring. As seen from Fig. 5a, the step structure of the re-polished surfaces should be too faint to reproducibly generate the optimal step structuring after liquid Si interaction. We believe that a homogeneous and sharp microstepped surface is an essential prerequisite for obtaining a fully parallel and macrostepped structuring.

Table 1. Experimentally observed occurrences of parallel macrosteps on the SiC-bottom wafer using the sandwich Si-melting process on different initial surface types.

Starting surface	as-received wafer	Repolished wafer	epilayer
Occurrence of parallel macrosteps	0%	50%	100%

Considering the better control of the macrostepping allowed with epilayers, the time dependency of the step-bunching mechanism was investigated using epilayers only as starting surface. At first glance, both the SEM images and the histograms of Figure 6 suggest that increasing structuring time allows a reduction and homogenization of the mean step width. However, as seen in Figure 7a, a closer inspection by AFM on the apparent large terraces (> 20 µm width) formed after 15 min of interaction shows that it is not smooth (unlike expected from a natural terrace) but composed of microsteps similar to the original morphology of the starting epilayer. Furthermore, the AFM cross-section profile (Figure7b) obtained on such apparent large terraces does not follow the regular increase and decrease of the altitude expected in standard step bunching. Instead, the profile is flat when measured on these apparent large terraces, especially the larger ones. This is not observed in the case of the narrower (but more regular) steps formed after 2h of structuring, for which the cross-section profile corresponds to a standard step bunched morphology (with average step width and height of 3-5 µm and 0.2-0.3 µm respectively). It can thus be proposed that these large areas formed during short structuring time are in fact unreacted zones and thus cannot be considered as macrosteps. This leads us to suggest the structuring scenario illustrated in Figure 8. Basically, it involves that the step bunching does not occur homogeneously over the entire surface but rather starts at specific step edges, by local dissolution of SiC into liquid Si. This dissolution continues laterally and along the basal plane. When the contact duration with liquid Si is increased, new dissolution starting points appear and propagate in the same manner.

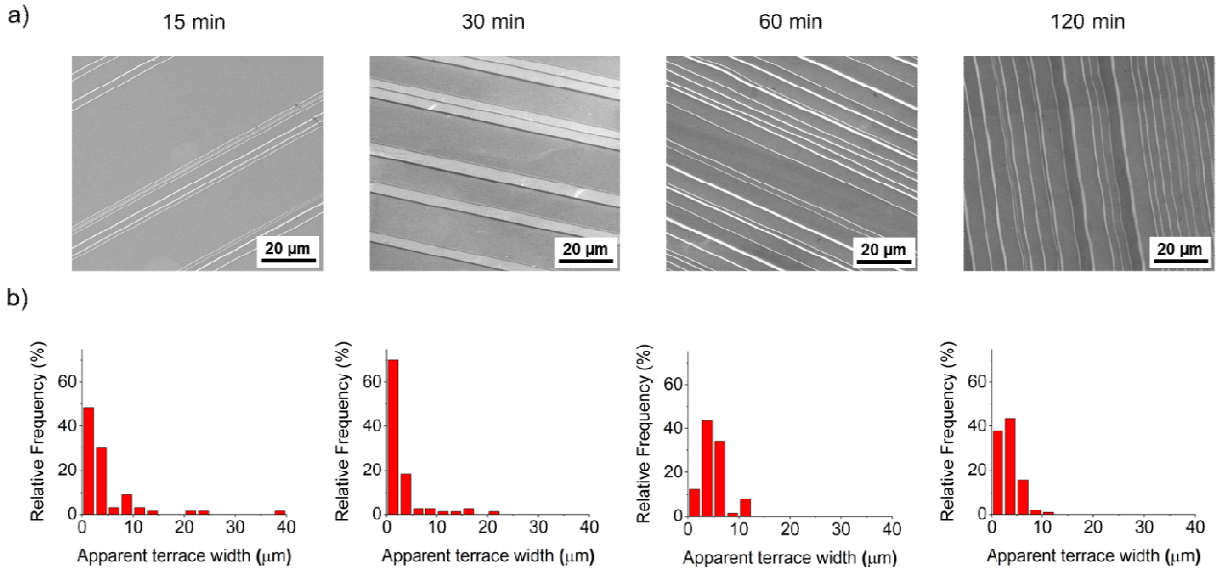

Figure 6. Effect of the structuring durationon a) the surface morphology as observed by SEMand b) the corresponding apparent step width distributions. These results were obtained using epilayer surfaces as bottom wafer of the stack.

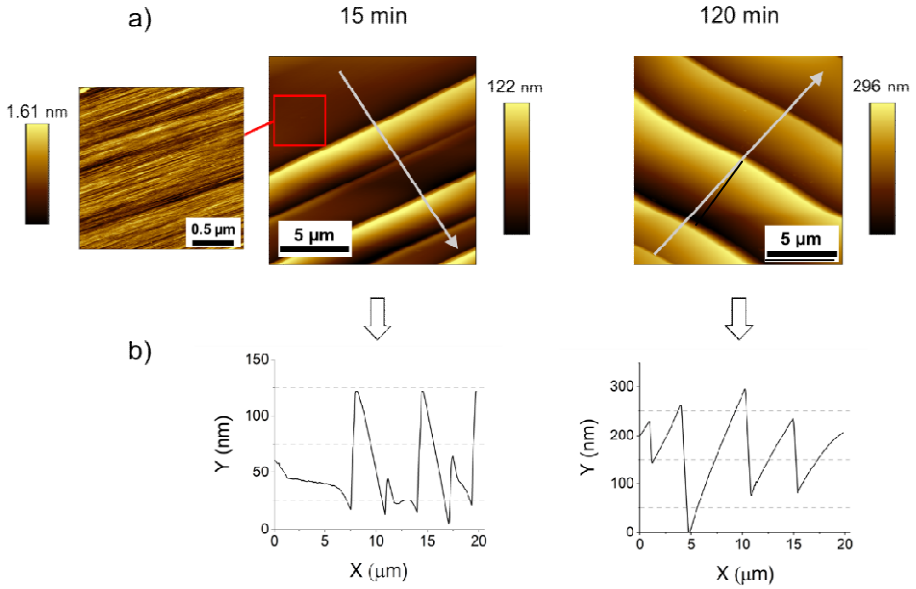

Figure 7. a) AFM images (15x15 µm scans, 2x2 µm scan on the left) of the surface morphology after 15 and 120 min of interaction with liquid Si and b) the corresponding cross section profiles along the grey arrows drawn in a).

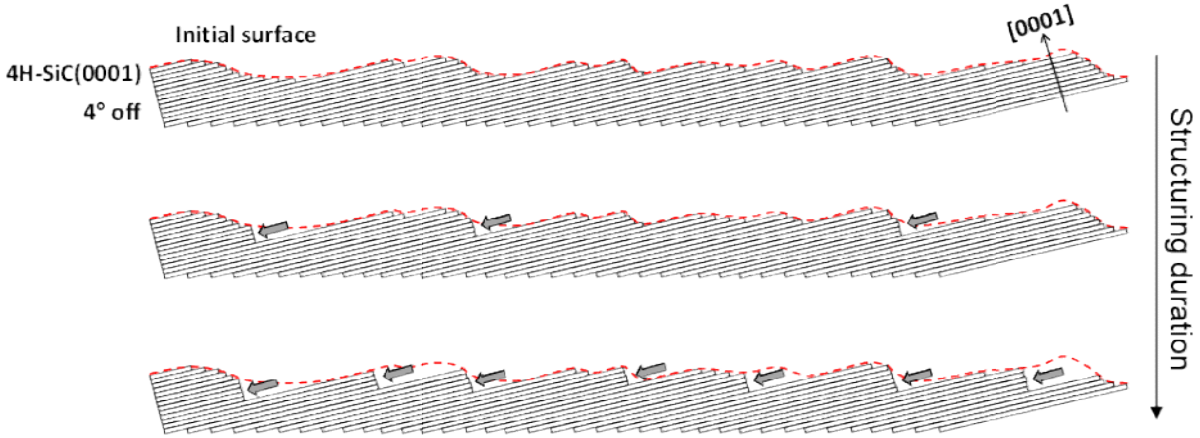

Figure 8. Schematic illustration of the proposed mechanism explaining the time dependence of the surface structuring evolution. The initial surface is drawn wavy for representing the microstepped structure of the starting epilayer.

The next step would be to see how the proposed mechanism could fit with the literature on step bunching and faceting. Most of these papers concern crystal growth while very few deals with dissolution. The step bunching is often associated with the presence of an Ehrlich-Schwoebel (ES) barrier (additional energy barrier experienced by adatoms when diffusing down a step or a kink) [19] which variation in 1-, 2- or 3-D mode can lead to step edge roughening or even step meandering [20]. However, applying this ES barrier for explaining the present results is not simple. Indeed, one would need to consider ES barrier variation depending on the initial surface morphology. In addition, one cannot just say that growth is basically the reverse of dissolution. For instance, it was predicted that while growing crystals could evolve toward a steady-state shape, dissolving crystals could evolve away from a steady-state shape [21]. Another illustration of such difference between growth and dissolution can be found in a previous work made on this sandwich

configuration [11] in which the step bunched morphology was found to differ between the SiC-top and SiC-bottom wafers of the stack (with identical 30 µm liquid Si thickness). And, as discussed earlier, the SiC-top wafer should be subjected to crystal growth while the SiC-bottom should undergo dissolution.

Finally, results presented in [10], obtained in a sessile drop configuration, are probably the closest work to refer to since it concerns only dissolution at relatively similar temperature (1600°C). It was reported that parallel steps can be obtained on Si face when the system is in a stationary dissolution state. This corroborate well with our experimental conditions tough the impact of the initial surface morphology is not discussed in this paper.

Summary

A process allowing the reproducible structuring of 4°off 4H-SiC surfaces into parallel macrosteps was successfully demonstrated. It involves the thermal treatment under H_2 at 1550°C of a SiC/Si/SiC sandwich set up with a 30 µm thick liquid Si interlayer. The dissolution occurring on the SiC-bottom wafer, due to the thermal gradient inside the stack, naturally generates a step bunching whose parallelism can be reproducibly controlled via the prior deposition of an epitaxial layer. The optimal treatment time of 2 h leads to regular arrays of ~ 3-5µm wideterraces. In addition to the potential use of such surfaces for testing MOS devices, the results of the present paper can be useful to the TSSG crystal growers for who the control of the step bunched morphology is critical.

Acknowledgements

This work has been financially supported by French ANR in the framework of the 19-CE24-0007 "Risemos" project. Electron microscopy was performed at the Centre Technologique des Microstructures of the University of Lyon (CTmu).

References

[1] C. Langpoklakpam, A.-C. Liu,K.-H. Chu, L.-H. Hsu, W.-C. Lee, S.-C. Chen, C.-W. Sun, M.-H. Shih, K.-Y. Lee, H.-C. Kuo, *Review of Silicon Carbide Processing for Power MOSFET*. **Crystals 2022, *12*, 245**. Doi: 10.3390/cryst12020245

[2] S. Das, Y. Zheng, A. Ahyi, M.A. Kuroda, S. Dhar, *Study of Carrier Mobilities in 4H-SiC MOSFETS Using Hall Analysis*. **Materials 15 (2022) 6736**. Doi: 10.3390/ma15196736

[3] J. Woerle, B. C. Johnson, C. Bongiorno, K. Yamasue, G. Ferro, D. Dutta, T. A. Jung, H. Sigg, Y. Cho, U. Grossner, and M. Camarda, *Two-dimensional defect mapping of the SiO_2/4H−SiC interface*. **Phys. Rev. Mater. 3 (8) (2019) 084602**. Doi: 10.1103/PhysRevMaterials.3.084602

[4] N. Alyabyeva, J. Ding, M. Sauty, J. Woerle, Y. Jousseaume, G. Ferro, J.C. McCallum, J. Peretti, B.C. Johnson, A.C.H. Rowe, *Nanoscale Mapping of Sub-Gap Electroluminescence from Step-Bunched, Oxidized 4H-SiC Surfaces*. **Phys. Status Solidi B (2023), 2200356.** Doi: 10.1002/pssb.202200356

[5] I. D. P. Fiorenza, F. Iucolano, G. Nicotra, C. Bongiorno, F. A. L. Magna, F. Giannazzo, M. Saggio, C. Spinella, F. Roccaforte, *Electron trapping at SiO_2/4H-SiC interface probed by transient*

capacitance measurements and atomic resolution chemical analysis. **Nanotechnology 29 (39) (2018) 395702**. Doi:10.1088/1361-6528/aad129

[6] M. Camarda, J. Woerle, V. Souliere, G. Ferro, H. Sigg, U. Grossner, and J. Gobrecht, *Analysis of 4HSiC MOS Capacitors on macro-stepped surfaces*. **Mater. Sci. Forum, 897, (2017), 107–110**. Doi: 10.4028/www.scientific.net/MSF.897.107

[7] K. Murayama, T. Hori, S. Harada, S. Xiao, M. Tagawa, T. Ujihara, *Two-step SiC solution growth for dislocation reduction*, **J. Crystal Growth 468 (2017) 874-878**. Doi: 10.1016/j.jcrysgro.2016.11.100

[8] Y. Dang, X. Liu, C. Zhu, Y. Fukami, S. Ma, H. Zhou, X. Liu, K. Kutsukake, S. Harada, T. Ujihara, *Modeling-Based Design of the Control Pattern for Uniform Macrostep Morphology in Solution Growth of SiC*, **Crystal Growth & Design 2023 23 (2), 1023-1032**. Doi: 10.1021/acs.cgd.2c01194

[9] V. Soulière, D. Carole, M. Camarda, J. Woerle, U. Grossner, O. Dezellus, and G. Ferro, *4H-SiC(0001) surface faceting during interaction with liquid Si*. **Mater. Sci. Forum, 858, (2016), 163–166**. Doi: 10.4028/www.scientific.net/MSF.858.163

[10] X. Xing, T. Yoshikawa, O. Budenkova, and D. Chaussende, *A sessile drop approach for studying 4H-SiC/liquid silicon high-temperature interface reconstructions*, **J. Mater. Sci., 57, 2, (2022), 972–982**. Doi:10.1007/s10853-021-06816-y

[11] Y. Jousseaume, F. Cauwet, G. Ferro. *Macrosteps formation on 4H-SiC surfaces via Si melting within a sandwich configuration*. **J. Crystal Growth 593 (2022) 126783**. Doi: 10.1016/j.jcrysgro.2022.126783

[12] Y. Jousseaume, F. Cauwet, J. Wörle, U. Grossner, G. Ferro, *Controlled macrostepping of Si-face 4°off 4H-SiC over a large area via liquid Si-induced reconstruction*, To be published in **Mater. Sci. Forum 2023**.

[13] K. Alassaad, V. Soulière, F. Cauwet, H. Peyre, D. Carole, P. Kwasnicki, S. Juillaguet, T. Kups, J. Pezoldt, G. Ferro, *Ge incorporation inside 4H-SiC during Homoepitaxial growth by chemical vapor deposition*. **Acta Materialia, 75, (2014), 219–226**. Doi: 10.1016/j.actamat.2014.04.057

[14] F. Mercier, J.-M. Dedulle, D. Chaussende, M. Pons, *Coupled heat transfer and fluid dynamics modeling of high-temperature SiC solution growth*. **J. Crystal Growth 312 (2010) 155–163.** Doi: 10.1016/j.jcrysgro.2009.10.007

[15] S.Endo, K. Kamei, Y. Kishida, K. Moriguchi, *Effects of crystalline polarity and temperature gradient on stepbunching behavior of off-axis 4H-SiC solution growth*, **Mat. Science Forum 821-823 (2015) 26-30.** Doi: 10.4028/www.scientific.net/MSF.821-823.26

[16] C. Hallin, F. Owman, P. Mårtensson, A. Ellison, A. Konstantinova, O. Kordina, E. Janzèn, *In situ substrate preparation for high-quality SiC chemical vapour deposition*, **J. Cryst. Growth, 181, (2024), 241–253**. Doi: 10.1016/S0022-0248(97)00247-9

[17] K. Kojima, S. Kuroda, H. Okumura, K. Arai, *Effect of additional silane on in situ H_2 etching prior to 4H-SiC homoepitaxial growth*, **Mater. Sci. Forum 556-557 (2007) 85-88**. Doi:10.4028/www.scientific.net/MSF.556-557.85

[18] L.A. Marasina, V. V. Malinovsky, I. G. Pichugin, P. Prentky, *Chemical Etching of Sapphire*, **Crvstal Res. & Technol. 17 (3) (1982) p.36**. Doi: 10.1002/crat.2170170320

[19] M. Lagally, Z. Zhang, *Thin-film cliffhanger*. **Nature 417 (2002) 907–909**. Doi: 10.1038/417907a

[20] H. Turski, F. Krzyżewski, A. Feduniewicz-Żmuda, et al., *Unusual step meandering due to Ehrlich-Schwoebel barrier in GaN epitaxy on the N-polar surface*, **Appl. Surf. Sci. 484 (2019) 771-780**. Doi: 10.1016/j.apsusc.2019.04.082

[21] R.C. Snyder, M.F. Doherty, *Faceted crystal shape evolution during dissolution or growth,* **AIChE Journal Vol. 53, No. 5 (2007) 1337**. Doi: 10.1002/aic.11132

Annexes

Thermal simulation of a graphite/SiC/Si$_{(liq)}$/SiC stack under H_2 atmosphere.

The calculations were performed with COMSOL Multiphysics v.6.1 software using the "thermal transfers" module. The simulated stack involves a SiC/Si(liq)/SiC sandwich in contact with a bulk graphite piece which is heated. The graphite is the only source of heat in the system. See figure A1 for a representation of the simulated box.

In order to stick the reality as much as possible, the following hypotheses were formulated:

- Axisymetric model along the vertical axis r = 0
- The thermal contacts within theSiC/Si/SiC stack are supposed ideal due to good wetting of liquid silicon.
- Thickness of each part of the stack: SiC = 250 µm, Si = 30 µm
- Graphite part homogeneously heated at 1550°C (unique source of heat)
- Heating of the stack by thermal conduction with the graphite part. The contact between the graphite and the SiC-bottom wafer was not assumed perfect. An additional thermal resistance was applied at the interface under the form of a simulated roughness of 15 µm.
- Cooling from the top part of the stack, modelled with natural radiation (emissivity of 0.8 and 1 respectively for SiC and graphite) and H_2 thermal conduction. The backside of the graphite part is not considered in contact with H_2.
- H_2flow from the above part was simulated using a velocity field of 0.1 m.s^{-1}. Its thermal conductivity (extrapolated to 1550°C) was set to k = 2 W.m^{-1}.K^{-1}.

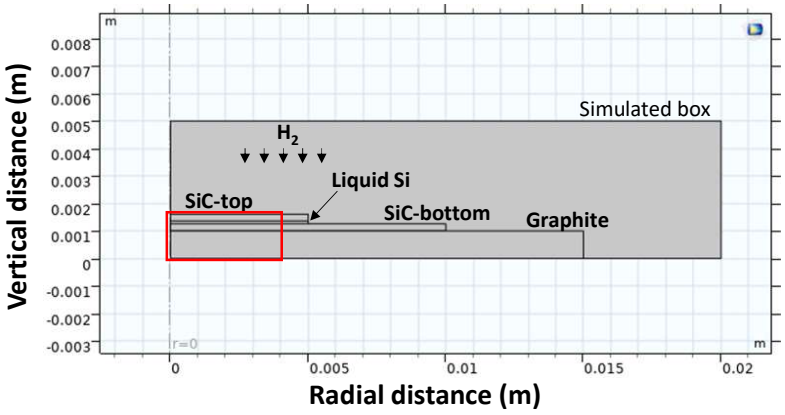

Figure A1: Schematic representation of the simulated box before calculations. The red square corresponds to the area shown in Figure 1 of the paper.

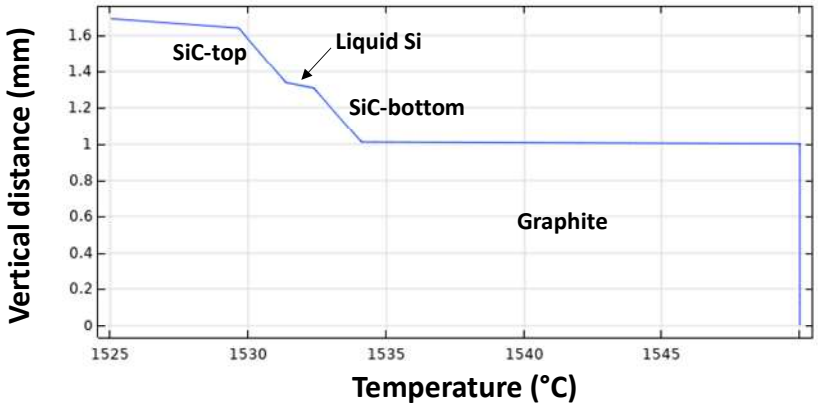

Figure A2. Temperature evolution along the vertical axis at r = 0, after calculations.