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Comparator Circuit for Power Applications based on Enhancement-mode p-GaN HEMTs

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1. Abstract

This paper presents a new comparator design for power applications using Enhancement-mode p-GaN HEMT Process Design Kit (PDK) developed by IMEC. The comparator drives a 200 V power p-GaN HEMT achieving rising/falling times of 1.4 ns and 2.5 ns respectively, and a propagation delay time of 3 ns for a rated output voltage of 6 V and 1 MHz of switching frequency. Transistor-level simulations are carried out using Cadence Software under temperature and load variation to verify the performance of the circuit.

2. Introduction

Gallium Nitride (GaN) - High Electron Mobility Transistor (HEMT) technology has been introduced during the last decade. In power applications when high-frequency and high-temperature is required, GaN-based devices show up better performance than Silicon Carbide (SiC)-based devices [1]. Nowadays, GaN on Silicon-on-Insulator (GaN-on-SOI) technology allows monolithic integration of low and high-power devices in a single Integrated Circuit (IC) [2]. In this way, the parasitic inductance of circuits that use discrete devices can be reduced. In power electronics circuits, gate drivers are required to provide the voltage level to turn-on the power devices. Gate driver ICs include a comparator circuit, which plays an important role to interface the low voltage input from a digital controller with the high-power switches [3].

In 2009, Depletion-mode (D-mode) GaN-on-Silicon (GaN-on-Si) HEMT technology was used to integrate a temperature-compensated comparator and a high-voltage power device in one smart power chip [4]. In 2011, a gain-bootstrapped comparator using Enhancement-mode (E-mode) and D-mode AlGaN/GaN HEMTs on GaN-on-Si was reported. E-mode HEMT was introduced as current source to eliminate the negative power supply [5]. In 2020, an auto-zero comparator and a high voltage supply regulator were designed employing only E-mode p-GaN HEMTs [3]. In 2021, a GaN comparator derived from a Resistor-Transistor Logic (RTL) is presented. The inverters of this comparator consist in a p-GaN HEMT acting as pull-down and a resistive load working as pull-up. Nevertheless, the use of resistors in ICs involve large operating currents [6]. On the other hand, despite the technological maturity that GaN has reached over the years, the lack of a P-type device implies a challenge in analog design.

This work proposes a new comparator circuit using Enhancement-mode p-GaN HEMT logic devices using. The new comparator uses N-type transistor acting as diode-connected load instead of the resistors

used in [6]. The comparator is designed to drive a 200 V GaN HEMT power device. To validate the performance of the circuit, transistor-level simulations under temperature and load variation were developed in Cadence using E-mode p-GaN IMEC- PDK.

3. Methodology

In this work, E-mode p-GaN power ICs process PDK is used. This technological platform has the following components [7]: a Low Voltage device (LV), a High Voltage device (HV), a 2DEG (Two-Dimensional Electron Gas)-based resistor, and a MIM (Metal-Insulator-Metal) capacitor. In Fig. 1, the schematic circuit of the proposed comparator is depicted. As can be seen, the comparator has three main stages. The differential pair input stage is formed by Q_3 and Q_4 in diode-connected structure. The input bias is given by Q_9 acting as diode-connected and Q_{10} - Q_{12} form a current mirror. The second one is a differential gain stage, where Q_7 , Q_8 , Q_{13} and Q_{15} work as diode-connected loads. The output stage provides an output voltage (V_o) through Q_{17} and Q_{18} . The p-GaN HEMTs working as diode-connected loads are shown in blue color (see Fig. 1).

The proposed comparator is based on p-GaN HEMT Low Voltage devices with a gate Threshold Voltage (V_{TH}) of 2.6 V and a gate-drain length (L_{GD}) of 1.2 μm . Meanwhile, the power p-GaN HEMT has a L_{GD} of 5.75 μm , an effective Gate Width (W_G) of 36 mm, a Drain-Source ON resistance ($R_{DS,ON}$) of 40 m Ω and a Gate-Source Capacitance (C_{GS}) of 52 pF, operating at a frequency of 1 MHz. The Drain-Source Voltage (V_{DS}) is 200 V and the Drain Current (I_D) is equal to 10 A [7]. The power device requires a gate-source voltage of 6-7 V [3]. Therefore, the aspect ratio (width-to-length W/L) of each logic transistor of the comparator is optimized by simulation (see Table I) to achieve an output voltage equal to 6 V with a voltage supply (V_{DD}) of 7 V.

Table 1. Feature size of Low Voltage p-GaN HEMTs

	W/L		W/L
Q_1, Q_2	30 $\mu\text{m}/1.2 \mu\text{m}$	Q_{10}, Q_{11}, Q_{12}	10 $\mu\text{m}/1.2 \mu\text{m}$
Q_3, Q_4	2.3 $\mu\text{m}/1.2 \mu\text{m}$	Q_{13}, Q_{15}	300 $\mu\text{m}/1.2 \mu\text{m}$
Q_5, Q_6	30 $\mu\text{m}/1.2 \mu\text{m}$	Q_{14}, Q_{16}	10 $\mu\text{m}/1.2 \mu\text{m}$
Q_7, Q_8	2.7 $\mu\text{m}/1.2 \mu\text{m}$	Q_{17}	5 $\mu\text{m}/1.2 \mu\text{m}$
Q_9	12 $\mu\text{m}/1.2 \mu\text{m}$	Q_{18}	40 $\mu\text{m}/1.2 \mu\text{m}$

4. Results

In Fig. 2, the voltage transfer curve of the p-GaN comparator is depicted. The Reference Voltage (V_{ref}) increases from 2.5 V to 5 V with a step size of 0.5 V, and temperature varies from 27°C to 250°C. The Lower Output Voltage (V_{OL}) of the comparator is 80 mV and the Higher Output Voltage (V_{OH}) is 6 V, while

V_{ref} is lower than 4.5 V. With higher V_{ref} values, the V_{OH} starts to drop. In the worst-case scenario, at the highest temperature, the curves show a maximum voltage decrease of 8.33 %, which indicates the shift of the V_{TH} due to the increase in temperature.

The Fig. 3a presents the rising and falling times and Fig. 3b shows the propagation delay time of the proposed comparator under temperature variation. The comparator exhibits fast rising and falling times achieving 1.4 ns and 2.5 ns respectively. The propagation delay times are 2.5 ns (rise) and 3ns (fall) at 27°C. These results show a good performance of the comparator and smaller values than other structures presented in [3] and [6]. As can be seen in Fig. 3, rising, falling and propagation delay times increase as the temperature does.

The total power consumption of the comparator under load and frequency variation is shown in Fig. 4. Static and dynamic losses due to switching frequency, capacitive load, and voltage supply has been considered. The overall power consumption of the comparator is 24 mW handling a load of 52 pF and operating at 1 MHz. Fig. 4 illustrates that dynamic losses rise due to the increase of the operating frequency.

5. Conclusion

In this paper, a new comparator circuit was designed using E-mode p-GaN HEMT PDK. The circuit was simulated and analyzed under temperature, load, and frequency variations. The comparator presents fast turn on/off transitions lower than 2.5 ns working at 1 MHz. Despite the challenge that the lack of a P-type device implies, the results demonstrated the feasibility of monolithic integration of low voltage circuits and GaN HEMT power devices for high power applications.

6. Acknowledgment

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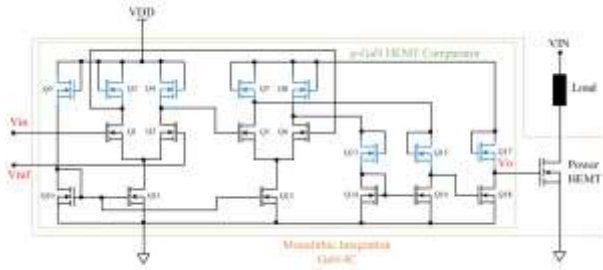


Fig.1: Transistor level E-mode p-GaN HEMT comparator

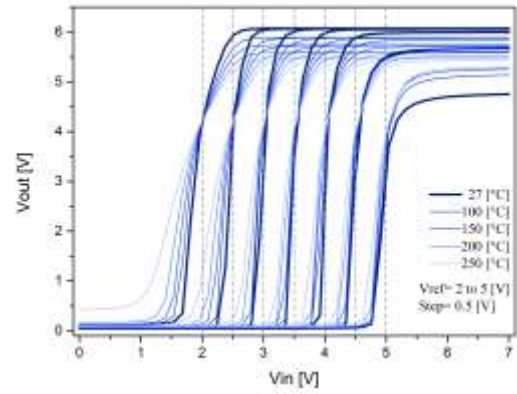


Fig.2: Voltage transfer curves of the p-GaN Comparator

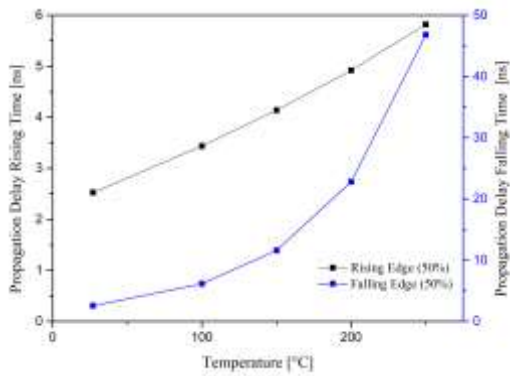
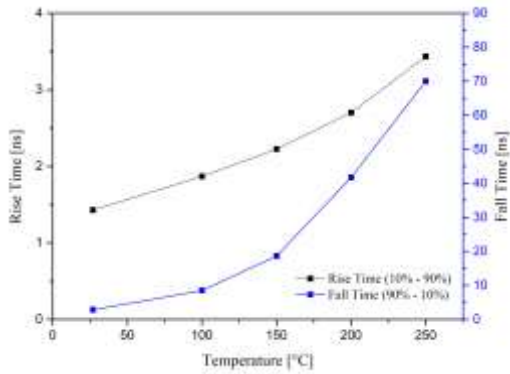


Fig.3: (a) Rising and falling time (b) Propagation delay time ($V_{DD}=7V$, Switching frequency = 1 MHz, $C_{load}=52pF$)

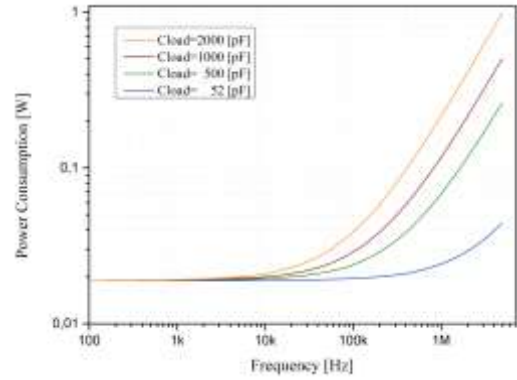


Fig.4: Total power dissipation of the p-GaN comparator ($V_{DD}=7V$)