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***Abstract*—This paper presents the design of three new comparators circuits for power applications using Enhancement-mode p-GaN HEMT Process Design Kit (PDK) developed by IMEC. The design challenge in this technology is the lack of P-type devices, therefore diode-connected structures with N-type devices are introduced as pull-up devices. Comparators are monolithicaly integrated with 200V/10A power p-GaN HEMTs. The output voltage of the comparators is set to 6V to turn-on the power device suitably. To verify the performance of the circuits, 1MHz of input signal frequency is selected. Relevant parameters such as rising, falling and propagation delay times, together with the power-delay product are discussed. For rated output voltage and frequency, the lower rise/fall/propagation delay times achieved are 0.83/0.89/1.14 ns. Transistor-level simulations and proof of concept of each proposed structure are carried out considering temperature and frequency variation.**

***Index Terms*—comparator, gallium nitride, p-GaN, HEMT, gate driver**

I. Introduction

Gallium Nitride (GaN) material based technology enable devices like High Electron Mobility Transistor (HEMT) with better thermal conductivity, low resistance, and high electron mobility of the Two-Dimensional Electron Gas (2DEG) compared to Silicon Carbide (SiC) ones [1]. Therefore, GaN-HEMTs are more suitable for power applications when high-frequency and high-temperature are required, namely in medium and high-power [2]. Nevertheless, GaN technology based devices are normally-ON devices (Depletion-mode) limiting the field of applications to simple switch for power converters. To overcome the lack of normally-OFF GaN HEMTs, a layer of magnesium (Mg) doped GaN layer (p-GaN) between the gate and the AlGaN/GaN heterostructure can be placed [3]. Hence, this p-GaN layer helps to deplete the 2DEG resulting in a normally-OFF device [4]. Recently, the introduction of GaN-on-SOI (GoS) process [5] have enabled a monolithic integration of p-GaN (normally-OFF or Enhancement-mode) along with the conventional GaN devices, similarly to CMOS process. This technology have been introduced in the perspective: 1) to implement GaN based integrated circuits (GaN-ICs) [6] 2) to build power management units and 3) to get more energy efficient operation of power electronic systems [7].

Further, it has been reported a significative reduction of parasitics inductance of GaN-ICs compared to circuits with discrete components [8]. Nowadays, Gallium Nitride has reached enough technological maturity and the market shows an increasing trend of the GaN-IC based devices for high power applications (from 200V to 1kV) [9]. It is important to remind that power electronics circuits require gate drivers to provide specific voltage and current level to turn-on the power devices. Gate driver ICs include a comparator circuit, which plays an important role to interface the low voltage input from a digital controller with the high-power switches [10]. In 2009, Depletion-mode (D-mode) GaN-on-Sillicon HEMT technology was used to integrate a temperature-compensated comparator and a high-voltage power device in one smart power chip [11]. In 2011, a gain-bootstrapped comparator using Enhancement-mode (E-mode) and D-mode AlGaN/GaN HEMTs on GaN-on-Si was reported. E-mode HEMT was introduced as current source to eliminate the negative power supply [12]. In 2020, an auto-zero comparator and a high voltage supply regulator were designed with a 650V E-mode p-GaN gate GaN-on-Si plataform employing only E-mode p-GaN HEMTs [13]. In 2021 [14], a GaN comparator derived from a Resistor-Transistor Logic (RTL) is presented. The inverters of this comparator consist in a p-GaN HEMT acting as pull-down and a resistive load working as pull-up. Nevertheless, the use of resistors in ICs involve large operating currents. Despite the advances in GaN technology over the years, the lack of a P-type device implies a challenge in analog design.

This work proposes three new designs of comparator circuits using Enhancement-mode p-GaN HEMT logic devices. The new comparators use active load (diode-connected) instead of the passive load (resistors) used in previous works [11]- [14]. The design of the comparators are optimized to satisfy the gate driving conditions of the 200V/10A GaN HEMT power device. To assess the performance of these new proposal, transistor-level simulations under temperature and frequency variation were carry out in Cadence Virtuoso using 200V E-mode p-GaN PDK from IMEC.

This paper is divided into following sections. In Section II, the methodology is presented. Section III, the proposed schematic circuits are described and explained. In Section IV, the simulation results are shown and the performance assessment of the comparators are examined through Figure-of-Merits (FOM) we proposed. Conclusions of the work are presented in the last section.

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II. Methodology

In this work, E-mode p-GaN power ICs process is used through the GaN-IC PDK of Imec [4] to design three new comparators. This technological platform has the following components: N-type HEMT Low Voltage device (LV), N-type HEMT High Voltage device (HV), 2DEG-based resistor, and MIM (Metal-Insulator-Metal) capacitor.

The proposed comparators are based on p-GaN HEMT Low Voltage devices with a Threshold Voltage (V_{th}) of 2.6V and a Gate-Drain Length (L_{GD}) of 1.2μm. The power p-GaN HEMT has the following electrical characteristics: L_{GD}=5.75μm, an effective Gate Width (G_W) of 36mm, a Drain-Source ON resistance ($R_{DS,on}$) of 40mΩ and a Gate-Source Capacitance (C_{GS}) of 52pF, operating at 1MHz. The power switch has a Drain-Source Voltage (V_{DS}) of 200V and a Drain Current (I_D) of 10A [4]. It is worth noting that power devices require a gate-source voltage of 6-7V [13] to ensure its turn-on. Therefore, the aspect ratio (W/L) is optimized by simulation to achieve a rated Output Voltage (V_o) of 6V.

III. Proposed Topologies for p-GaN Comparators

In this section three new comparator circuit topologies are proposed. In Fig. 1, the schematic circuit of the first comparator (T_1) is depicted. This structure uses p-GaN HEMTs as diode-connected load (shown in blue color Fig. 1) instead of the resistors used in [14]. As it can be seen, this topology

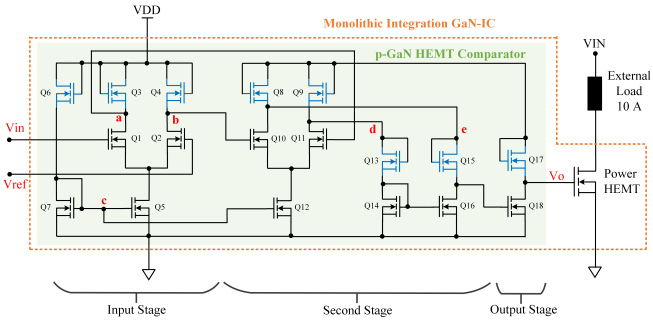

Fig. 1. Transistor level N-type p-GaN HEMT Comparator 1 (T_1)

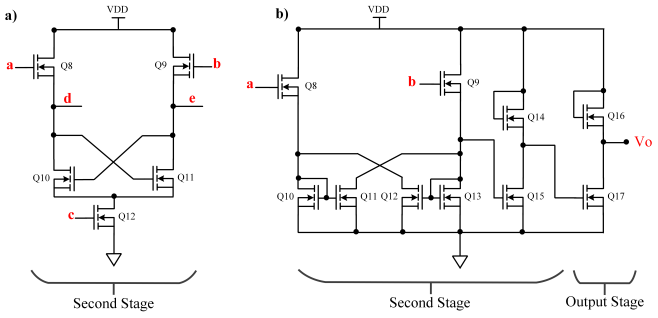

Fig. 2. Transistor level N-type p-GaN HEMT a) Comparator 2 (T_2) b) Comparator 3 (T_3)

has three main stages. The differential pair input stage (Q_1 and Q_2) are linked to a diode-connected (active) load (Q_3 and Q_4). The input bias of the circuit is fixed by Q_6 and the current mirrors: Q_5,Q_7,Q_{12}. The second stage is a differential gain amplifier stage, where Q_8 and Q_{10} (Q_9 and Q_{11}) work as common source with active load (diode-connected loads). The output stage provides V_o through Q_{17} and Q_{18}, which is stabilized by the level-shift circuit formed by Q_{13}, Q_{14}, and Q_{15}, Q_{16} .

The second proposed comparator (T_2) is illustrated in Fig. 2a. The input, output and bias stages are the same as the first comparator. However, a cross-coupled gate configuration is included in the second stage to increase the Voltage-to-Current gain (via the output resistance) and hence improve the speed of the circuit. The drain terminal of Q_{10} is connected to the gate of Q_{11}, while the gate of Q_{10} has the same potential that drain of transistor Q_{11}.

Fig. 2b displays the third proposed comparator (T_3). The transistors of the input differential pair are biased by Q_6 (diode-connected) and Q_5, Q_7 working as current mirror. The second stage of this comparator is formed by a self-biased cross-coupled latch (Q_{10}, Q_{11}, Q_{12}, Q_{13}). Source followers (Q_8, Q_9) and diode-connected transistors (Q_{10}, Q_{13}) work as common-mode feedback loop with low gain. The output voltage is achieved through Q_{16} and Q_{17}. The main advantage of using a cross-coupled latch is reducing transitions times [16].

In the output stage, the Higher Output Voltage (V_{OH}) and Lower Output Voltage (V_{OL}) are determined by the aspect ratio relationship of upper and lower GaN HEMTs. The difference between V_{OH} and V_{OL} is called output voltage swing. To reach an output voltage of 6V, the minimum Voltage Supply (V_{DD}) must be at least V_{OH} plus V_{th} of the LV device used in the circuit. The values between minimum and maximum Input Voltage (V_{in}) where the comparator can switch the output level without error is denominated comparison range. In this study, aspect ratio optimization of each LV device was performed. The obtained values are shown in Table I.

TABLE I
Circuit Parameters

Comparator 1 (T_1)		**Comparator 2** (T_2)		**Comparator 3** (T_3)	
Parameter	**W**	**Parameter**	**W**	**Parameter**	**W**
Q_1,Q_2	30μm	Q_1,Q_2	10μm	Q_1,Q_2	7μm
Q_3,Q_4	2.3μm	Q_3,Q_4	20μm	Q_3,Q_4	55μm
Q_5,Q_6,Q_7	10μm	Q_5,Q_6,Q_7	10μm	Q_5,Q_6,Q_7	5μm
Q_8,Q_9	2.7μm	Q_8,Q_9	250μm	Q_8, Q_9	50μm
Q_{10},Q_{11}	30μm	Q_{10},Q_{11}	5μm	Q_{10},Q_{11}	2μm
Q_{12}	10μm	Q_{12}	35μm	Q_{12}, Q_{13}	2μm
Q_{13},Q_{15}	300μm	Q_{13},Q_{15}	10μm	Q_{14}	1.2μm
Q_{14},Q_{16}	10μm	Q_{14},Q_{16}	5μm	Q_{15}	12μm
Q_{17}	5μm	Q_{17}	1.5μm	Q_{16}	1.2μm
Q_{18}	40μm	Q_{18}	12μm	Q_{17}	30μm

*Aspect ratio (W/L), where L=1.2μm.

IV. Results and Discussion

All simulations are developed considering a load C_L=52pF at 1MHz. In Fig. 3, the voltage transfer curves of the p-

GaN comparators are presented. The Reference Voltage (V_{ref}) increases from 3 to 6V with a step size of 0.5V. The reference voltage range was selected considering the threshold voltage of the LV HEMT. Therefore, for V_{TH} lower than 3V, the transistors of the input stage cannot operate. On the other hand, for reference voltage values greater than 6V (close to V_{DD}), the transistors work in saturation region and the circuit is not sensitive to the changes in V_{in}. T_1 shows an operating voltage range of 2.8-4.3V. The lower output voltage is 80mV and the higher output voltage has a value of 6V when V_{ref} is lower than 4.5V. For superior V_{ref} values, the V_{OH} starts to drop. T_2 and T_3 have an operating voltage range of 2-5V and 2.5-6V respectively. The simulations demonstrated that the proposed comparators can reach the desired V_o, it can be seen in Table II. Additionally, T_1 has the best linearity performance, however it presents narrow input voltage comparison range compared with T_2 and T_3.

TABLE II
OUTPUT VOLTAGE *

Parameter	Units	T_1	T_2	T_3
Lower Output Voltage (V_{OL})	[mV]	80	150	100
Higher Output Voltage (V_{OH})	[V]	6	6.08	6.1

* Test conditions: $f = 1MHz$, $C_L = 52pF$.

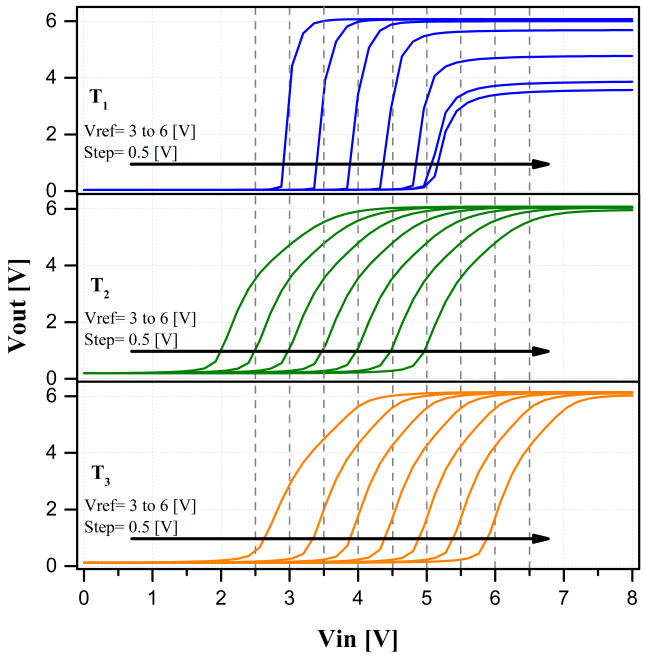

Fig. 3. Voltage transfer curves of the proposed p-GaN comparators

Figure 4a presents the Rising Time (t_r) and Fig. 4b illustrates the Falling Time (t_f) under temperature variation from 27°C to 250°C. To measure these transition times, a criteria of change in the output from 10% to 90% was considered. In Table III, t_r and t_f at 27°C are presented. T_3 exhibits fast rising and falling times achieving t_r=0.83ns and t_f=0.89ns. As expected with the increase in temperature the rising and falling times also increase. Despite the fact that T_2 presents rising/falling times shorter than the T_1, this topology still has narrow input voltage comparison range next to T_3. During temperature variation, T_3 presents best performance in transient analysis, it means shorter transition times than T_1 and T_2.

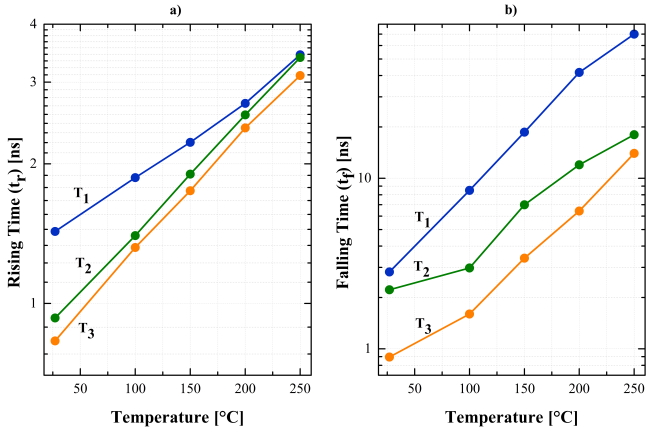

Fig. 4. a) Rising time b) Falling Time, $V_{DD} = 7V$, $f = 1MHz$, C_L=52pF

TABLE III
RISING AND FALLING TIME*

Parameter	Units	T_1	T_2	T_3
Rising Time (t_r)	[ns]	1.43	0.93	0.83
Falling Time (t_f)	[ns]	2.82	2.22	0.89

* Test conditions: $f = 1MHz$, $C_L = 52pF$, 27°C.

On the other hand, Fig. 5 shows the Propagation Delay Rising Time (t_{pdr}) and Propagation Delay Falling Time (t_{pdf}) of the comparators considering temperature variation. The propagation delay time is measured when the output voltage reaches 50% of its value with respect to 50% of the input voltage value. T_3 shows the lower value of rising/falling propagation delay times reaching t_{pdr}=1.47ns and t_{pdf}=1.57ns respectively (see Table IV).

TABLE IV
PROPAGATION DELAY TIME*

Parameter	Units	T_1	T_2	T_3
Propagation Delay Rising Time (t_{pdr})	[ns]	2.52	4.25	1.47
Propagation Delay Falling Time (t_{pdf})	[ns]	2.55	2.11	1.57

* Test conditions: $f = 1MHz$, $C_L = 52pF$, 27°C.

Furthermore, not only propagation delay times are crucial in the performance of p-GaN HEMT comparators but also the power consumption during operation. The Total Power (P_{total}) of the comparator comes from two sources: static and dynamic losses. The first losses are due to the quiescent current and the voltage supply. Meanwhile, dynamic losses are associated with switching frequency, handled load (high voltage p-GaN

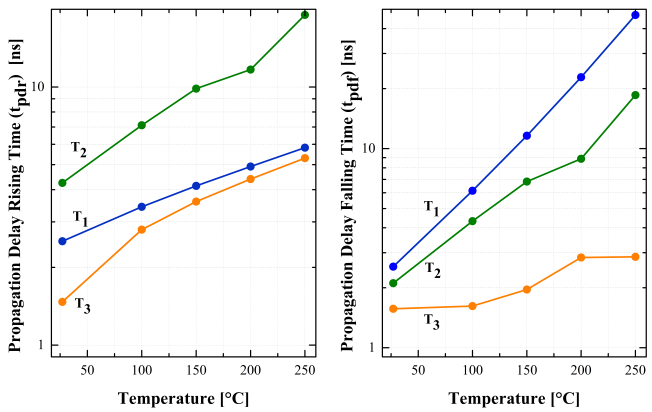

Fig. 5. a) Propagation delay rising time b) Propagation delay falling time, V_{DD}=7V , f=1MHz, C_L=52pF.

HEMT), and voltage supply. To calculate the dynamic power consumption [15] see (1):

$$P_{dynamic} = C_L * f_s * V_{DD}^2 \tag{1}$$

To analyze the trade-off between the power dissipated and the speed of the proposed circuits, the Figure of Merit called Power-Delay Product (PDP) is used [15] (2):

$$PDP = P_{total} * t_{pd,avg} \tag{2}$$

where, $t_{pd,avg}$ is the average of rising and falling propagation delay times and is equal to $(t_{pdr} + t_{pdf})/2$. The Fig. 6 shows the Power-Delay Product of three comparators. PDP-FoM is measured in terms of energy. The best performance has the third comparator (cross-coupled latch). It reaches a PDP between high and low transitions of 15.33pJ. Meanwhile, T_1 and T_2 show poor PDP characteristics, around 3 and 4 times larger than T_3.

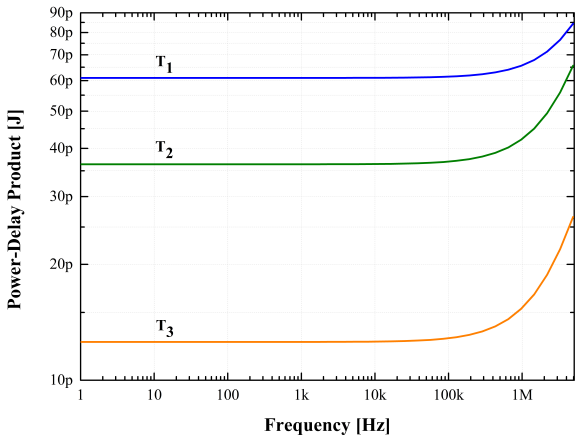

Fig. 6. Power-Delay Product of proposed p-GaN Comparators

V. Conclusion

Three new comparator topologies were proposed using E-mode p-GaN HEMT PDK. The circuits were simulated and analyzed under temperature and frequency variations. T_3 presents wider input voltage comparison range, faster turn on/off transitions and lower PDP, however it presents low linearity, which can be improved by working on the bias point of the comparator. As observed, to meet the design requirements, a trade-off between circuit speed, consumed power, linearity, and input voltage comparator range must be achieved according to the application.

Despite the challenge that the lack of a P-type device implies, the results demonstrated the feasibility of monolithic integration of low voltage circuits and GaN HEMT power devices for high power applications and with a large range of performance following the need of the circuit designer.

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