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Keywords

«LVDC», «AC-DC Converter», «Short circuit», « Fault tolerance », « Thermal model »

Abstract

In Low Voltage Direct Current (LVDC) grids DC short circuits can generate very high currents and huge stress for electronic power converters. Assessing their withstanding capabilities is critical. The present paper proposes to couple a thermal and electrical model of an AC/DC converter. This method allows to solve coordination issues between protection selection and converter sizing, as well as ensuring a reliable protection whatever the distance the fault occurs.

Introduction

In the recent decades, the development of distributed energy resources, such as solar panels and Energy Storage Systems (ESS), coupled with the increase of native DC consumers leads to consider more and more the creation of a Low Voltage Direct Current (LVDC) grid. Unlike traditional AC distribution grid, LVDC networks offer higher transmission capability and efficiency [1], [2], while allowing at the same time a high compatibility between production and consumption [3].

Despite these advantages, electrical safety is often referred in literacy as a barrier to wider deployment. Indeed, the behavior of a DC short-circuit is very different from that of an AC short-circuit., due to the use of capacitors in VSC-based converters which discharge almost instantaneously in the fault. In addition to this rapid evolution of the short-circuit, there is the absence of a zero-crossing of the current: thus a current interruption necessarily generates an electric arc. Therefore to ensure safety, a fast and selective protection device is needed [2], [4]. Many different propositions can be found in the literature [2], [5]–[7]. Among them, a fuse-based protection scheme allowing both a fast and selective reaction, as well as a cheap product, is promising [8].

However, the request for a fast protection device is not enough: there must be a constraint on the maximal tripping time. In the absence of international standards, this constraint is most of the time omitted. In this paper, we propose to use an electro-thermal modeling of commonly used low voltage AC-DC converters to determine the maximum tripping time of fuses: the aim being to avoid a destruction of the converter during a DC short-circuit, because of the overcurrent riding though the converter free-wheel diodes.

Electro-Thermal Modeling

The model used for simulations is represented in Figure 1. The choices made to determine parameters are explained in the following.

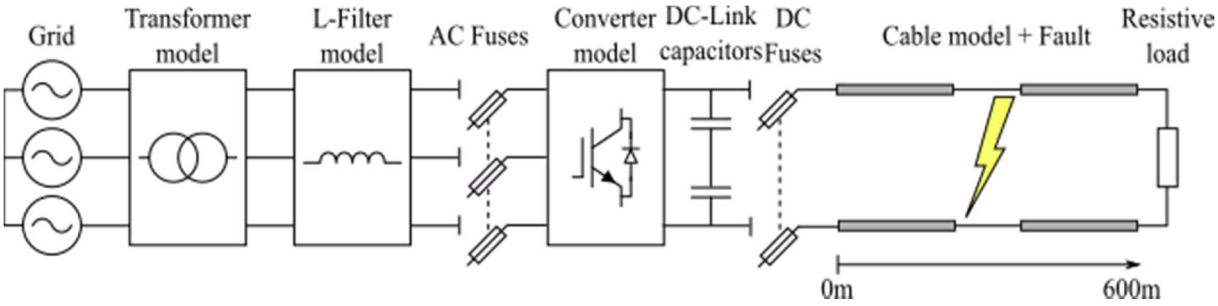

Figure 1 : Electric circuit of the studied low voltage system

AC Grid

In order to model the distribution grid feeding the AC-DC converter, it has been chosen to use a representation on the secondary side of the MV/LV power station transformer. Consequently, the AC grid is represented by a three-phase 400 V line-to-line voltage source, while the transformer is represented by its short-circuit impedance on the secondary side. This impedance is composed of an inductance in series with a resistor, whose values are in Table 1.
The parameters given correspond to a 400 kVA MV/LV transformer, widely used in urban area to create LV distribution grid. The international standard IEC 60076 has been used to determine its parameters.

Regarding AC cables, they are not represented because of the location of the AC-DC converter in the LV substation, or at least very close.

Table 1 : Grid parameters

Transformer	Primary voltage	20 kV
	Secondary voltage	400 V
	Short-circuit voltage	4 %
L-Filter	Inductance	2 mH
	Resistance	53 mΩ
DC-link Capacitor	Capacitance	1500 µF
	Resistance	61 mΩ
DC Cable [9]	Linear inductance	0,071 Ω/km
	Linear Resistance	0,124 Ω/km
	Length	600 m
Fault	Location	0 – 600 m
	Impedance	1 mΩ
Load	Power	40 kW
	Resistance	14 Ω

Table 2 : Converter requirements

Apparent power	40 kVA
AC grid line-to-line voltage	400 V
RMS phase current	58 A
DC-link voltage	750 V [10]
Sine-triangle modulation with 1/6 added third harmonics	
DC voltage ripple	5 %
THDI	8%
Grid frequency	50 Hz
Carrier frequency	3 kHz
Maximum junction temperature	175 °C
Ambient temperature	40 °C

Converter

Electrical parameters

A significant issue for a LVDC distribution grid is power reversal. Indeed, usually an injection of power in a LVDC grid is immediately absorbed by the system and leads to a decrease of power coming from the AC grid. However, if power generation supplants power consumption, there is a need for a power reversal in the DC grids, which means reversing intensity or voltage. In view of this constraint, the

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converter interfacing AC and DC grids must be a Voltage Source Converter (VSC). Power reversal being facilitated thanks to this technology, because it requires only an intensity reversal, unlike Line-Commutated Converters (LCC), which require a voltage reversal [11]. This second option being time-consuming due to the zero-crossing needed and can cause damages on cable polymeric insulation. In addition, VSC has high degree of flexibility , as well as an inbuilt ability to control both its active and reactive power, which makes it more useful in congested urban power grid area [12]. Finally, DC loads require most of the time a constant voltage. This can be achieved easily through a VSC, whereas a LCC would be more interesting for point to point lines.

Among available VSC topologies described in the literature[13]–[16], the two most promising and widely studied for low voltage applications are the Two-Level Voltage Source Inverter (VSC2L) and the Three-Level Neutral Point Clamped Inverter (NPC3L), represented respectively on Figure 2 and Figure 3. Whereas VSC2L is preferred due to its lower number of semiconductors and therefore conduction losses, NPC3L allows a better energy quality thanks to its greater number of voltage level. Thus, both topologies are studied in the paper, due to their complementary.

Figure 2 : Two-Level Voltage Source Converter (VSC2L) topology

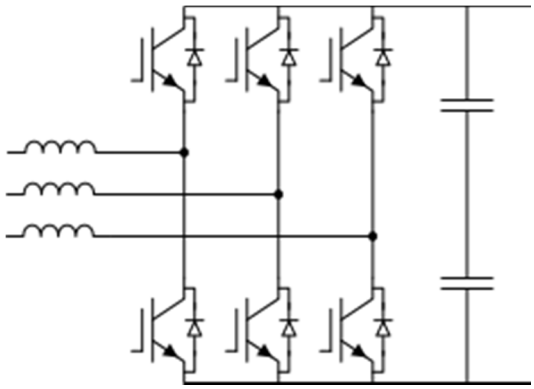
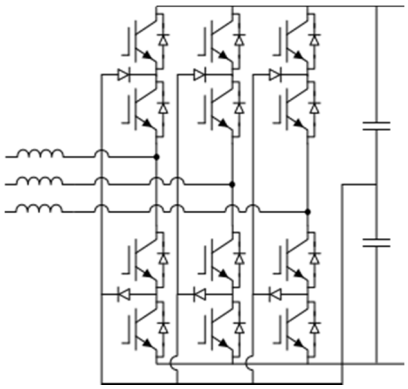


Figure 3 : Three-Level Neutral Point Clamped Converter (NPC3L) topology



As regards the power modules composing the converter, they have been chosen to meet the requirements described in Table 2. Two references have been selected for each topology: one reference with a rated RMS current of 75 A, whereas the other is designed for a current of 150 A. Indeed, rated current values being standardized in manufacturer's catalogue, the closest one from our application was 75 A. The second reference correspond to an oversizing of the converter: its rated current is three times higher than the one needed in our application in steady state. The aim being to study influence of oversizing on the converter during a short circuit.

Finally, the sizing of the DC-link capacitor has been performed using data given in Table 2 and using the method described in [17]. In order to reach a standardized capacitance value, that is to say 750 µF, it has been necessary to increase slightly the calculated value, which is advantageous in our application: it ensures less voltage oscillations from the DC bus. The creation of a middle point required to split the capacitor in two serial one, resulting in an increase of the capacitance. The Equivalent Serial Resistance (ESR) modelling the different dissipative effects of the capacitor is made thanks to the manufacturer's datasheet.
The AC filter is designed to get Total Harmonic Distortion (THD) from current smaller than 8%. Although IEC 61000-3-12 advises a maximal 13% THD, this constraint has been strengthened to take into account both source and load operation of the converter which are covered by the standard. Because L-filters offer a constant attenuation of -20 dB/decade over the whole frequency range [18] and studied topologies have similar dominant harmonics, the designed L-filter is the same for both converter topologies. Its value, as well as its internal resistance, are given in Table 1.

Thermal parameters

Another important aspect of the model is the thermal equivalent circuit. It describes the physical structure of a component in terms of thermal transitions from the junction to the external environment. Each transition consists of a thermal resistor and a thermal capacitor, as represented on Figure 4.

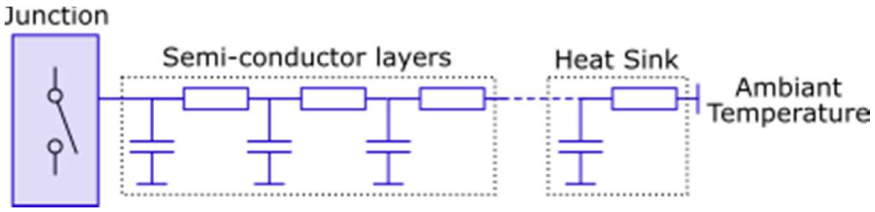


Figure 4 : Example of a Thermal Equivalent Circuit using Cauer representation.

In our model, each diode and IGBT transistor has several semi-conductor layers (up to 7 layers) before being linked together and connected to the external environment using a heat sink. This model assumes a radial heat exchange: there is no direct heat exchange between junctions.

Semi-conductor layers values are given by the manufacturer's datasheet and are synthetized in Table 3 and Table 4. In the case of NPC3L, it is necessary to make the difference between upward and downward components on each arm, due to a difference in solicitation. Therefore, they are indicated respectively as "Boost" and "Buck".

Table 3 : Thermal resistance of semi-conductor layers for used components

Component	Current (A)	R_1 (K/W)	R_2 (K/W)	R_3 (K/W)	R_4 (K/W)	R_5 (K/W)	R_6 (K/W)	R_7 (K/W)
IGBT	75	0,04052	0,1552	0,1499	0,08419	0,04511	0,02287	0
Diode		0,05493	0,1305	0,2066	0,09947	0,05086	0,03518	0
IGBT	150	0,03327	0,0131	0,0572	0,09906	0,1837	0,05764	0,02414
Diode		0,06346	0,191	0,1239	0,06974	0,04478	0,01864	0
IGBT Boost	75	0,07293	0,2385	0,2953	0,221	0,1007	0,04771	0
Diode Boost		0,1249	0,3089	0,3519	0,1682	0,1227	0,03868	0
IGBT Buck		0,07293	0,2385	0,2953	0,221	0,1007	0,04771	0
Diode Buck		0,099	0,3013	0,3943	0,2655	0,1052	0,06239	0
IGBT Boost	150	0,04211	0,1276	0,229	0,1354	0,07859	0,02721	0
Diode Boost		0,06071	0,2016	0,2916	0,1073	0,04882	0	0
IGBT Buck		0,04539	0,1216	0,1974	0,109	0,07095	0,02568	0
Diode Buck		0,09502	0,3259	0,5048	0,2211	0,1156	0,0377	0

Table 4 : Thermal capacitance of semi-conductor layers for used components

Component	Current (A)	C_1 ($J.K^{-1}$)	C_2 ($J.K^{-1}$)	C_3 ($J.K^{-1}$)	C_4 ($J.K^{-1}$)	C_5 ($J.K^{-1}$)	C_6 ($J.K^{-1}$)	C_7 ($J.K^{-1}$)
IGBT	75	0,02533	0,0714	0,1637	1,946	19,6	157,3	0
Diode		0,01103	0,0452	0,066	0,6489	7,965	86,85	0
IGBT	150	0,01585	0,1137	0,0804	0,1917	0,4174	9,863	102,2
Diode		0,03296	0,0660	0,2213	2,208	25,57	275,7	0
IGBT Boost	75	0,00611	0,0263	0,0485	0,1858	3,297	42,91	0
Diode Boost		0,01407	0,0280	0,1015	0,6498	6,609	96,27	0
IGBT Buck		0,00611	0,0263	0,0485	0,1858	3,297	42,91	0
Diode Buck		0,00711	0,0187	0,0394	0,1426	2,667	39,71	0
IGBT Boost	150	0,0441	0,1136	0,2727	1,052	14,54	135,2	0
Diode Boost		0,02776	0,0748	0,2489	3,86	62,71	0	0
IGBT Buck		0,08031	0,0939	0,2927	1,257	13,85	154,5	0
Diode Buck		0,0328	0,0506	0,1394	0,7664	8,238	118,1	0

As regards heat sink thermal capacitance and resistance, they are calculated from the geometry described in Figure 5. The heat sink is divided in two parts : the base and the straight fins. Thermal resistance in the base is 0,006 $K.W^{-1}$ and is calculated using (1), assuming a power junction large enough to allow a perpendicular heat exchange [19]–[21].

$$R_{th\ base} = \frac{e}{\lambda . S} \quad (1)$$

Where parameters are:

- e : base thickness (m)
- λ : thermal conductivity ($W.m^{-1}.K^{-1}$)
- S : base surface (m^2)

Fins equivalent thermal resistance is 0,0043 $K.W^{-1}$ is calculated using method described in [19], as well as Nusselt correlation defined in [22]. The fan, used to create the forced convection, has an airflow of 115 $m^3.h^{-1}$. Because the thermal operating range of transformers is -25°C to 40°C, according to IEC 60076, thermodynamic air properties are given at 40°C in Table 5.

Table 5 : Aluminum and 40°Cair thermal properties

	T (K)	ρ ($kg.m^{-3}$)	μ ($kg.m^{-1}.s^{-1}$)	c_p ($J.kg^{-1}.K^{-1}$)	λ ($W.m^{-1}.K^{-1}$)
Air	313	1,126	1,91E-05	1006	0,0272
Aluminum		2698,9		897	237

The dynamic regime for the heatsink is taken into account by calculating the heat capacities for each element using equation (2) and assuming one-dimensional heat flow [21], [22]. It results in thermal equivalent thermal capacities in the heat sink base and fins are respectively 68,63 $J.K^{-1}$ and 239,67 $J.K^{-1}$.

$$C_{th} = c_p . \rho . e . S \quad (2)$$

Where Table 5 gives aluminum thermal parameters c_p and ρ, while e and S are respectively thickness and section through which the heat flows.

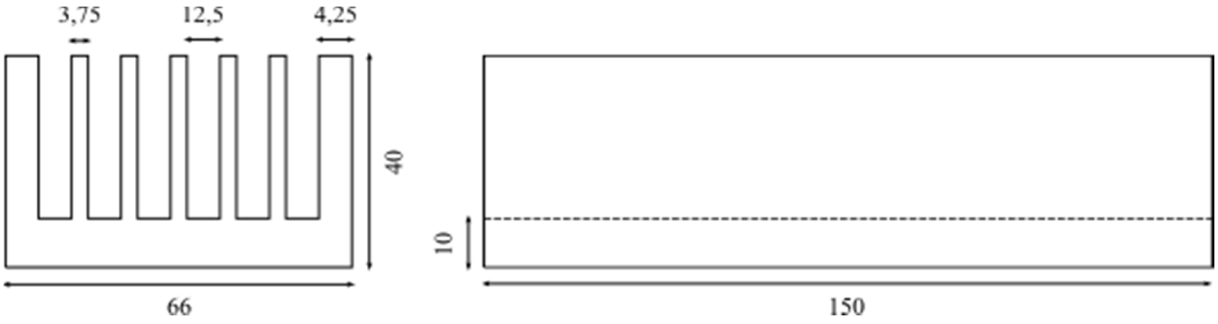


Figure 5 : Front (left) and side (right) view of the heat sink geometry including dimensions in mm

DC Grid

We assume a radial topology for the LVDC grid to allows an exploitation similar to that of MV and LV AC distribution grids. Environmental perturbation due to earth current are limited by a metallic return and DC voltage constraint on the transformer is limited by using symmetrical poles.

In order to understand the impact of the fault location on the fault current, a 600 m long cable has been modelled. Each pole is modelled as an independent conductor and split in two sections, represented each by an inductance in series with a resistance. Parameters are given in Table 1. If linear inductance and resistance are required to understand transient phenomena, it is not the case of linear capacitance. Strongly linked to unknown environmental parameters (earth composition, insulation…), it is neglected in the model [8]. The cable length is based on the maximal theoretical length of AC cable in the distribution grid, assuming a ±10% voltage variation [23] and a constant impedance cable [24] : the aim being to provide a radial distribution grid as long as in AC.

The fault impedance is a 1 mΩ resistance, so that the maximal short-circuit current is provided by

capacitor discharge[8], [25], [26], while being coherent with reality. Finally, the load is a 14 Ω resistance, in order to be at the rated current when a fault occurs between cables.

Protection scheme

Fuse location

Two protection strategies are available in the literature. First and foremost, it is possible to keep the same protection scheme as in AC with a fuse located at the beginning of the DC feeder[27]–[30]. This strategy allows to benefit from the capacitors discharge to react quickly, but the current to interrupt is high [5], [8], [25] which could prevent the fuse to blow up. In order to avoid this phenomena, another method would be to insert a fuse on converter AC side [31], [32]. However tripping time are higher which could prevent an efficient protection of the converter. Therefore, in this paper both strategies are implemented and compared. Fuses are located as illustrated in Figure 1.

Fuse type

Due to their low cost, simple operation and high reliability, fuses have been used since the early days of distribution networks. Nowadays, LV feeders are still protected by fuses [23]. Although they have undergone considerable evolution since their early days, to meet requirements of different application, all have the same decisive features. The key part is the fuse design . Made from a high conductivity material, it includes a number of reduced sections, commonly called “necks”, “notches” or “weak spots”. Those elements are surrounded with an arc-quenching material, generally sand quartz that blows out the arc when the reduced sections melt and “burn back” to open the circuit. This function gives fuses their current-limiting ability. To contain the sand quartz, an insulated container, called the fuse body, is made of ceramic or engineered plastic. Finally, there are copper or aluminum end connectors to connect the fuse element to the circuit it protects.

Among available fuses, special ones are dedicated to DC applications. Often referred as “high-speed”, “ultra-fast” or “semiconductor” fuses, they are specially designed to minimize I^2t, peak current let-through and arc voltage. To achieve this goal, their fuse elements have weak spots of a different design than a similarly rated industrial fuse and have higher operating temperatures to be compatible with power electronics components.
As regards industrial fuses, they are categorized by IEC 60269 according to their function and their operational classes:

- The first letter defines the function class:
  - a: Partial range protection (only short-circuit)
  - g: Full range protection (short-circuit and overcurrent)
- The second the object to be protected:
  - G: Cable and line protection
  - M: Switching device protection in motor circuits
  - R: Semiconductor protection
  - L: Cable and line protection, in accordance with the old and no longer valid standard
  - B: Mine equipment protection
  - Tr: Transformer protection
  - PV; Photovoltaic protection

In view of the available devices, only three fuse types can be used in a LVDC grid: aG, gG for AC grid and semiconductor fuse for DC grid. As regards their current range, manufacturers recommend avoiding a current load higher than 90% of the fuse range[33]–[35]. Consequently, from standard fuse rating, available fuse rating for DC side are 63A and 80A, whereas for AC side is at least 80A.

Tripping time assessment

Among parameters allowing to characterize a fuse, the I^2t value is one of the most significant. Also called joule integral, it expresses the amount of energy transmitted to the system before the fuse opens, although strictly speaking it is not an energy. Indeed, its unit is A^2s and not joules. Usually, two I^2t value

are defined: the pre-arcing (or melting) value and the total I^2t value. The first one corresponds to the required amount of "energy" to start the melting of the fuse, whereas the second corresponds to the total amount of "energy" transmitted between the fault start and the fuse opening. This last value is generally available in fuse datasheet.
Consequently, a fuse blowing up during a short-circuit can be estimated by dynamically calculating the I^2t value transiting through it, in integrating the square of the current. When this value reaches the manufacturer value, we assume that the fuse blows and clears the circuit instantaneously. The arcing time is neglected before the melting time of the fuse.

Results & discussion

Overall behavior

Short circuits between the positive and the negative pole resulted in both topologies having the same behavior during the fault. This process is well described is the literature [25], [26], [36] and can be decomposed in 3 steps:

1. Voltage drops and capacitors current increases in a few milliseconds.
2. Line inductances discharge and diodes are in freewheeling mode.
3. AC grid feeds the fault through the diodes.

The transition from the first to the second step requires two conditions. Firstly, IGBTs must be switched off. This is achieved through their gate signals: if the DC voltage drops below 85% of its nominal value, the IGBTs are blocked. The aim is to prevent them from conducting a high current, insofar as they are the less resilient components of the converter. Secondly, bus voltage needs to reach a zero value. Under this condition, current from inductances discharge through them, while capacitors end their own discharge. Consequently, fault current is higher and longer than those provided by capacitors discharge, as illustrated in Figure 6, and implies a supplementary constrain: the converter destruction can be achieved without the participation of the AC grid, because of the inductances discharge.

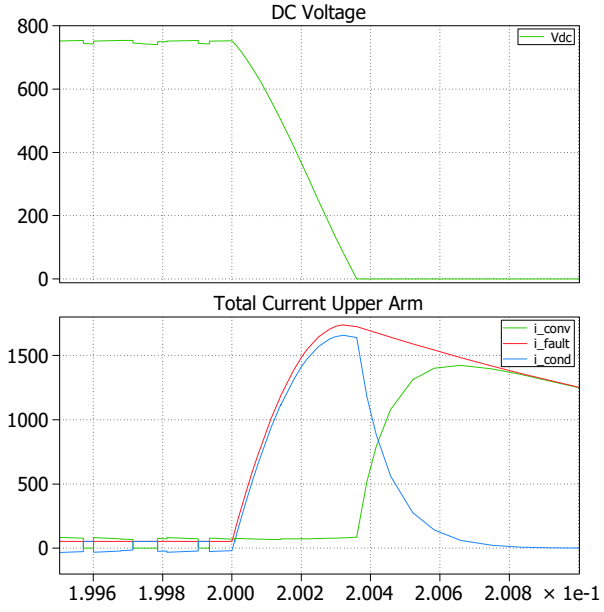


Figure 6: DC bus voltage and current in the upper node of the converter for a fault at 150m

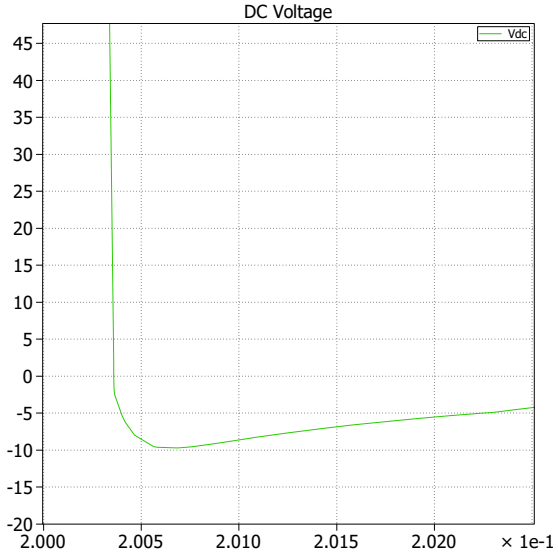


Figure 7: Zoom on DC bus voltage zero-crossing for a fault at 150m using real diodes

Focusing on DC voltage evolution, it remains null until the AC grid starts to feed the fault. Indeed, like in other articles, diodes are considered as perfect: this absence of resistors leads to a forced zero voltage during this step. Diodes voltage cannot become positive, because it would mean they stopped the fault which is impossible in forced conduction.
This uses of perfect diodes leads to another limitation of the model. Unlike physical observation of the phenomena, the inductance discharge current goes only though one arm of the converter, resulting in an overestimation of diodes critical time. In order to solve this limitation, diode model has been corrected

to include a voltage source V_f in series with a resistor R_{ON} during the conduction. Both values are deduced from the characteristic $V_{CE} = f(I_C)$ of the manufacturer's datasheet.

As illustrated in Figure 7, real diodes leads to an inversion of the DC voltage bus, because the voltage constrain on the diodes has been relaxed. A new equation linked DC voltage V_{DC}, current through the converter i_{conv} and diodes parameters appears.

$$i_{conv\_VSC2L} = 3\frac{V_{DC} - 2V_f}{2R_{ON}} \quad (3)$$

$$i_{conv\_NPC3L} = 3\frac{V_{DC} - 2(V_{f_{buck}} + V_{f_{boost}})}{2(R_{ON_{buck}} + R_{ON_{boost}})} \quad (4)$$

In (3) Vf and R_{ON} correspond respectively to the VSC2L diode forward voltage and conduction resistor, as defined previously. Because NPC3L topology has three asymmetrically operated diodes per arm, two different type are defined. Buck diodes correspond to the diodes in the upper part of the arm and the clamped diodes, whereas boost diodes are in the lower part of the arm. Therefore, in equation (4) R_{ONbuck} and R_{ONbuck} correspond respectively to these different diodes used in each arm.

Fuse time assessment

As illustrated on Figure 8 and Figure 9, the fault location has a direct influence on the time required to blow a fuse, as well as the acceptable time for diodes. This is due to the line inductance: the more it increases, the more the current peak decreases which leads to an increase of the fuse blowing time. However, this evolution is not symmetric according to which fuse are considered. For AC fuse it is a linear evolution, insofar as only AC grid current goes through the fuse and this current has an almost constant RMS value. On the contrary, DC fuses benefits from the capacitors discharge which allows them to blow faster if the line is small enough. In our simulation the 80A DC fuse has a 1750 A².s thermal constraint, whereas the 80A aR fuse has a 1250 A².s thermal constraint. Despite this difference, the DC fuse succeeds in melting first thanks to the fast capacitor discharge. Unfortunately, this advantage disappears as the inductance increases and at the end of the line the roles are reversed.
An inflection point can be observed in the fuse melting curves, it corresponds to the critical distance from which the beneficial effect of the capacitors gradually disappears until it reaches a linear trace similar to that of AC fuses. These critical distances value 150m and 350m respectively for the 80A and 63A DC fuses.

As regards diodes, two behaviors can be observed. First and foremost, there is a linear destruction time for the 150A modules. In both cases, it can be linked to the module thermal capacitances. Indeed, the 150A modules have high thermal capacitance which allows them to overcome the inductance discharge. Unlike 75A modules which initially experience the discharge of the inductances before the phenomenon is mitigated by the remoteness of the fault and the increase of the inductance. This is noticeable by to the apparition of inflexion point at 150m and 225m on Figure 9.

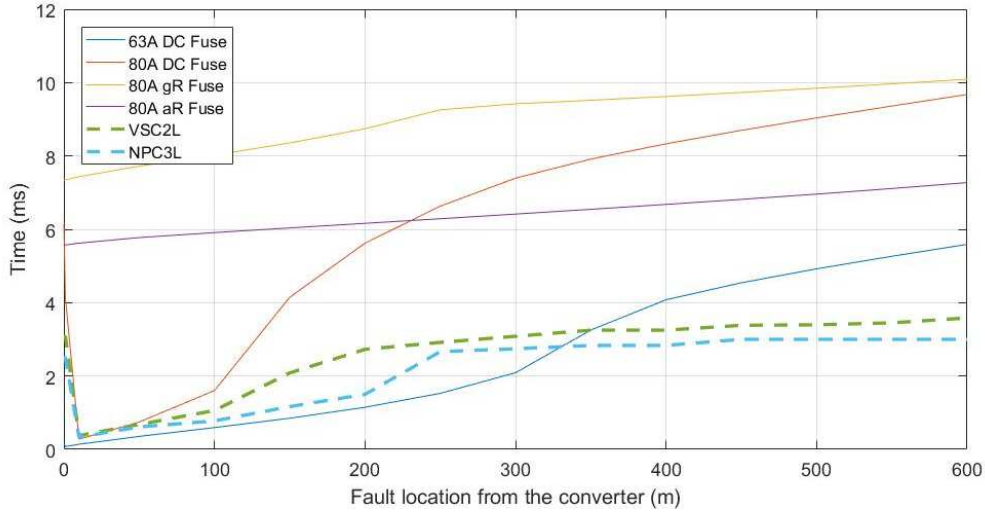


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Figure 8 : Melting time of fuses and most critical diode as a function of the location of the short-circuit for 75A VSC2L and NPC3L converters

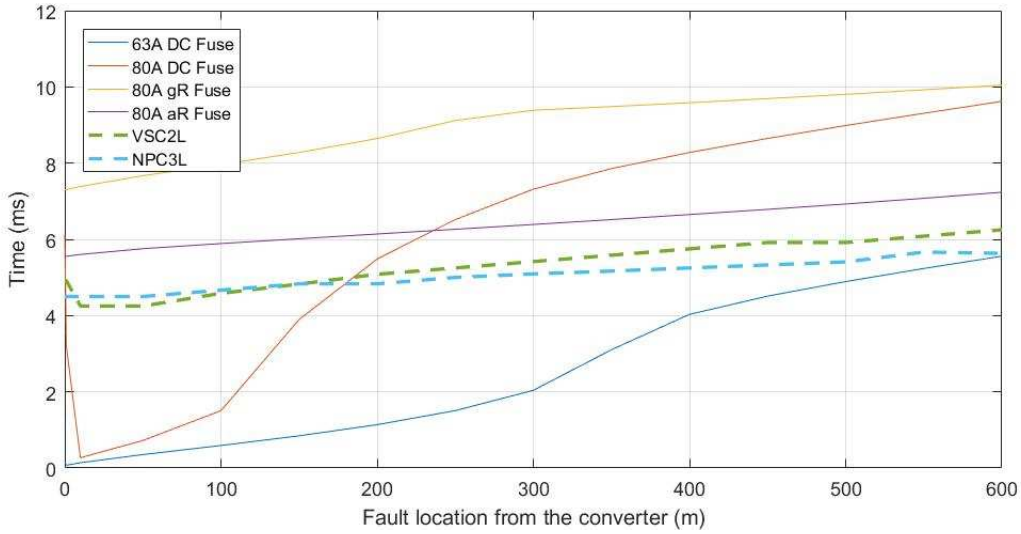

Figure 9: Melting time of fuses and most critical diode as a function of the location of the short-circuit for 150A VSC2L and NPC3L converters

According to these graphs, it is possible to determine the best coordination between available fuses and power modules by applying the following principle: module curbs must always be above fuse curbs, which means that fuses must blow up before a diode reaches its critical temperature. This coordination is reached by using a 150A power module with a 63A DC fuse,

Conclusion

The thermo-electrical model built allows to highlight the effectiveness of fuses to protect a power converter: thanks to the discharge of the DC-link capacitors during a fault, DC fuses offer better blowing time than AC fuses. However, only the combination of an oversized power module with a low-size fuse allows an efficient protection of the converter. Indeed, the inductance discharge after the DC bus voltage zero-crossing can generate a thermal constraint on diodes before a fuse react. This phenomenon can be mitigated by a fault remoteness or an inductance increase but leads to slower fuse reaction. From the modeling point of view, this paper highlights the necessity to consider conduction parameters from diodes in order to have a physically coherent model.

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