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**Research, Development and Improvement of
Manufacturing Technology of Integrated Transducers
and Sensors of Energy Parameters, Including for Control
and Regulation of Parameters of Technological Processes
of MEA Production (Flexible Manufacturing Systems
(FMS), Flexible Manufacturing Modules (FMP), Etc.).
TECHNICAL REPORT on the theme 0-706-88. 1990**

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HAL Id: hal-04173202

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**Scientific and Research Technological Institute of
Instrument Engineering**

**TECHNICAL REPORT
on the theme 0-706-88**

**Research, Development and Improvement of Production Technology of
Integral Transducers and Sensors of Energy Parameters, Including
Control and Regulation of Parameters of Technological Processes of
MEA Production (Flexible Manufacturing Systems (FMS), Flexible
Manufacturing Modules (FMP), Etc.)**

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
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Abstract

The report presents the results of research and development on the design and manufacturing technology of integrated silicon transducers for mechanical systems. The set of technical solutions, supported by research and development, includes the following key points: The miniaturization limits have been achieved within the anisotropic chemical etching technology on standard substrates used in planar technology; The results on expanding the temperature range of sensors with p-n junctions have significantly surpassed expectations, exceeding by more than 50°C; A technical solution for reducing the pressure limit, which restricts the use of sensors with semiconductor elastic elements, has been investigated, and these solutions have been obtained for the small class of sensors weighing less than 40 g; The system of technological solutions for the development and production of mechanical sensors is complemented by a group of plasma profiling processes that are crucial for aligning crystal shapes with lathe-machined components.

The conducted research allows for: Defining the scope of research and development aimed at creating various mechanical sensors, primarily including parametric series of pressure sensors for non-aggressive environments; Identifying the need for R&D in creating pressure resistance elements through hydraulic fluids for silicon elastic elements, investigating the long-term stability of sensor elements and connections; Provide mathematical support for calculating stresses in sensor housings under high pressures and vibrations; Exploring solutions to raise the upper limit of the working temperature range; Investigating methods for vacuum bonding silicon with the metal casing to create absolute pressure sensors.

I. INTRODUCTION

Quality of industry products, improvement of their technical characteristics at the modern stage of technology development is largely determined by the parameters of information-measuring systems, control systems and technical diagnostics. Practically, in all of the above systems, the link responsible for the functions of primary perception and transformation of information signals is the mechanical sensors ¹.

At the moment, these measurements are carried out by sensors with a large mass, low sensitivity, and high labor intensity of production. The structural and technological solutions used in the majority of sensors do not allow for a significant improvement in their metrological and operational parameters. Therefore, in the country and industry, efforts to create a new generation of miniature semiconductor sensors for mechanical quantities have become one of the main directions in a series of comprehensive programs for miniaturizing electronic and electrical equipment ².

In the current stage of development, the piezoresistive effect is considered the most accurate and widely used method for converting mechanical quantities into electrical signals. However, until now, efforts to create silicon-based piezoresistive integrated transducers (IPTs) have not addressed several issues regarding the expansion of their operational capabilities. These issues include concerns related to the characteristics of size and weight, operating temperature range, sensitivity to small mechanical inputs, and other factors.

Further miniaturization of IPTs will provide several advantages in various aspects. Compact sensors based on integrated circuit technology will significantly reduce the size of the entire measurement system, decrease errors during bench tests, and provide conditions closer to real-world operating conditions, thus

expanding the dynamic range of the sensors. Additionally, when miniature IPTs are manufactured in bulk, the specific production costs of sensor equipment are reduced.

II. EXPERIMENTAL STUDIES

A. Development of Test Microtransducers, Measurement Modules and Prototype Transducer

1) Designing IPT for Small Pressures

The measurement range, metrological, and operational characteristics of semiconductor mechanical sensors are largely determined by their elastic element (EE).

We propose a design of an integral piezoresistive transducer (IPT), in which EE combines the function of pressure-to-strain conversion in piezoresistors with mechanical decoupling of the latter from thermomechanical stresses occurring in the sensor-housing connection area (Fig.1).

The design is implemented by group methods of microelectronics technology, including its EE is formed by anisotropic chemical etching of the orientation of silicon wafers (001).

The elastic membrane has a stiffening rib in the form of a rectangular beam, the symmetry plane of which coincides with the symmetry plane of the membrane.

The effect of increasing the conversion accuracy and expanding the measurement range (EE) is based on three main points:

- 1) Reducing the effect of membrane stresses on the piezoresistor, by limiting the deflections of the membrane by the beam.
- 2) The more attenuated the transmission of membrane stresses to the surface, the greater the ratio of beam and membrane thicknesses.
- 3) There is a significant increase in the bending stresses to the beam surface as the neutral line shifted toward the membrane.

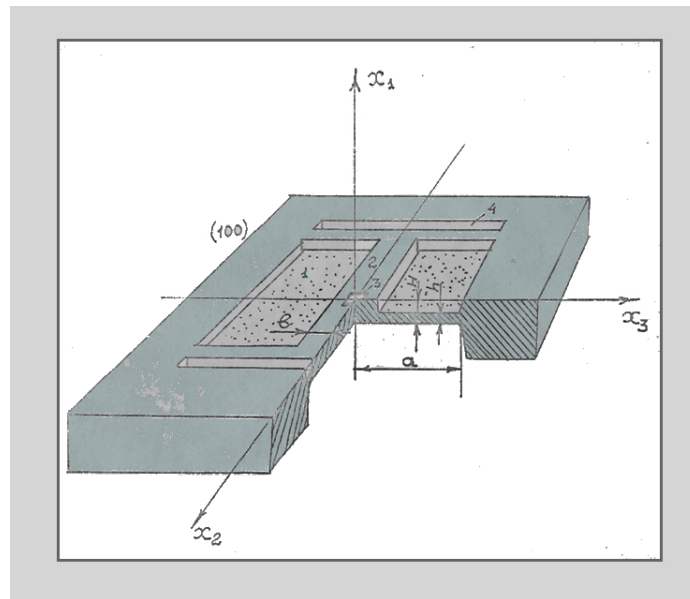


Fig. 1. Elastic element of the membrane-beam type with stress decoupling from the attachment side.

The membrane converts pressure into distributed load on a double-ended beam, on which longitudinal and transverse piezoresistors are located, connected in a bridge measurement circuit. The beam combines the membrane's stress with its own bending stresses, and in the area where the strain resistors are located, an increasing dependence of the difference between longitudinal and transverse stresses on pressure is achieved.

The reduction of the influence of the attachment on the conversion characteristic of the IPT is achieved, first, through mechanical decoupling, which is performed by the etched membrane providing a hinged attachment of the beam, and second, by placing the bridge measurement circuit at the geometric center of the EE, which is the most remote point from the attachment areas. Theoretical studies have made

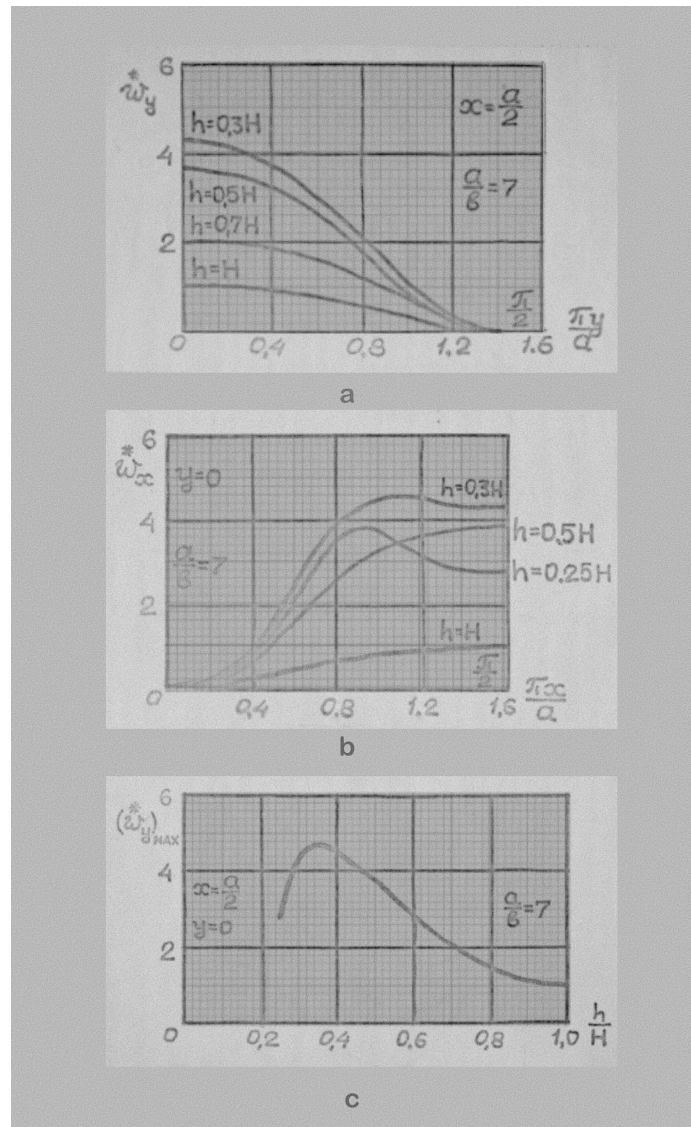


Fig. 2. Dependence of deflections on geometrical parameters EE .

assumptions of material isotropy for EE and linearity of the problem under consideration, allowing the application of the superposition method.

The objective of the research was to determine the stresses on the surface of EE and to find a potentially simpler method to solve this problem.

A plate with a uniformly distributed load is described by the differential equation.

$$\frac{\partial^4 w}{\partial x^4} + 2 \frac{\partial^4 w}{\partial x^2 \partial y^2} + \frac{\partial^4 w}{\partial y^4} = \frac{q}{D} \quad (1)$$

where $D = \frac{Eh^3}{12(1-\nu^2)}$ is the stiffness of the plate; ν - Poisson's ratio; E - Modulus of elasticity; h - thickness; q - uniformly distributed load (pressure); w - deflection of the wall at the point with coordinates (x, y) .

Boundary conditions for the model under study:

$$\begin{aligned} (w)_{x=0} = 0; \quad (w)_{y=\pm \frac{a}{2}} = 0; \quad \left(\frac{\partial w}{\partial x} \right)_{x=\frac{a-b}{2}} = 0; \quad \left(\frac{\partial w}{\partial y} \right)_{x=\pm \frac{a}{2}} = 0; \\ \left(\frac{\partial w}{\partial x} \right)_{x=0} = 0; \quad EI \left(\frac{\partial^4 w}{\partial y^4} \right)_{x=\frac{a-b}{2}} = D \frac{\partial}{\partial x} \left[\frac{\partial^2 w}{\partial x^2} + (2-\nu) \frac{\partial^2 w}{\partial y^2} \right]_{x=\frac{a-b}{2}} + q \frac{b}{2} \end{aligned}$$

where I is the moment of inertia of the beam cross section; a - side of the beach; b - width of the beam.

The solution of the diffeomorphic equation (1) for the deflections is as follows:

$$\begin{aligned} w = \frac{qa^4}{D} \cdot \left[\sum_{m=1,3,5,\dots}^{\infty} \left[A_m \left(\operatorname{ch} \frac{m\pi x}{a} - 1 \right) + (B_m + I_m) \frac{m\pi x}{a} \operatorname{sh} \frac{m\pi x}{a} + \right. \right. \\ \left. \left. + (D_m + H_m) \frac{m\pi x}{a} \operatorname{ch} \frac{m\pi x}{a} + (b_m - D_m) \operatorname{sh} \frac{m\pi x}{a} \right] \cos \frac{m\pi y}{a} + \right. \\ \left. + \sum_{n=1,3,5,\dots}^{\infty} F_n \operatorname{ch} \frac{n\pi y}{a-b} \left(\frac{n\pi y}{a-b} \operatorname{th} \frac{n\pi y}{a-b} - n\gamma \operatorname{th} n\gamma \right) \sin \frac{n\pi x}{a-b} \right] ; \\ \gamma = \frac{\pi a}{2(a-b)} \end{aligned}$$

The expression for the mechanical stresses in the surface layer EE surface layer looks like:

$$\begin{aligned} \sigma_x = q \left(\frac{a}{H} \right)^2 \left[f(y) + \frac{\nu}{1-\nu^2} \left(\frac{h}{H} \right)^3 \varphi(y) \right]; \\ \sigma_y = q \left(\frac{a}{H} \right)^2 \varphi(y) \end{aligned}$$

where h is the thickness of the plate ; H - total thickness of plate and beam;

$$\begin{aligned} \varphi(y) &= \left(\frac{H}{h}\right)^3 (1-\nu^2) 6\pi^2 \left\{ \frac{4}{\pi^2} \sum_{n=1,3,5,\dots}^{\infty} (-1)^{\frac{n-1}{2}} n^2 \gamma^2 F_n \operatorname{ch} \frac{n\pi y}{a-b} \left(n\gamma \operatorname{th} n\gamma - \right. \right. \\ &\quad \left. \left. - \frac{n\pi y}{a-b} \operatorname{th} \frac{n\pi y}{a-b} - 2 \right) + \sum_{m=1,3,5,\dots}^{\infty} m^2 \cdot [A_m (\operatorname{ch} m\alpha - 1) + (B_m + I_m) m\alpha \operatorname{sh} m\alpha + \right. \\ &\quad \left. + (D_m + H_m) m\alpha \operatorname{ch} m\alpha + (G_m - D_m) \operatorname{sh} m\alpha] \cdot \cos \frac{m\pi y}{a} \right\}; \\ f(y) &= -6\pi^2 \left\{ \sum_{m=1,3,5,\dots}^{\infty} m^2 \cdot [(A_m + 2B_m + 2I_m) \operatorname{ch} m\alpha + (B_m + I_m) m\alpha \operatorname{sh} m\alpha + \right. \\ &\quad \left. + (D_m + H_m) m\alpha \operatorname{ch} m\alpha + (D_m + G_m + 2H_m) \operatorname{sh} m\alpha] \cdot \cos \frac{m\pi y}{a} + \right. \\ &\quad \left. + \frac{4}{\pi^2} \sum_{n=1,3,5,\dots}^{\infty} (-1)^{\frac{n-1}{2}} n^2 \gamma^2 F_n \operatorname{ch} \frac{n\pi y}{a-b} \left(n\gamma \operatorname{th} n\gamma - \frac{n\pi y}{a-b} \operatorname{th} \frac{n\pi y}{a-b} \right) \right\}; \\ \alpha &= \frac{\pi(a-b)}{2a} \end{aligned}$$

For clarity and the possibility of evaluation calculations, the graphical dependence of mechanical characteristics on the main geometric parameters EE (Fig. 2 - Fig. 6) was obtained.

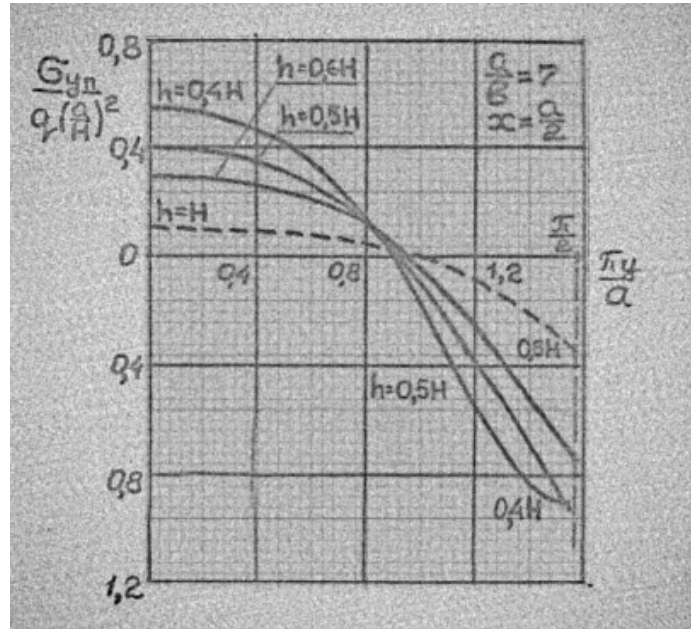


Fig. 3. Distribution of longitudinal stresses on the beam surface.

2) Designing IPT with Extended Operating Temperature Range

The upper limit of the operating temperature range T_{\max} of a monolithic IPT with an insulating p-n junction is determined by the conditions when the insulating resistance R_i^{p-n} of the junction reaches the critical value $R_{i_{\min}}^{p-n}$. At $R_{i_{\min}}^{p-n}$, the shunt effect of the resistance to EE in one of the measuring circuit

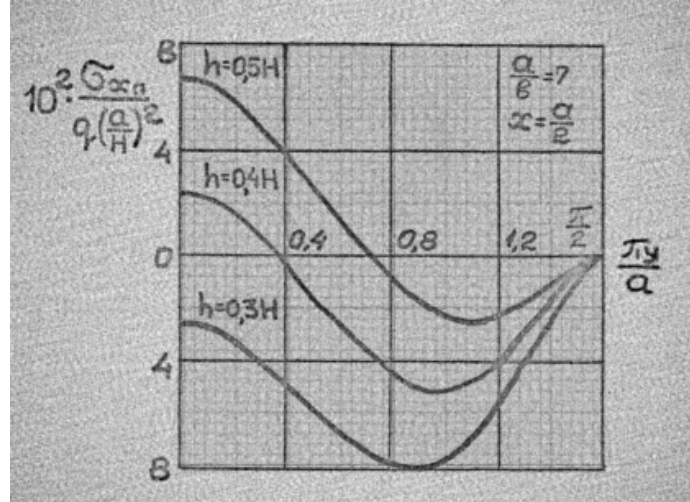


Fig. 4. Distribution of shear stresses on the surface along the beam axis.

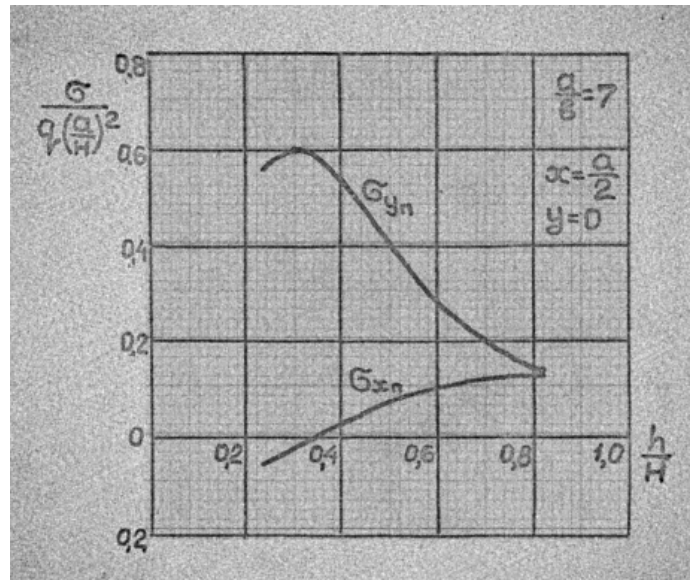


Fig. 5. Dependence of surface stresses of the center EE on the ratio of membrane and beam thicknesses.

(MC) arms changes the value of the transfer coefficient K_{mc} by 1% relative to the nominal value, equal to $K_{mc} = 10 \text{ mV/V}$. From ³, where IPT with piezoresistor resistance equal to $R_{ch} = 1000 \Omega$ was studied, the upper value of the range corresponds to temperature $T_{\max} = T_{\text{per}}$ when the reverse bias voltage p-n transition $U_{\text{rev}} = 5 \text{ V}$ has reverse current I_{rev} equal to $2 \cdot 10^{-6} \text{ A}$. For this IPT design, it is assumed that in the temperature range $T_{\min} \leq T \leq T_{\max}$ MC has lumped parameters, and the physical principle of conversion of mechanical matter into electrical signal is studied and undeniable. Therefore, modeling and experimental studies are related to the study of the temperature dependences in the range $(0 \div 300)^\circ\text{C}$ of the VAC parameter of the isolating p-n junction, which determines R_i^{p-n} the reverse current density $J_{\text{rev}}(T)$. The conversion characteristic will be as follows:

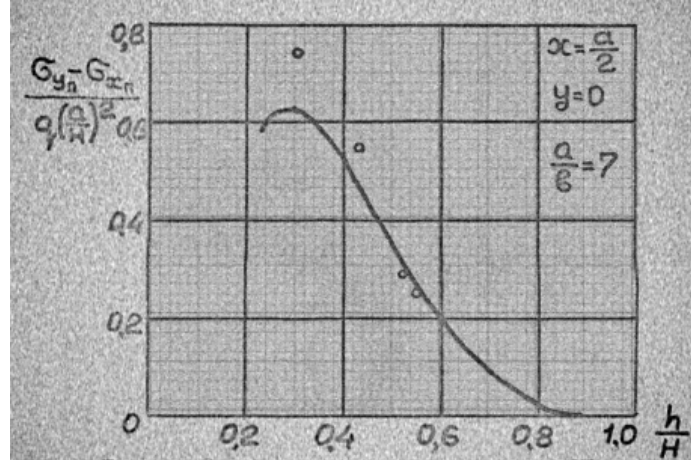


Fig. 6. Dependence of EE sensitivity on ratio of thicknesses.

Reducing the complementary temperature error IPT by approaching to zero the value and temperature dependence of the normalized null output K_{mc0} is possible if the following design requirements are met:

- minimizing the deviations of the electrical resistance IPT from the average values and the identity of their temperature characteristics;
- minimization of values and variances of the initial deformations of the elastic element in the areas of piezoresistor (PR) placement; identity of the temperature dependences of these values;
- equality of all thermal resistances in the heat sink chain $PR - EE - BR$;
- minimization of temperature gradient in the plane of PR placement on EE .

The deformation transducer design, which satisfies the above requirements, includes identical square contact pads with a size of b at the vertices of a square with a size of a . These contact pads are connected by four single-band PR width d_{ch} longitudinal ($R_{1,3}$) and transverse ($R_{2,4}$) piezoresistors (see Fig. 7). Contact pads and piezoresistive channels are created by local doping (boron doping) of the planar surface with an orientation of (001) of the monolithic monocrystalline silicon structure *RigidBase - ElasticElement* ($RB - EE$). The elements MC are located in the body EE , which is H_{ee} thick and is located at a distance of C from the base boundary, which is also H_w thick.

When the size of the elastically deformable part EE is greater than $0.2\text{ cm} \times 0.2\text{ cm}$, we can assume that the equality $\varepsilon_{x_2} \approx \varepsilon_{x_4} \approx \varepsilon_{x_0}$ holds, then for IPT , where $|K_{||}| \approx |K_{\perp}|$, from (3.1) the transformation characteristic will be:

$$\frac{V_{out}}{V_{in}} = 0.5 \cdot K_{||} \cdot \varepsilon_{x_0} \left(1 - \frac{K_{\perp}}{K_{||}} \right). \quad (2)$$

where $K_{||}$, K_{\perp} are the longitudinal and transverse gauge factors of the silicon channel PR , respectively; ε_{x_0} is the amount of strain EE at the geometric centers of the piezoresistors $R_1; R_3$ channels.

The leakage current of the p-n junction or reverse current J_{rev} is divided into three components ⁴:

- I_{0gen} - current of generation of carriers in the carrier poor p-n junction region in the body of elastic element;

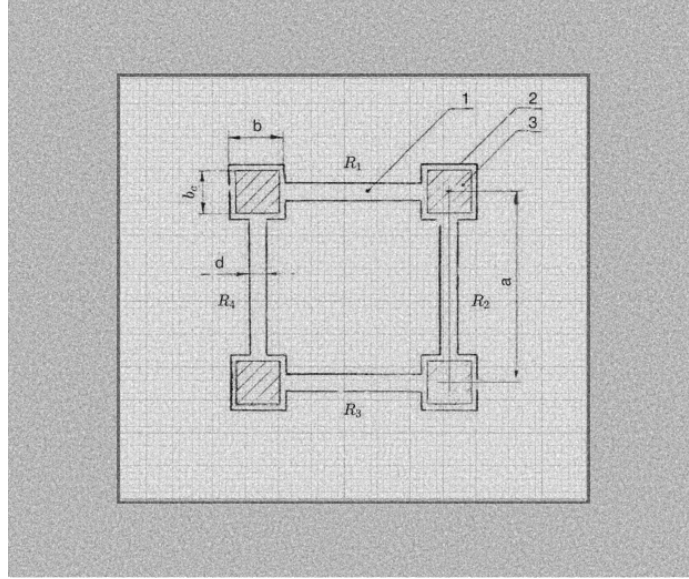


Fig. 7. Topological structure of a symmetric four-branch bridge circuit. 1-piezoresistive channel PR; 2-diffusion contact pad of p-type; 3-contact "Al-Si (p-type)".

- I_{Sgen} - charge carrier generation current in the carrier poor p-n junction region on the surface of the elastic element;
- I_d is the diffusion component of the reverse current, i.e.

$$I_{rev} = I_{0gen} + I_{Sgen} + I_d , \quad (3)$$

$$I_{0gen} = \frac{1}{2} q \frac{n_i}{\tau_0} d_{p-n} \cdot A_{p-n} , \quad (4)$$

where n_i is the carrier concentration in the native semiconductor; τ_0 is the carrier lifetime in the p-n junction region; d_{p-n} is the width of the p-n junction region; q is the elementary charge;

$$I_{Sgen} = \frac{1}{2} q S_0 \cdot n_i \cdot d_{p-n} \cdot P_{p-n} , \quad (5)$$

where S_0 is the surface recombination rate; P_{p-n} is the perimeter of the $p-n$ junction;

$$I_d = \frac{q n_i^2 L_p}{\tau_p N_n} \cdot A_{p-n} , \quad (6)$$

where L_p is the diffusion length of minority charge carriers in the EE body; N_n is the concentration of impurity in the EE body; n_i - concentration of free charge carriers; τ_p - lifetime of minority charge carriers in body EE ; μ_p is the mobility of minority charge carriers in body EE .

In deriving the calculated dependence of the inverse current density J_{rev} on temperature to determine the upper limit of the operating temperature range of monolithic IPT , where PR p-type in EE n-type are isolated by a layer of carrier-poor $p-n$ junction, the following conditions, initial data and calculation

relations were chosen.

(1) The dependence of $I_{rev}(T)$ is determined by relations (3)-(6) and temperature changes of parameters:

- of free charge carriers $n_i(T)$ from relation $n_i(T) = n_{i0} \cdot e^{21.3(1-\frac{T_0}{T})}$;
- the lifetime $\tau_p(T)$ for the minority charge carriers in the body EE ;
- the lifetime of $\mu_p(T)$ for the minority charge carriers in the EE body from the relation ⁵ :

$$\mu_p(T) = \mu_{p0} \left(\frac{T_0}{T} \right)^{2.5} \quad (7)$$

where $\mu_{p0}(T)$ is the hole mobility at temperature $T_0 = 293 \text{ K}$;

- the diffusion length $L_p(T)$ for the minority charge carriers in the body EE from the relation:

$$L_p(T) = \left(\frac{\mu_p(T) \cdot \tau_p(T) \cdot k \cdot T}{q} \right)^{1/2} \quad (8)$$

- S_0 —does not change with temperature and is equal to the maximum value $S_0 = 1 \cdot 10^4 \text{ cm/sec}$.

(2) $P - N$ junction is a sharp, asymmetric, stepped, $p - n$ type junction (that is, $\tilde{\rho}_{ch} \ll \rho_{ee}$) with the width of the bulk charge region in the EE body equal to

$$d_{p-n} \approx 3.65 \cdot 10^3 \left(\frac{V_{rev}}{N_e EE} \right)^{1/2} \quad (9)$$

a uniform distribution of bulk charges along the metallurgical junction boundary.

(3) In the topological structure MC in Fig. 7, the geometrical parameter b is given a constant value equal to $b = 40 \cdot 10^{-4} \text{ cm}$. For the calculations, $b = d_{ch}$, then changing the area of the insulating $p-n$ junction is possible only by changing the length of PR $l_{ch} = (a - b)$. The ratio of the perimeter $p - n$ junction P_{p-n} to the area A_{p-n} is a constant value equal to

$$K_{p-n} = \frac{P_{p-n}}{A_{p-n}} = 500 \text{ cm}^{-1} \quad (10)$$

(4) The reverse bias voltage $p - n$ junction and supply voltage MC are $V_{rev} = V_{in} = 5V$.

(5) The boundary values of the resistances EE are determined by the values: $\rho_{ee1} = 20 \Omega \cdot \text{cm}$, the intrinsic conductivity temperature $+150^\circ\text{C}$; $\rho_{ee1} = 0.5 \Omega \cdot \text{cm}$ is the calculated value of the breakdown voltage $p - n$ transition in the EE volume, chosen equal to $V_{br} = 10 \cdot V_{in}$ from the ratio:

$$V_{br} = 10 \cdot V_{in} = 86 \cdot \rho_{ee} \quad (11)$$

$\rho_{ee1} = 4.5 \Omega \cdot \text{cm}$ is the standard resistivity value of silicon wafers in IPT production.

(6) Initial temperature value $T_0 = 293\text{K}$.

Taking into account the selected initial data and the calculated relations, the temperature dependence of the reverse current density VAC of the IPT isolating $p - n$ -junction is determined by the following expression:

$$J_{rev} = q \cdot a_{p-n} \cdot \left(\frac{1}{\tau_p(T)} + S_0 \cdot K_{p-n} \right) \cdot e^{22.2 \cdot \left(\frac{T-293}{T} \right)} + q \cdot \left[\left(\frac{k \cdot \mu_{p0}}{q \cdot \tau_p(T)} \right)^{1/2} \cdot \left(\frac{113.7}{T} \right)^3 \cdot P_n \cdot e^{22.2 \cdot \left(\frac{T-293}{T} \right)} \right] \cdot e^{22.2 \cdot \left(\frac{T-293}{T} \right)} \quad (12)$$

where $a_{p-n} = \frac{d_{p-n} \cdot n_{i0}}{2}$ is a parameter characterizing the concentration of intrinsic charge carriers n_{i0} in the $p-n$ junction region at temperature $T = 293 \text{ K}$; $P_n = \frac{n_{i0}^2}{N_{ee}^2}$ is the concentration of minority charge carriers in the EE body at $T = 293 \text{ K}$; $k = 1.38 \cdot 10^{-23} \text{ J/K}$ - Boltzmann constant.

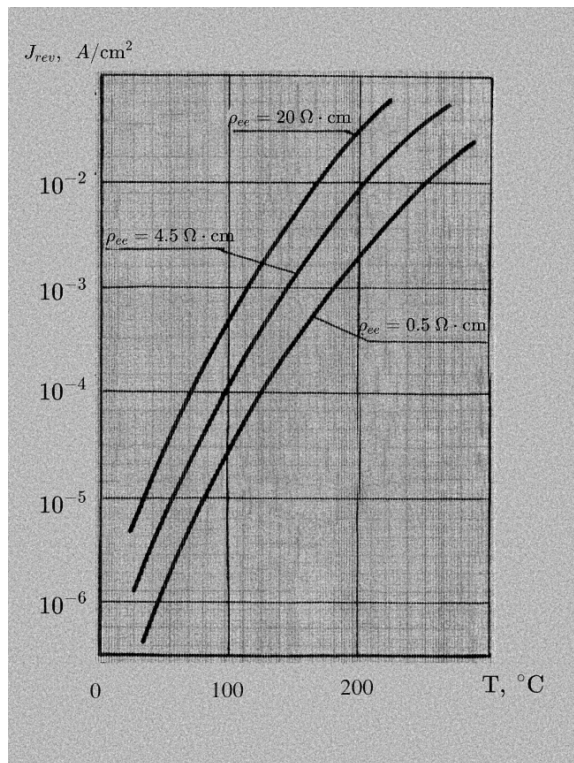


Fig. 8. Calculated dependences of reverse current density J_{rev} of p-n junction IPT on temperature for different values of resistivity of elastic element ρ_{ee}

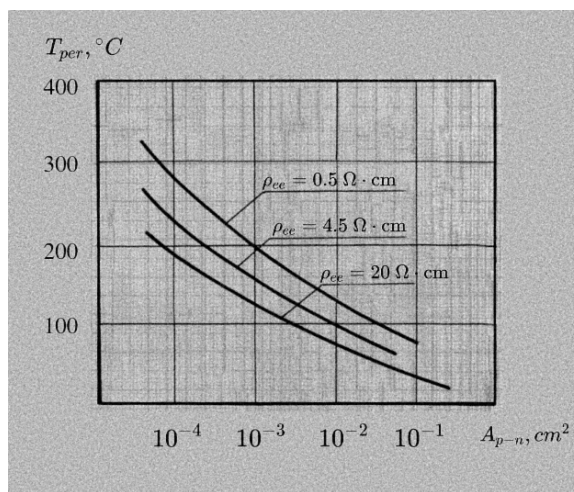


Fig. 9. Calculated dependences of permissible temperature T_{per} values on the area of insulating p-n junction A_{p-n} for different values of resistivity of elastic element ρ_{ee}

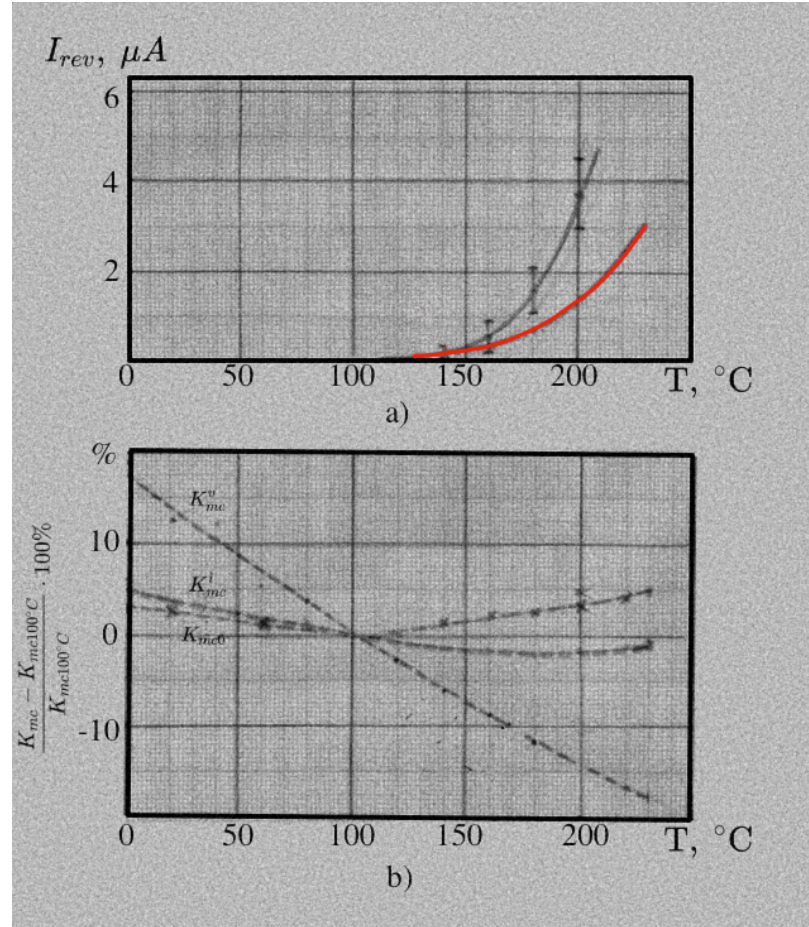


Fig. 10. Temperature dependences of IPT sample parameters: a) I_{rev} reverse current: — experimentally, — calculated; b) K_{mc0} - normalized null output, K_{mc}^v -IPT bridge sensitivity when $V_{in} = 5$ V stabilized voltage is fed to the MC, K_{mc}^i - IPT bridge sensitivity when $I_{in} = 5\mu A$ stabilized current is fed to the MC

Fig. 8 shows the calculated dependences of $J_{rev}(T)$ for the selected values of ρ_{ee} on which the dependences of the allowable temperature values T_{per} on the insulating junction area of $p-n$ are plotted in Fig. 9. For the chosen topological structure, the minimum allowable value A_{p-n}^{min} can be determined by the minimum standard value of the resistance of the piezoresistor equal to 95Ω and the resistance of the surface of the piezoresistive layer equal for ion alloy layers $(80 \div 150) \Omega/\square$. In this case, the geometric parameter $\frac{a-b}{b} \approx 1$ and the area $A_{p-n}^{min} = 1.28 \cdot 10^{-4} \text{ cm}^2$. From the graphs in Fig. 9, the upper limit of the operating temperature range for A_{p-n}^{min} is determined by the values $185^\circ C$, $225^\circ C$ and $275^\circ C$ at resistances of the elastic element of $20 \Omega \cdot \text{cm}$, $4.5 \Omega \cdot \text{cm}$ and $0.5 \Omega \cdot \text{cm}$, respectively.

To experimentally verify the calculations, the beam forces IPT were fabricated from single-crystal silicon n type with orientation (001) and resistivity $\rho_{ee} = 4.5 \Omega \cdot \text{cm}$. The geometric parameters of the topological structure are as follows: $b = 40 \cdot 10^{-4} \text{ cm}$; $b = d$; $a = 3 \cdot b$, $A_{p-n} = 1.92 \cdot 10^{-4} \text{ cm}^2$; $K_{p-n} = \frac{P_{p-n}}{A_{p-n}} = 500 \text{ cm}^{-1}$. PR were formed by boron ion implantation technology with a doping dose of $2 \cdot 10^{15} \text{ cm}^{-2}$. The surface resistivity of the piezoresistive layers doped with ions $R_s = 85 \Omega/\square$ ⁶.

Fig. 10 shows experimental for IPT samples and calculated from the graph in Fig. 9 for this topological

structure MC dependences of the reverse current I_{rev} VAC on temperature, by which the upper limit of the temperature range (value T_{per} at $I_{rev} = 2 \mu A$) is determined:

- for samples IPT values $+180^{\circ}C \div +200^{\circ}C$
- for the value $+210^{\circ}C$ calculated from formula (3.10).

The experimentally measured temperature dependences $K_{mc0}(T)$, $K_{mc}^u(T)$, and $K_{mc}^i(T)$ in Fig. 10(b) are characterized by smooth changes throughout the range up to the limiting research temperature $+260^{\circ}C$.

The calculations performed and experimental studies give grounds to assert that monolithic silicon integral piezoresistive transducers with the isolation of piezoresistive channels of p -type conductivity from EE by the $p-n$ junction layer are able to work up to temperatures $+180^{\circ}C \div 300^{\circ}C$. The specific limits of the operating range will be determined by the values of the resistivity and geometrical parameters of the topological structure MC selected during the design.

B. Development and Research of Manufacturing Technology for Microtransducers, Measurement Modules and Prototype Transducer

The development of constructively constructive prospective technological solutions (CTS) for sensor devices with improved metrological and operational characteristics requires the solution to the problem of integration of sensitive elements with external conversion devices. The necessity of employing multiple separate sensitive elements within a single sensor device, distributed across different planes and levels, has posed a challenge in creating a flexible commutation board that allows for mounting its outputs on aluminum contacts and contacts with direct connection.

The development of sensitive elements with reduced thickness, based on fragile materials, necessitates the adoption of widely used methods to connect to other materials by welding, ensuring lower loads on the crystal during assembly. The required loads can be achieved by mounting crystals using anisotropic-electrically conductive composites.

Expanding the operating temperature range of sensor devices to $300^{\circ}C$ has required the development of thin film elements capable of functioning within this range, as well as thermal compensation schemes.

Thus, the analysis of prospective CTS requires additional development of the following technological processes:

- 1) Development of a package of new technologies and a precision silicon chemical etching unit.
- 2) Development of technology for the manufacture of multilayer boards with aluminum interconnects.
- 3) The technology of applying a coating to aluminum leads for assembly by the soldering method.
- 4) The technology for mounting leadless ICs using anisotropic electrically conductive compositions.
- 5) The technology of manufacturing thin-film thermoresistors for the temperature range of $(+150 \div 300)^{\circ}C$.
- 6) Development of experimental glass formulations for electrostatic glass-silicon bonding

1) Development of a package of new technologies and a precision silicon chemical etching unit (SCEU)

The purpose of this development, on the one hand, was to improve the operational characteristics of the integrated sensors of mechanical parameters, i.e. to increase the service life (in the sensor assembly), the mechanical strength reserve, as well as to increase the yield of good quality IPT in the final production

up to 30% and more, on the other hand, to reduce the labor costs of manufacturing *IPT* by automating the most labor-intensive operations of their production, in particular, the process of profiling the elastic element.

During the first stage of 1980-1989, experimental work was carried out to develop the technological modes of the most promising technological processes. These processes include deep plasma chemical etching of silicon, group anisotropic profiling of elastic elements of integrated converters, sedimentation of fusion, and dimensional processing of glass films with a structure close to silicon for the electro-adhesive connection of microelectronic measuring module components, protection based on polyimide lacquers for measuring circuits from the effects of the working medium, which, when used in conjunction with the standard planar film technology for manufacturing microelectronic devices, would allow for the implementation of new design and technological solutions for sensors of mechanical quantities developed on this topic, improve the operational characteristics of these sensors, and solve the issue of developing technological documentation for experimental and serial production of sensors.

Parallel to this, during the first stage, work was carried out on the development and manufacture of an experimental model of an automated setup for precision, anisotropic, deep silicon etching. This would help overcome the bottleneck (low productivity and low reproducibility) in the technology of profiling *IPT* sensors and significantly improve the quality of etching. As a result of the work, the following experimental technological processes were developed:

- Plasma chemical etching of silicon plates 925.2241.013-88.
- Application, melting, and dimensional processing of glass coatings 925.2241.012-88.
- Passivation (protection) of the *IPT* sensor measurement circuits 925.2241.029-88.
- Group anisotropic profiling of silicon plates 925.2241.029-88.

Design documentation was developed and the manufacture, assembly, and debugging of the idle sample of the pre-ion chemical etching setup for silicon (SCEU) SIAP.066741.OO11 was carried out. Act No. 073/89 of 14.12.89.

The results of the technological development of the set of new technological processes, the development of design documentation, and the debugging of the experimental model of the setup are more fully reflected in the interim technical report on the topic 0-706-88 OTR 195.2241.035.

In the second stage of work on this subject, testing of new technological processes under the conditions of pilot production of our enterprise was carried out.

According to test results (protocols 074/89, 075/89, 076/89, 077/89), the modes of technological operations were corrected and standard technological processes were issued.

- group anisotropic etching of silicon wafers TTP(P) 925.02255.00116;
- Passivation (protection) of the strain-sensitive circuits of the integrated transducers TTP 925.02255.00114;
- Application and dimensional treatment of glass coatings TTP 925.02255.00115;
- Deep plasma chemical etching of silicon. TTP 925.02255.00031. Inventory No. 925.25415 of 14.07.89.

Laboratory and pilot tests of batches of test samples of control and regulation sensor and low-frequency accelerometer *IPTs* manufactured using the developed technological processes showed an increase in the output of suitable *IP* sensors for control and regulation from 18.5

Using the new developed operational technological processes, the technological documentation (TD) for experimental production of integrated semiconductor converters of sensor measuring modules was developed, including the following:

A set of documents for the technological process of manufacturing integrated converters of low-frequency semiconductor accelerometer ANPPE-001 SIAP.402139.001 TP 925.02255.00132;

A set of documents for the technological process of manufacturing integrated converters of the measurement module of the SIAP.408 854.001 TP 925.02255.00133.

In 1990, debugging was carried out in the operating mode of an idle sample of precision chemical etching installations for silicon (UPHT) (Act No. 073/14.02.90).

Based on the results of preliminary factory tests, the Design Documentation (DD) was corrected and the documentation on the installation of SIAP.066741.001 UPHT was assigned the letter "O". The installation was masterminded in the experimental production of the SRTIIE enterprise, and interdepartmental tests were carried out with the assignment of the DD letter "O".

2) Development of Technology for Manufacturing Multilayer Boards with Aluminum Interconnects

Existing technological processes for manufacturing multilayer boards with aluminum interconnects, such as vacuum deposition or electroplating, require complex equipment or involve processing at high temperatures in molten salt baths. In the proposed invention application 164748816/21, a simpler method is suggested for manufacturing multilayer boards, based on sequential welding of the conductors of single layer boards made on lacquer-film dielectric FDI-AP YU0.037.0421U according to TTP 925.02256.00087.

During the technology processing, the optimal sizes of the conductors and holes of the single-layer boards were determined, the equipment was selected, the technological fixtures developed, and the optimal ultrasonic welding modes were chosen. As a result, the welded joints achieved a strength of at least 20 G and the transition resistance between the conductors of the adjacent layers was not greater than $1 \cdot 10^{-2} \Omega$. The board consisted of 4 layers.

Unlike existing methods, the developed technology only involves two types of operations: precision photolithography to obtain conductor patterns and holes on the single-layer boards, and ultrasonic welding.

Based on the conducted work, a "Set of Documents for the Technology of Manufacturing Multilayer Boards with Aluminum Interconnects" (925.02290.00016) has been developed.

3) The Technology of Applying a Coating to Aluminum Leads for Assembly by Soldering Method

The formation of solder coatings on aluminum leads is possible with the help of vacuum deposition or chemical deposition methods. When developing this technology, the chemical deposition method was chosen, which provides better adhesion compared to vacuum deposition, less internal stresses in the coatings, and the possibility of producing coatings of greater thickness.

During the experimental work, the following issues were addressed: the creation of an intermediate layer that is electrically compatible with aluminum and the solder coating, the removal of film and sludge from the surface of aluminum using fixtures, the optimization of electrolyte compositions and surface preparation techniques for aluminum, and the chemical deposition of nickel and the electrochemical deposition of a tin-bismuth alloy.

The selection of an intermediate layer based on the zinc and nickel-phosphorus alloy ensured high adhesion and minimal internal stresses that remained unchanged during the heating process of the soldering.

For the deposition of the tin-bismuth alloy, a citrate electrolyte (positive solution to application No. 4376294/22) was chosen, providing a uniformly coated and pore-free surface with high solder wetting.

Optimal technological regimes have been determined:

- Aluminum oxide removal temperature: 50°C
- Nickel plating temperature: 82 ÷ 85°C
- pH of the nickel plating solution: 3.2 ÷ 4
- Current density during tin-bismuth deposition: 0.4 ÷ 0.5 A/cm²
- Tin-bismuth deposition rate: (10 ÷ 12)μ/h

The conducted work allowed obtaining solderable coatings based on tin-bismuth with the following characteristics:

- Adhesion: not less than 3000H/cm²
- Solder spreading coefficient: not less than 1.5
- Thickness uniformity: not exceeding 1 μ
- Retention of solderability without additional reflow for 1 year.

Developed a set of documents for the Technological process of coating aluminum terminals for mounting by soldering” (925.02271.00016)

4) *The Technology of Mounting Leadless ICs Using Anisotropic Electrically Conductive Composition*

The use of reactoplasts (epoxy resins) as a polymer base ensures high-strength bonding of semiconductor crystals to the microassembly board. However, it does not allow the production of connections resistant to thermal cycling. Additionally, the long curing time of the composition (around 4-5 hours) and the challenges of working with the composition in its liquid phase significantly increase the complexity of manufacturing devices based on it.

The developed technology for mounting leadless ICs with aluminum interconnects on the interconnection board involves creating contact areas on the board using an anisotropic electrically conductive film made from thermoplastic materials. This is followed by thermocompression bonding of the flat contact areas of the inverted crystal with the film contact.

High-density polyethylene (HDPE) was chosen according to GOST 16377-77E as the polymer base for the film. The anisotropy of electrical conductivity is achieved by thermomechanical pressing of nickel carbonyl particles according to GOST 9722-79 into the film in a magnetic field.

During the research process, the optimal film thickness and size of the conductive particles were determined to be approximately 40 micrometers. Approximate attachment parameters were selected for the EM-431 assembly machine:

- Pulse heating temperature $T = (+150 \div 160)^{\circ}C$
- Mounting tool pressure $P = (10 \div 30) \text{ kg/cm}^2$
- Mounting time = 10 seconds

The developed technology for mounting leadless ICs ensures a transition resistance of no more than 10 Ω, insulation resistance of at least $1 \cdot 10^6 \Omega$, and crystal bonding strength of at least 50 G.

The developed technology consists of two types of operations: forming the anisotropic electrically conductive film and mounting the leadless ICs using the film as a spacer. On the basis of the research

results, a "Set of Documents for the Technology of Mounting Leadless ICs Using Anisotropic Electrically Conductive Compositions" (925.02285.00025) has been developed.

5) *The Technology of Manufacturing Thin-Film Thermoresistors for the Range of (+150÷300)°C*

Currently developed miniature semiconductor thermoresistors at temperatures above 160°C have a large non-linearity of the temperature response, which leads to the need to complicate the conversion equipment. This drawback can be eliminated by using thin-film thermoresistors made of platinum, nickel, and other metals. Nickel, selected for the sensitive element of the thermistor, provides high sensitivity and linearity, and at low cost allows one to refuse the use of precious metals.

In the process of work, the technological modes of chromium-nickel structure deposition, structure annealing, thermoresistors adjustment by ion etching, attachment of nickel strip leads, and sealing by compound were perfected. Tests of thermoresistors manufactured by the developed technology showed that:

- accuracy of nominal resistance value of thermoresistors is $\pm 2\%$;
- The range of temperatures $(+150 \div 300)^\circ\text{C}$;
- temperature coefficient of resistance of sensitive element is greater than $4.2 \cdot 10^{-3} \text{ }^\circ\text{C}^{-1}$;
- change of resistance during thermocycling at $20 \div 300$ for 150 cycles not more than 1.5%.

As a result of this work, a set of documents for "Typical manufacturing process of thin-film thermoresistors (RTD) for dialysis $(+150 \div 300)^\circ\text{C}$ 925.02255.00126.

6) *Development of Experimental Glass Formulations for Electrostatic Glass-Silicon Bonding*

The question of the applicability of glass for electrostatic glass-silicon connection can be solved on the basis of the evaluation of a number of glass properties. The main criterion is the Coefficient of Linear Thermal Expansion (CLTE) and the temperature at the beginning of the deformation of the glass (according to Littleton).

The temperature range of the devices stipulated the choice of temperature intervals, where estimation of the character of the changes CLTE of glass and silicon is extremely important: from $-60^\circ\text{C} \div +100^\circ\text{C}$; from $0^\circ\text{C} \div 200^\circ\text{C}$, because thermal deformations that arise in the silicon-glass system exert an essential influence on the output signal of the devices, directly proportional to the difference CLTE of glass and silicon.

The CLTE behavior of glass as a function of temperature is common to all types of glass. The CLTE of the glass remains constant from -60°C to the lower temperature annealing point. The lower annealing temperature is determined by the temperature at which the glass begins to deform.

CLTE of silicon in the range of -60°C to 200°C monotonically increases from $20 \cdot 10^7 \text{ }^\circ\text{C}^{-1}$ to $33 \cdot 10^7 \text{ }^\circ\text{C}^{-1}$.

Thus, the problem of reducing thermal stresses to a satisfactory minimum comes down to creating glasses that have in the range of 0°C to 100°C CLTE approximately $28 \cdot 10^7 \text{ }^\circ\text{C}^{-1}$ and in the range of 0°C to 200°C CLTE approximately $29 \cdot 10^7 \text{ }^\circ\text{C}^{-1}$, and the tolerances are up to 4 relative units of CLTE.

The calculation of thermal stresses on the bimetallic plate was used to determine the glass CLTE values corresponding to the minimum thermal stresses in the specified temperature ranges.

The solution of the problem of the development of the glass composition with the given properties was

started with the estimation of the relations between *CLTE* and the temperature of onset of deformation of different types of glass.

As a result, several glasses with low *CLTE* ($36 \cdot 10^7 \text{ }^\circ\text{C}^{-1}$) and high deformation onset temperature (about 500°C) were selected. All of these glasses were aluminoborosilicate with a relatively low alkali content (about 5%).

The compositions of the selected glasses were taken as matrices for the development of glasses with the specified *CLTE*.

It should be noted that *CLTE*, the density, Young's modulus, shear modulus, heat capacity, thermal conductivity, and a number of optical properties of glass can be calculated with satisfactory accuracy from the glass composition by the additive method. With additive coefficients for each oxide and a number of correction equations that determine the mutual influence of the oxides in the glass on the glass composition, all of the above properties can be calculated. To compare the calculated values of ⁷ and the experimentally obtained values of *CLTE* for some of the glasses studied, we present the table below.

Glass	Calculated CLTE values from 0°C to 400°C by Appen[3]	Experimental CLTE values 0°C to 400°C
IKS-10*	36	33.5
1	27	22.1
2	38	36

* - Oxygen-free chalcogenide glass in SU

As a result of solving the inverse problem (that is, the glass compositions were selected according to a given *CLTE*), the experimental compositions of the glasses were calculated, according to which the charge compositions were calculated.

Depending on the choice of charge, the melting temperatures were determined. Welded glasses were cast on a cast iron plate and annealed in electric furnaces. After that, samples of the obtained glasses were made to investigate physicochemical and thermophysical parameters, and also the crystalline ability of the glasses was investigated. and electrical conductivity measurements in $-60^\circ\text{C} \div 500^\circ\text{C}$ dialysis were carried out.

Measurements *CLTE* were made on cylindrical samples $\varnothing = 50 \text{ mm}$; $H = 5 \text{ mm}$; Flat-parallelism of cylinder bases 20°C by I200 C. The dilatometric curves, in addition to the change in relative elongation, determine the correct choice of the glass annealing temperature. Note that glass often had to be annealed a second time after primary annealing.

The analysis of the glass crystallization ability and the dilatometric curves made it possible to optimize the melting temperature.

After checking the physical and chemical properties of the experimental glasses, 1-2 samples of glass were selected from the batch. The last samples were tested for electrostatic bonding. As a result of studies of glasses of various compositions, three varieties of glass were chosen for electrostatic bonding with silicon (glasses 1,2,3). Glass 1 was designed for a range of -60°C to 100°C , glasses 2 and 3 for a range

of 0°C to 200°C . As a result of the check of the suitability of the glasses for electrostatic connection, as well as the check of the obtained samples for tightness and peel strength, the connection temperatures were determined: for glass 1 - 350°C , for glass 2 - 420°C , for glass 3 - 450°C .

C. Design and technological solutions and laboratory testing of low pressure IPT

The developed IPT has several design and technological solutions, which ensure a sufficiently high conversion accuracy ⁹. The most important of them are:

- 1) The central placement of the strain gauge bridge circuit means: a) Protection of the strain measurement circuit from possible influences of parasitic mechanical stresses from the attachment side; b) Uniform distribution of mechanical stresses in the area where the strain measurement circuit is located, resulting in independence from errors in layer alignment and the ability to use longer piezoresistors without losing sensitivity.
- 2) Approximation of the functioning of an elastic element to the model of an articulated beam.
- 3) Resistance of the design to technological errors in forming the configuration of the strain gauge strain gauge bridge.
- 4) The use of optimal impurity concentrations of p-type diffusion piezoresistors with resistivity of $2.3 \cdot 10^{-3} \Omega \cdot \text{cm}$, providing modes of autocompensation of temperature dependences of sensitivity ⁸.
- 5) Localization of the two-layer structure $\text{SiO}_2 - \text{Si}$ only in the conductive track region to reduce the influence of thermomechanical stresses that arise in such structures.

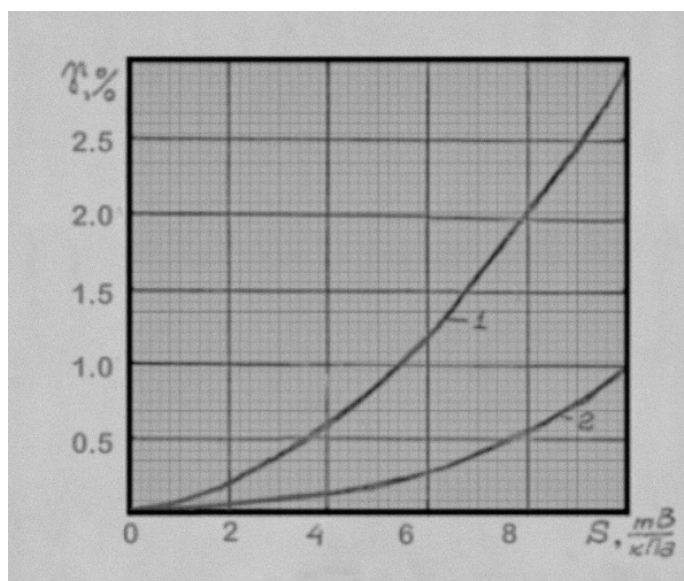


Fig. 11. Experimental dependences of nonlinearity of conversion on sensitivity for flat (curve 1) and ribbed (curve 2) integral transducers.

The effectiveness of the technical solutions incorporated in the design was experimentally confirmed. The measuring range was varied according to the calculation of the stress state and the selection of the thickness

ratios of the beam and diaphragm. At the same time, within a wide pressure range (from 0.1 kPa to 0.10 kPa), the basic error of the overwhelming majority of samples was within (0.2 - 0.1) % depending on the range of measured pressures and the form of representation of the formation characteristic. Orientation to the use of modern computer facilities, which allow approximation of the conversion function by the polynomial of higher orders, allows reducing significantly the basic error of measuring instruments (due to the reduction of approximation error).

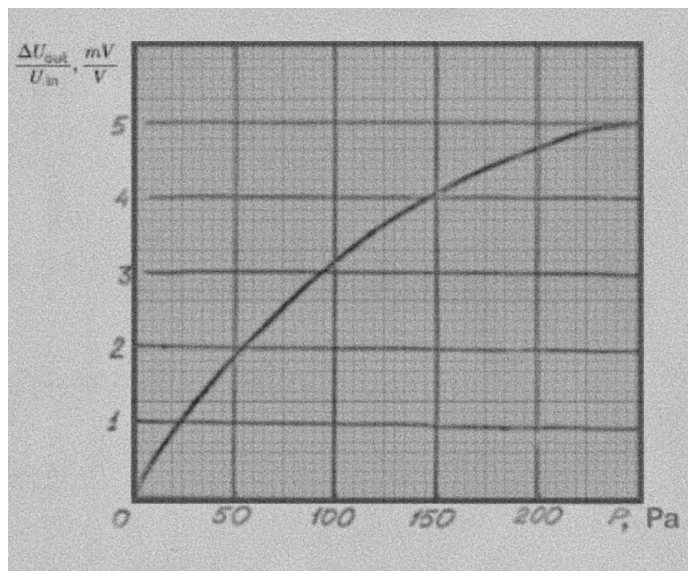


Fig. 12. Characteristic calibration characteristic of the transducers of supermarine pressures

The graphs in Fig. 11 show the experimental dependences of nonlinearity of integral semiconductor transducers on their sensitivity. Curve 1 describes the dependence for transducers with an elastic element (a flat square membrane), curve 2 describes the same dependence for transducers with stiffening ribs.

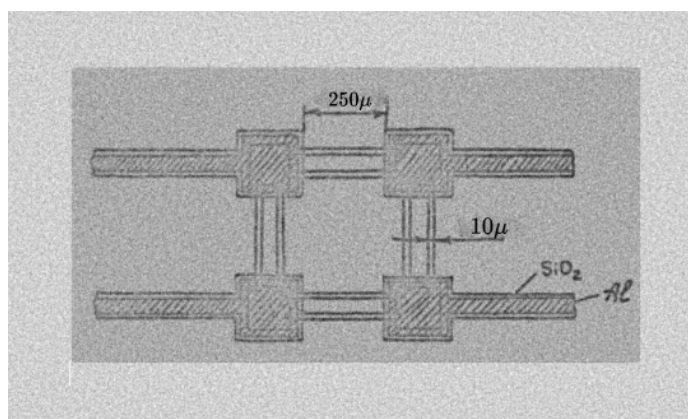


Fig. 13. Topology of the bridge measuring circuit of the transducer small pressure

From the graphs of Fig. 11 It follows that with equal sensitivity to the input quantity, the nonlinearity, and hence the basic error IPT of the proposed design is significantly less than the nonlinearity of the transducer

with a flat deformed region. With fixed and equal non-linearities of the transducers, the sensitivity of the diaphragm-beam transducer to pressure is greater, so the linear pressure conversion region expands toward smaller values.

The *IPT* with the dimensions creating the sensitivity limit (to work out the possibilities of the anisotropic chemical etching technology when forming elastic elements) were created. A characteristic calibration characteristic of such transducers is shown in Fig. 12. The effectiveness of mechanical decoupling of the

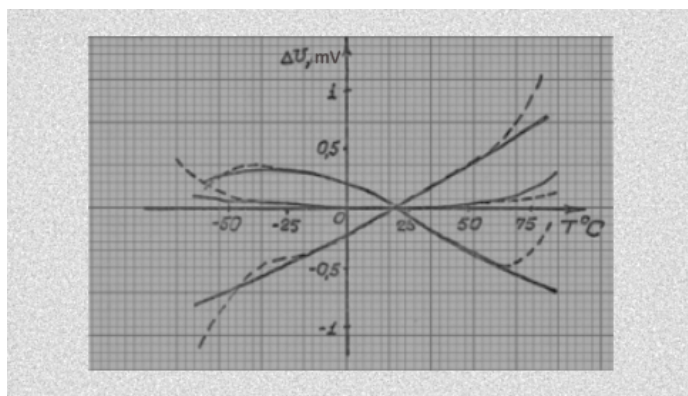


Fig. 14. Temperature dependence of the null output signal of the transducer small pressure

measuring circuit from the thermomechanical stresses generated in the silicon crystal mounting area is experimentally confirmed by the fact that in a wide temperature range (from -60°C to $+100^{\circ}\text{C}$) the temperature dependence of the null output signal was only slightly different between unmounted samples and samples mounted in an epoxy compound, which has a temperature coefficient of linear expansion more than an order of magnitude different from that of silicon (see Fig. 14).

Destruction of the samples under static pressure loading occurred at pressures tens of times higher than the nominal pressure, which allows to realize sensors with $30 \div 50$ margin of safety. The results obtained allow us to assert that this design can have a wide range of applications in pressure sensors.

III.CONCLUSIONS

The combination of technical solutions, supported by R&D, consists of the following key points:

- 1) The limits of miniaturization have been achieved within the scope of anisotropic chemical etching technology on standard substrates used in the planar technology of integrated circuit manufacturing. Further work should be oriented toward changing the overall microelectronics technology (e.g., changing the diameter and thickness of wafers, equipment and tooling for conducting thermal processes, etc.).
- 2) The results on the expansion of the temperature range of sensors with a piezoresistive full bridge measurement scheme, isolated from the elastic element by a p-n junction, have significantly exceeded expectations by more than 50°C . The upper limit of the operating range is approaching the technical feasibility limit for using the p-n junction isolation. Further expansion of the temperature range will require radical technical solutions.

For example, potential solutions could include the use of dielectric insulation, the substitution of semiconductor material, etc. Among all possible solutions, preference should be given to the one that allows the utilization of the largest number of well-established and proven technical solutions.

- 3) A technical solution has been found that extends the pressure range limitations previously imposed on the use of sensors with semiconductor strain elements, while still maintaining their compact size (weighing less than 40 grams). This technical solution can serve as a reliable basis for further research and development (R&D) activities aimed at creating a new class of sensors for various applications in general engineering, medicine, and other fields.
- 4) The system of technological solutions designed for the design and manufacturing of mechanical sensors has been supplemented with a set of plasma profiling processes, which are crucial for matching crystal shapes with components produced by turning operations.

The conducted work allows for:

- Defining the scope of R&D aimed at creating various mechanical sensors, with a particular focus on parametric series of pressure sensors for non-aggressive environments.
- Identifying the need for research and development in creating pressure reduction elements through hydraulic fluids to silicon elastic elements.
- Investigating the long-term stability of sensor elements and connection assemblies.
- Providing mathematical tools for calculating mechanical stress in sensor housings under high pressures and vibrations.
- Exploring solutions to extend the upper limit of the working temperature range.
- Methods for achieving vacuum-tight bonding of silicon with the metal casing to create absolute pressure sensors.

These areas of research will contribute to the advancement of the development and innovation of mechanical sensors and their applications.

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