

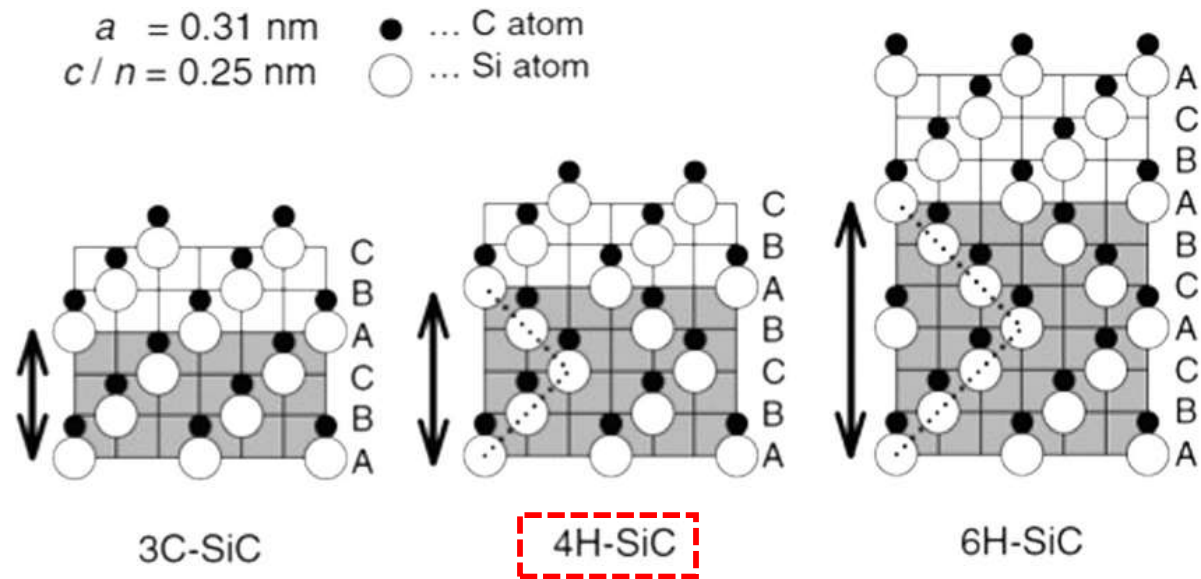
Surface nano-structuration of 4H-SiC by controlled high-temperature annealing

IWUMD23

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¹L2n, CNRS EMR 7004, UTT, France

Properties of SiC



K. Ashida et al, *JVSTB*. 33 (2015)

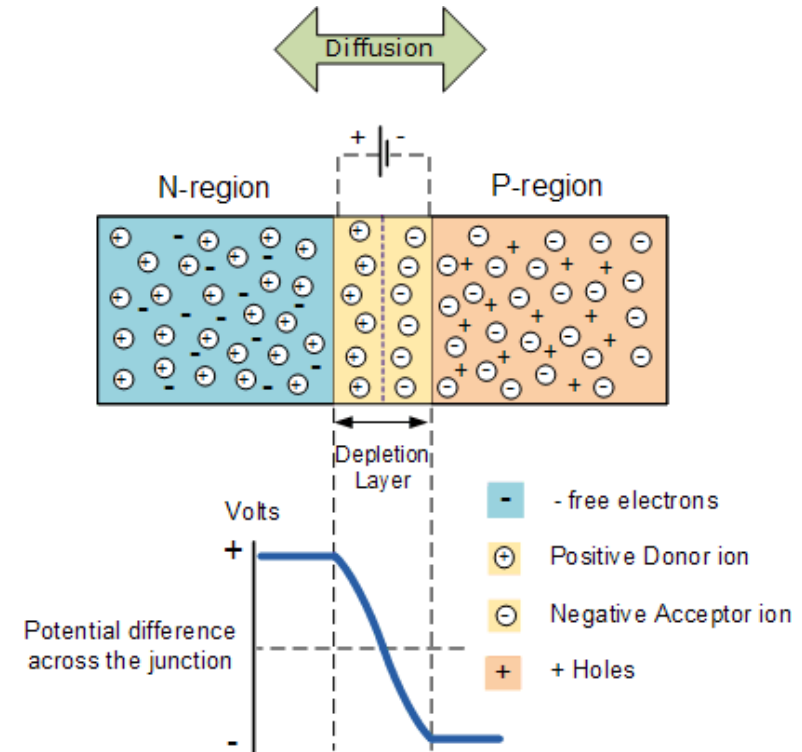
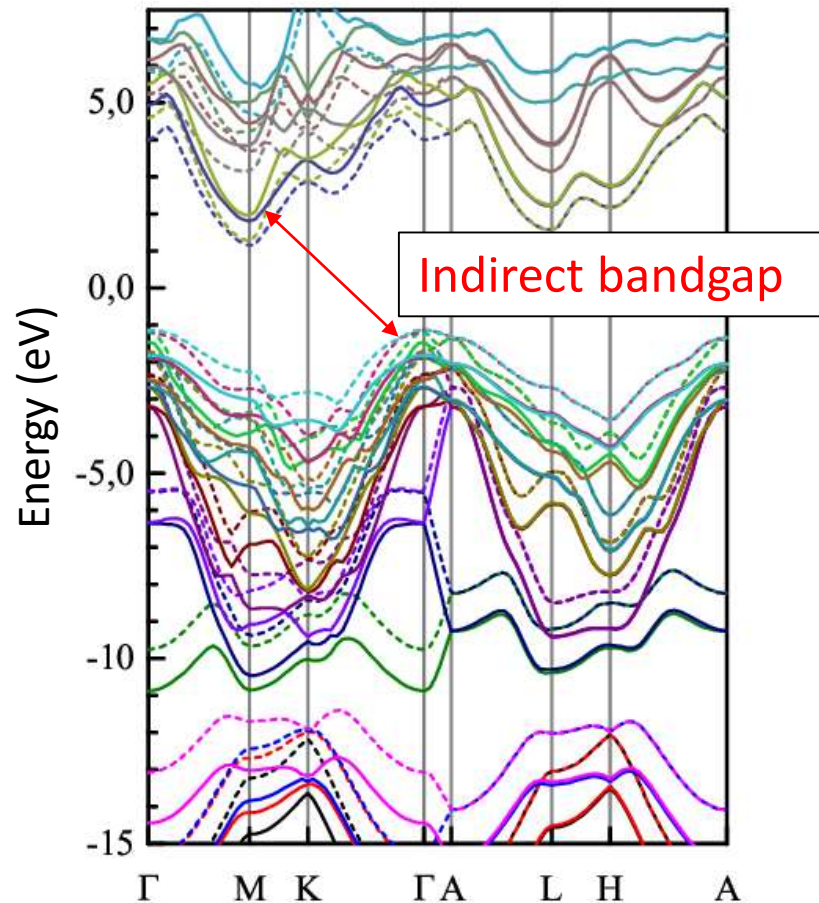
	6H-SiC	4H-SiC	3C-SiC	Si
λ (W/cm.K)	4,9	3,7	3,6	1,56
T_s or T_f (K)	$T_s: \sim 2840$			$T_f: \sim 1690$
E_g (eV)	3,0	3,26	2,2	1,12
E_c ($\times 10^6$) (V/cm)	3 à 5	3 à 5	1	0,25 à 0,8

C-M. Zetterling and M. Östling, Ed. *INSPEC, Process Technology for Silicon Carbide Devices* (2002)

- More than 200 polytypes
- Wide bandgap semiconductor
- Great thermal conductivity and thermal resistance

SiC as a LED material

4H-SiC



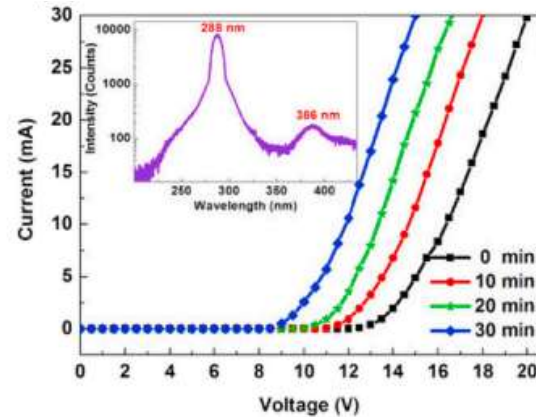
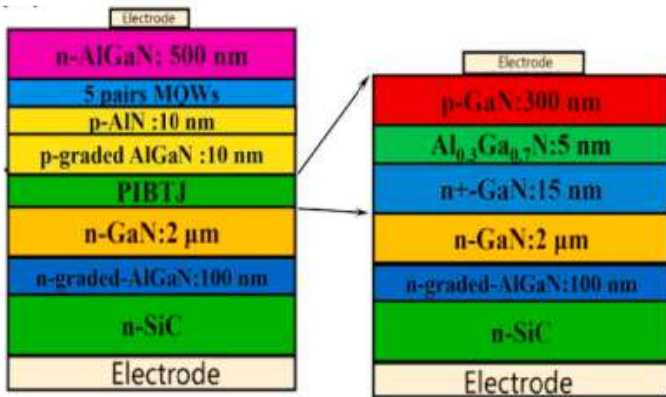
PN Junction Theory,

https://www.electronics-tutorials.ws/diode/diode_2.html

→ Not an active LED material

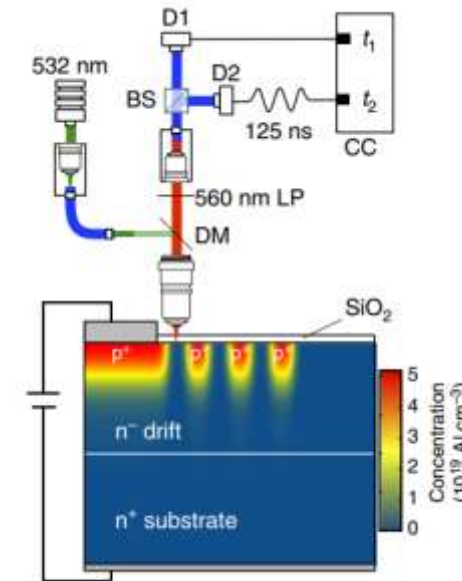
→ p-n junction: donor-to-acceptor pair luminescence (depends on doping, point defects...)

SiC for optoelectronics



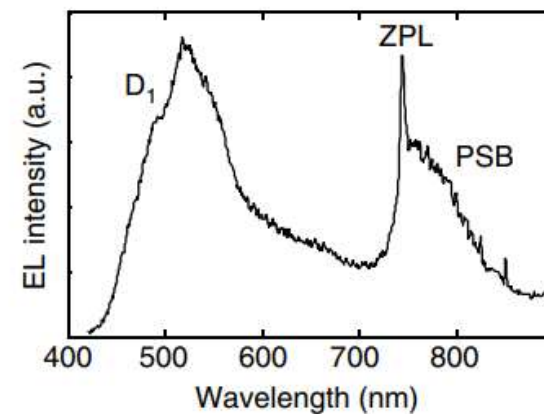
Hongwei Liang *et al*, *Jpn. J. Appl. Phys.* 55 (2016)

Vertical UV LEDs on SiC

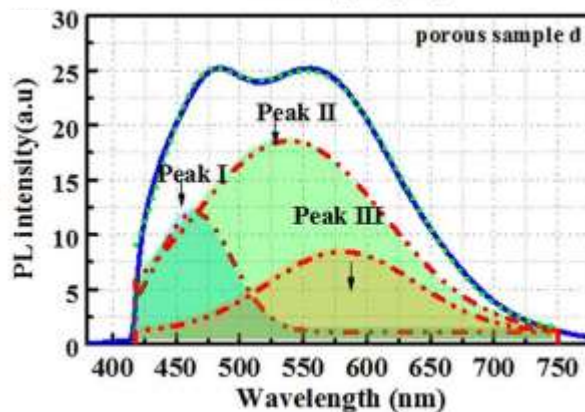
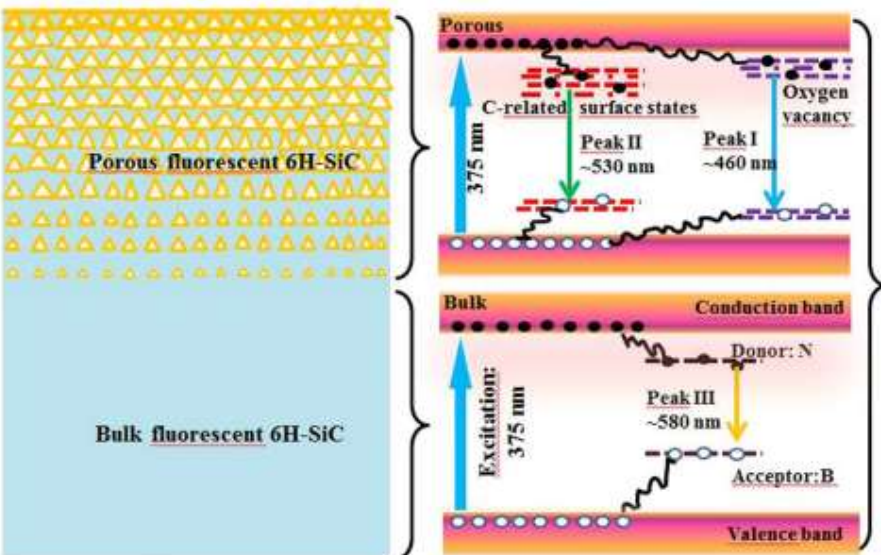


Single photon emitter

p-n diode



A. Lohrmann *et al*, *Nat. Commun.* (2015)

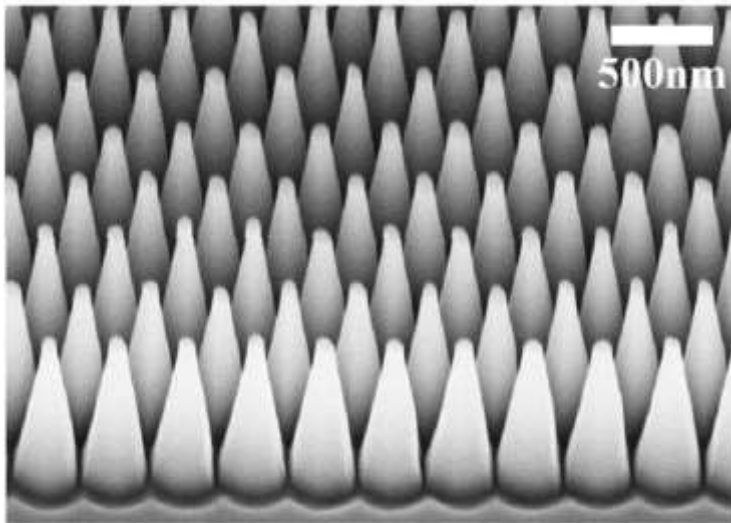


Fluorescent SiC

Weifang Lu *et al*, *Scientific Report.* 7 (2017)

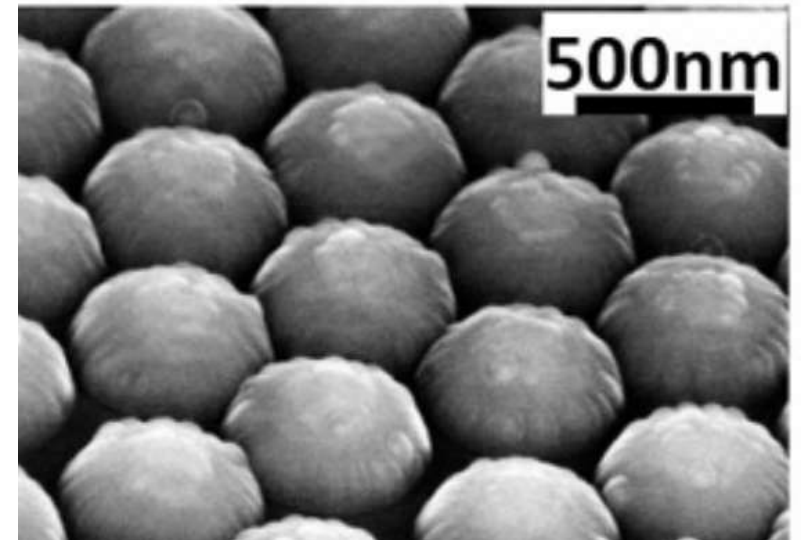
Issue

High refractive index of SiC (2.65 at 590 nm) → extraction of light is not optimal
Need surface **micro(nano)-structuring** → **anti-reflectance structures**



E-beam lithography of N-B doped 6H-SiC

Y. Ou *et al*, *Mater. Sci. Forum.* 740-742 (2013)



Nanosphere lithography of N-B doped 6H-SiC → Si₃N₄ coating of nano-domes

Y. Ou *et al*, *Scientific Reports*, 4 (2014)

Idea: control of Si sublimation at SiC surface with **high-temperature annealing** → fast nanostructuring of surfaces for local and large areas

- **1. Method**

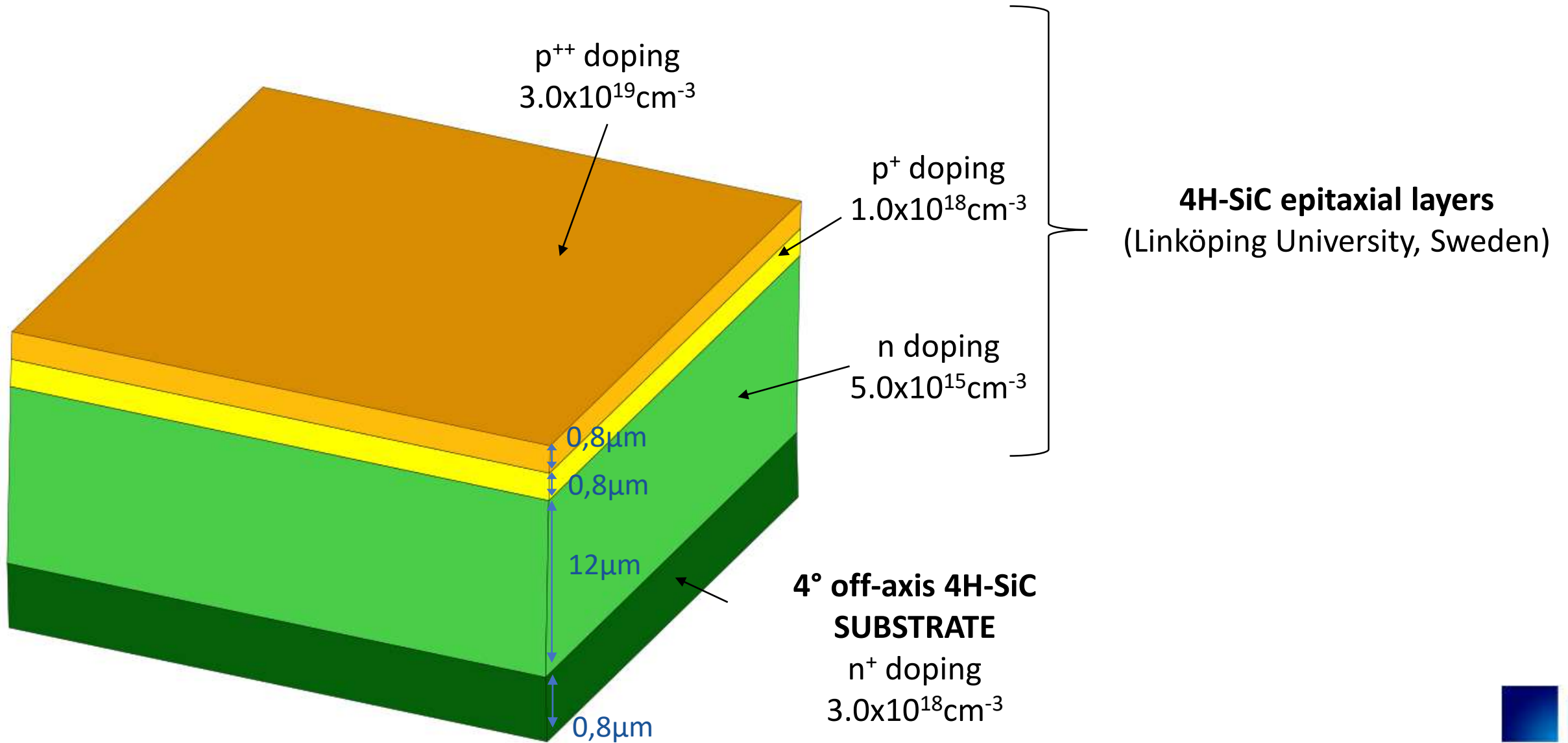
- **2. Surface analysis**

- **3. Electroluminescence**

- **4. Photoluminescence**

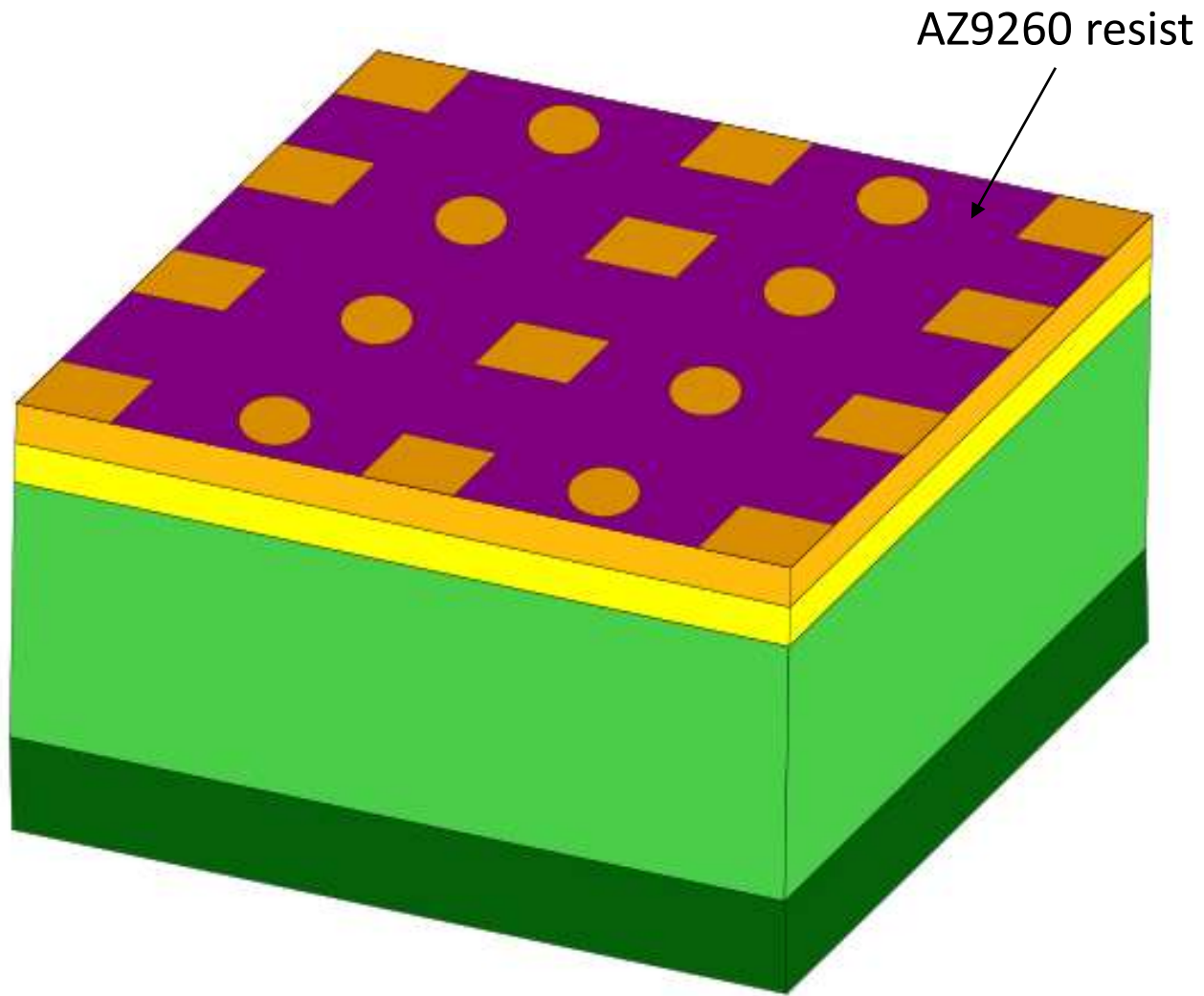
- **Conclusion**

1. METHOD (patented)

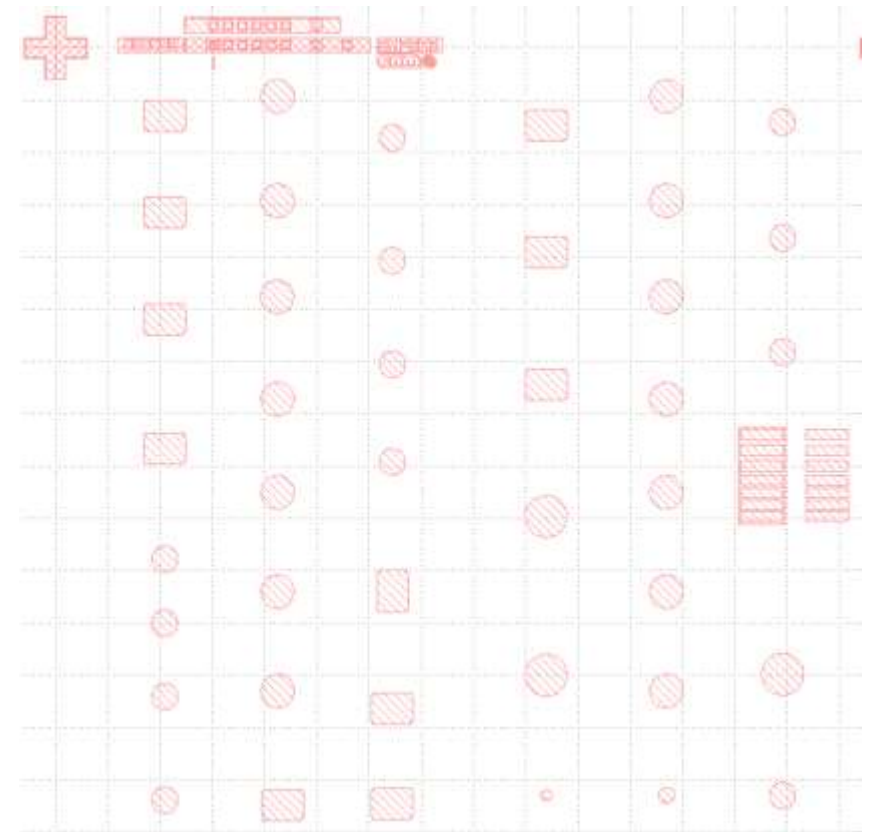


Formation of p-n diodes

1. METHOD (patented)

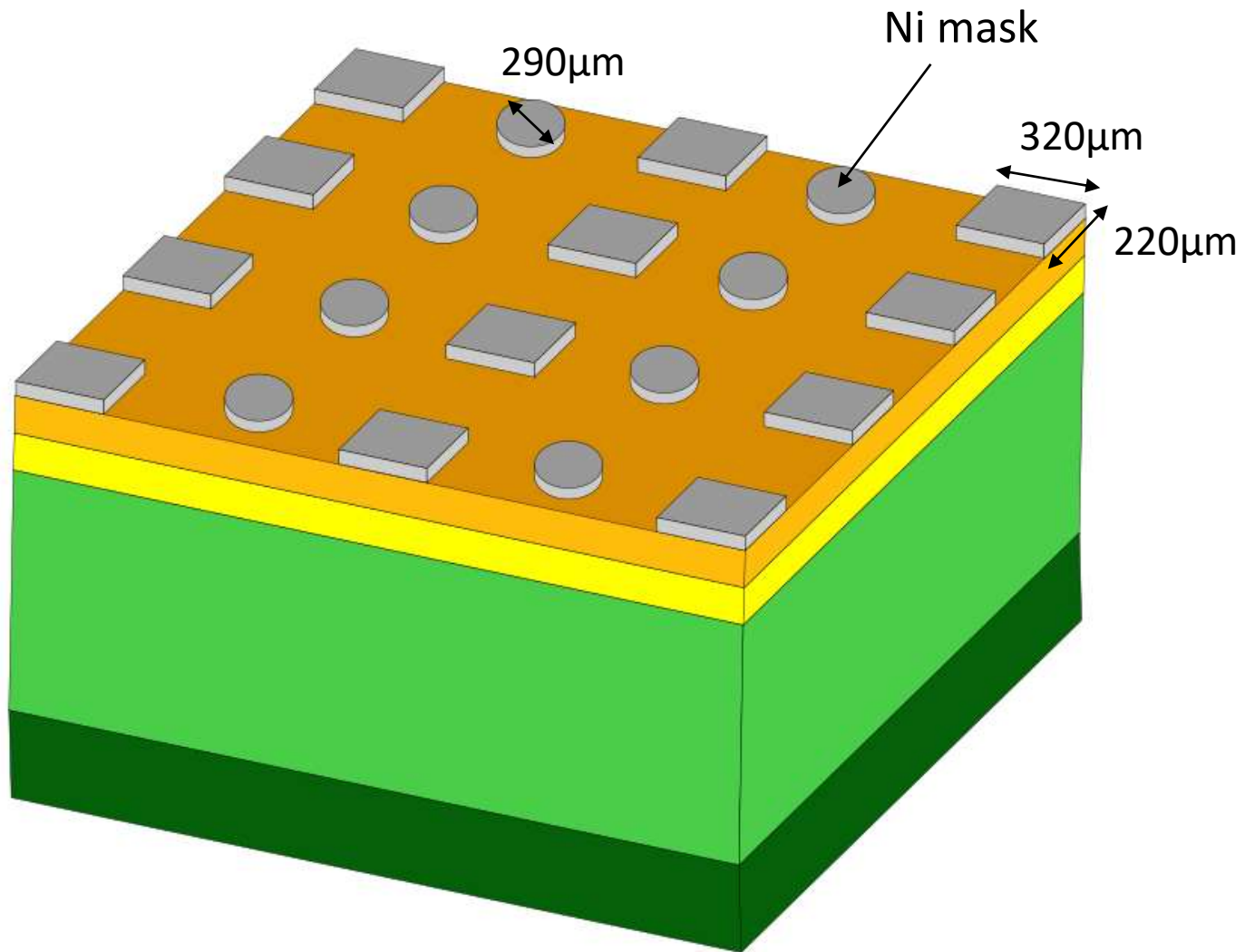


UV PHOTOLITHOGRAPHY

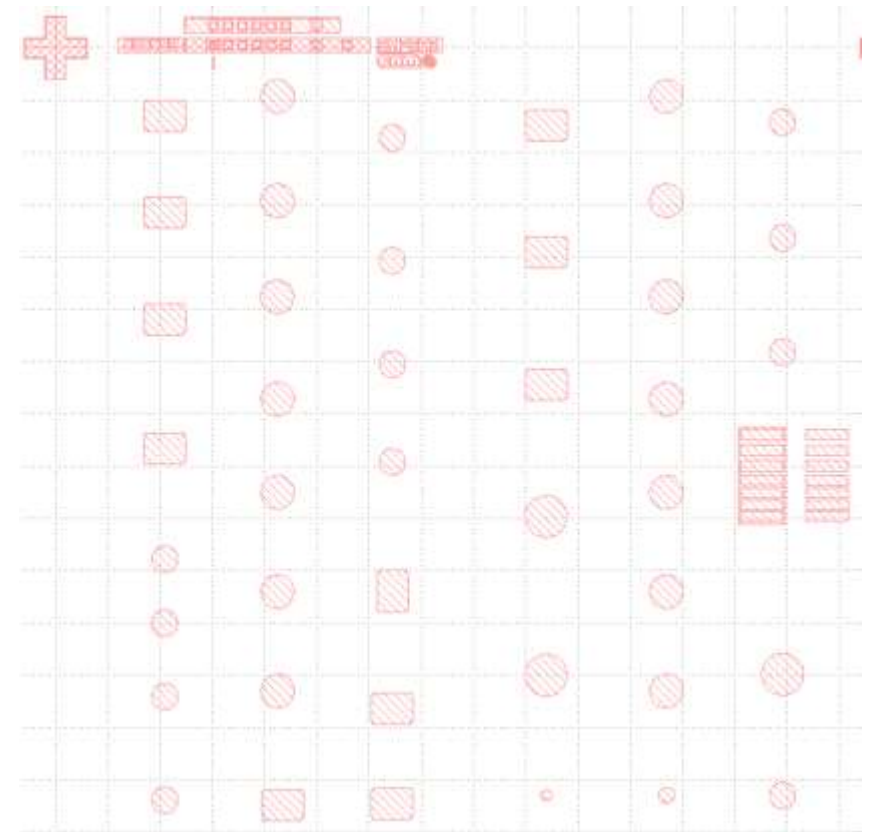


Formation of p-n diodes

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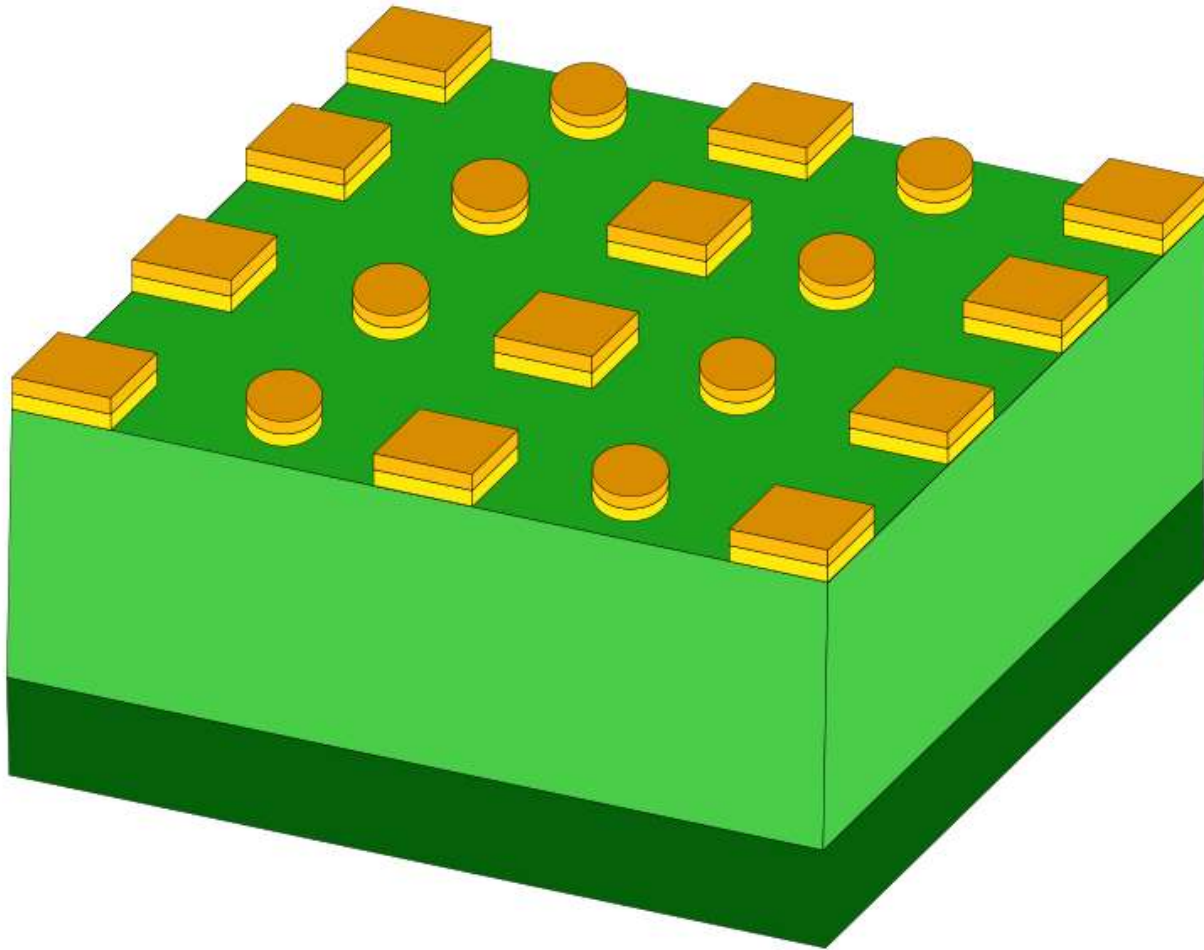


UV PHOTOLITHOGRAPHY



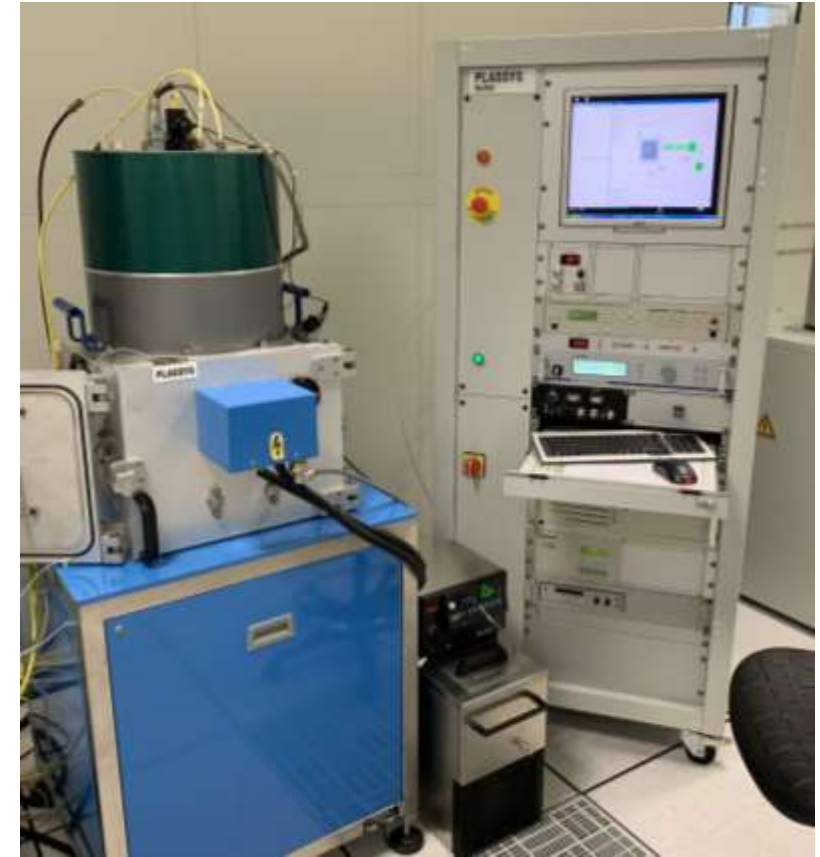
Formation of p-n diodes

1. METHOD (patented)



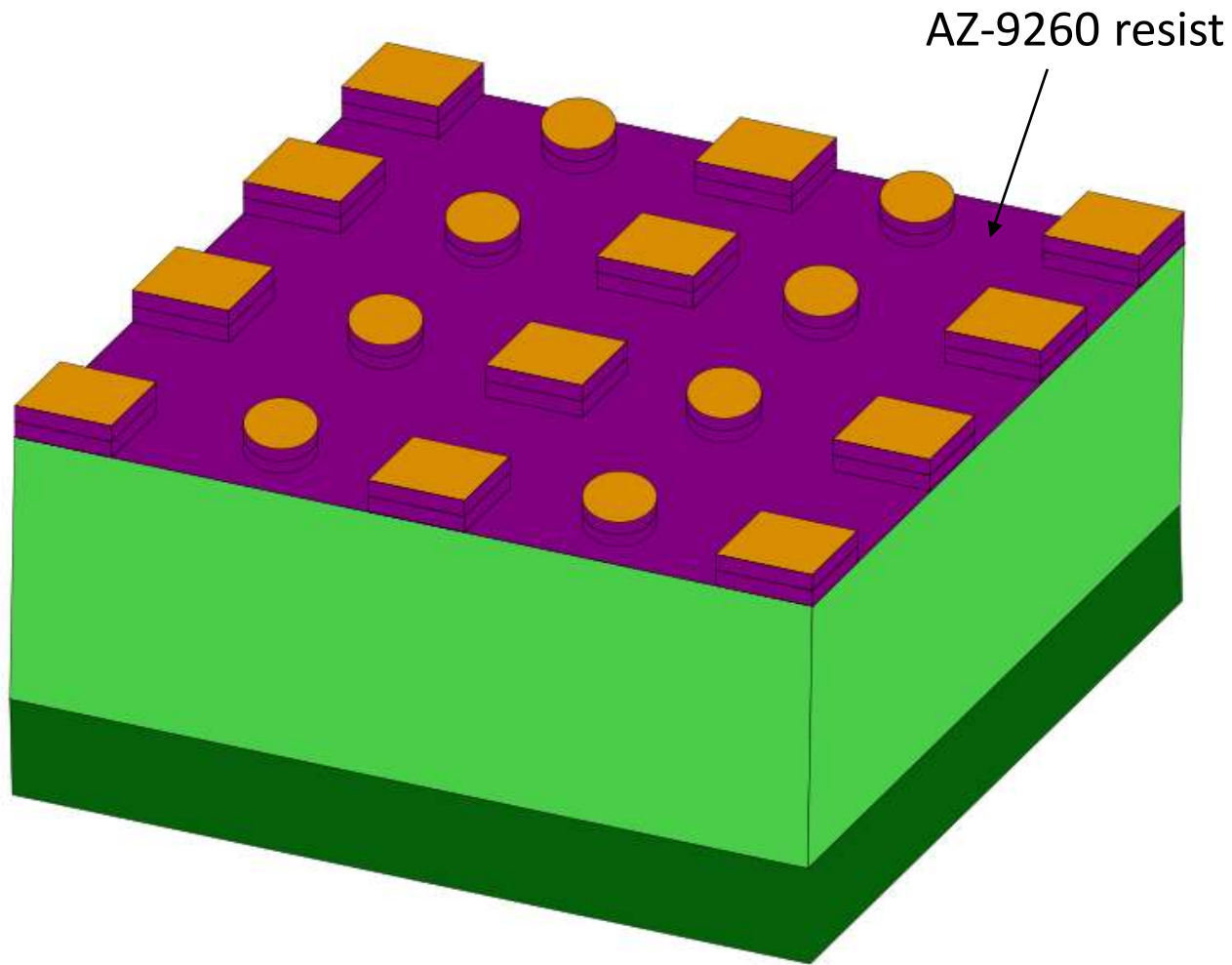
Formation of p-n diodes

RIE/ICP etching



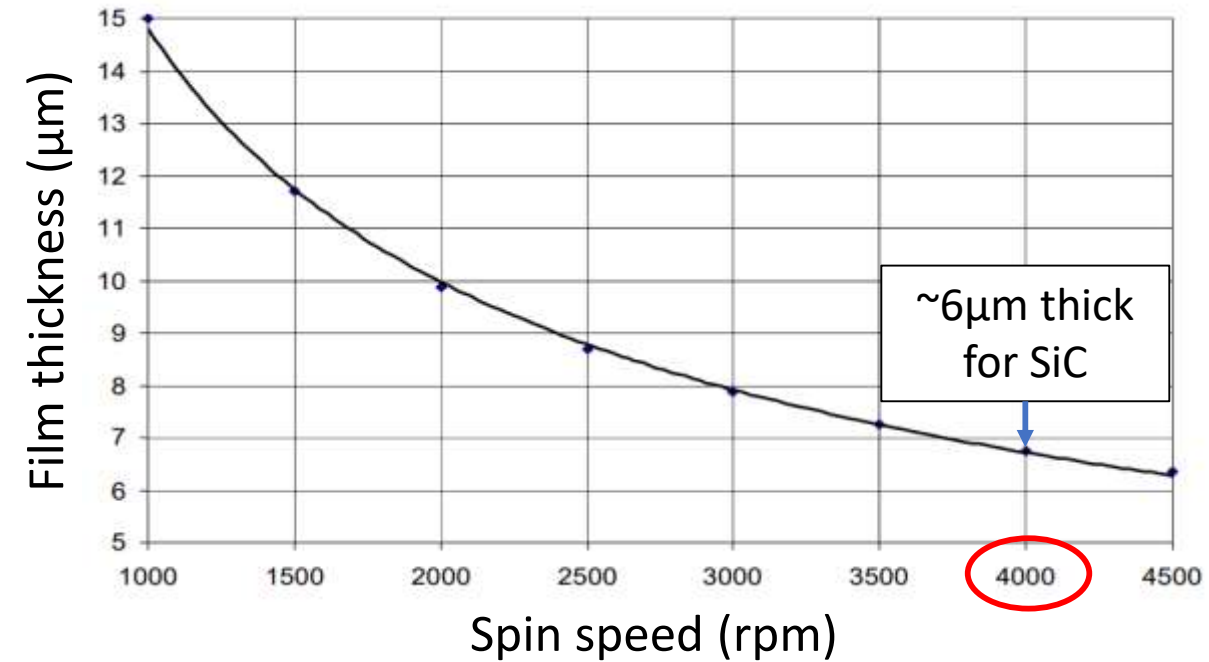
- SF6; 100/1000W
- **3 μ m etched**

1. METHOD (patented)

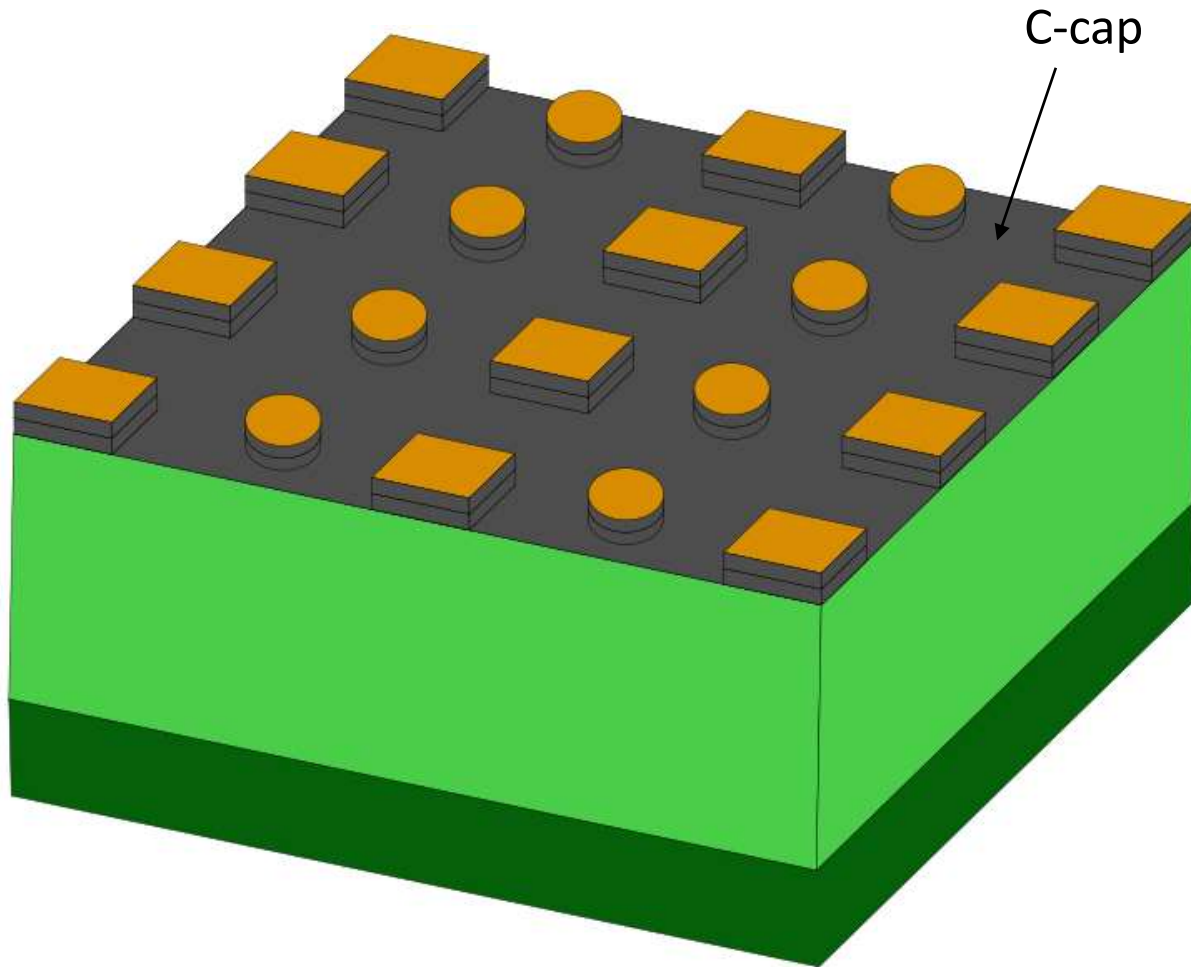


SURFACE PROTECTION

AZ-9260 thickness VS. Spin speed
(for Si substrate)



1. METHOD (patented)



SURFACE PROTECTION

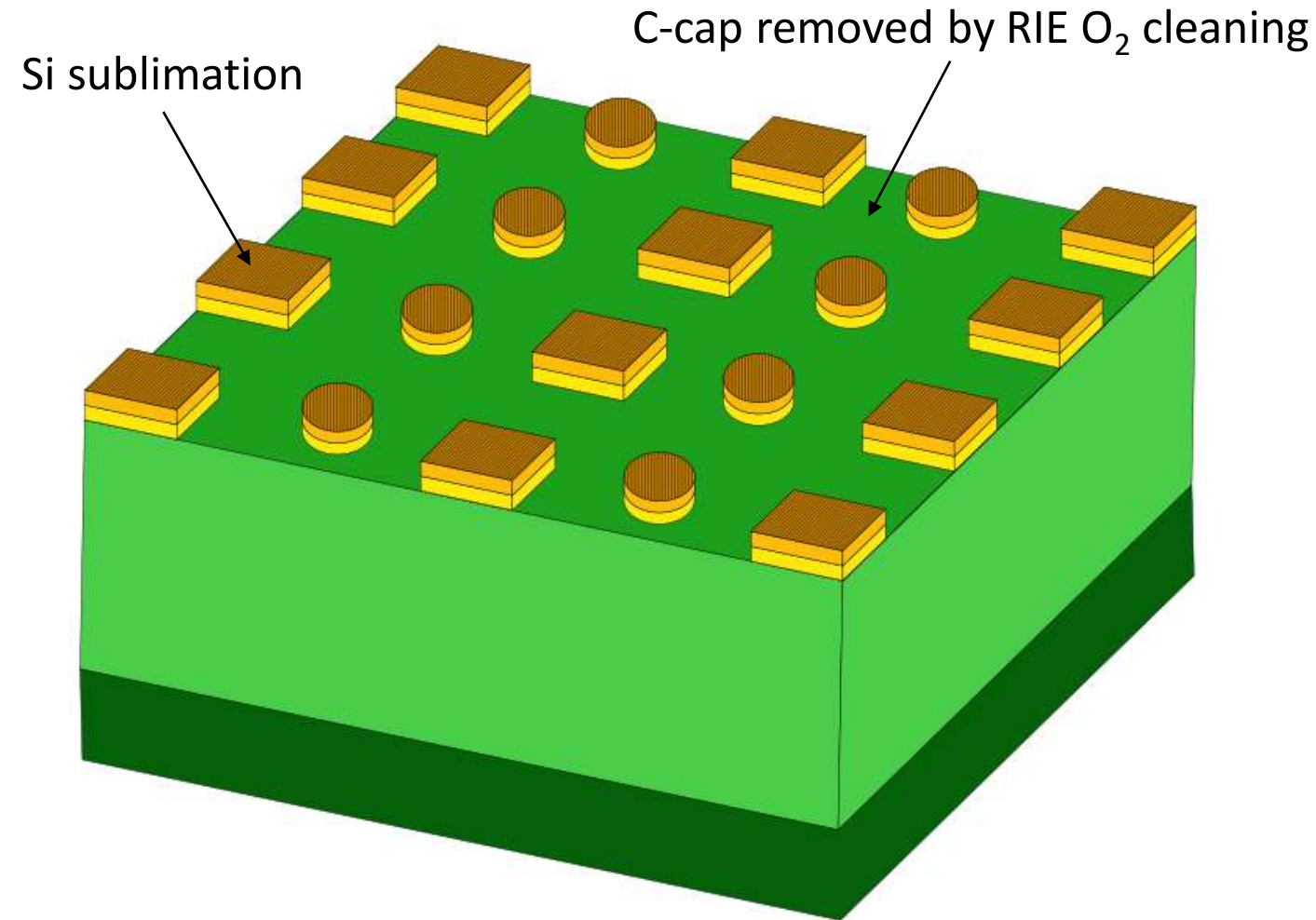


- AET pyrolysis furnace
- Heating 30min at 750°C under Ar

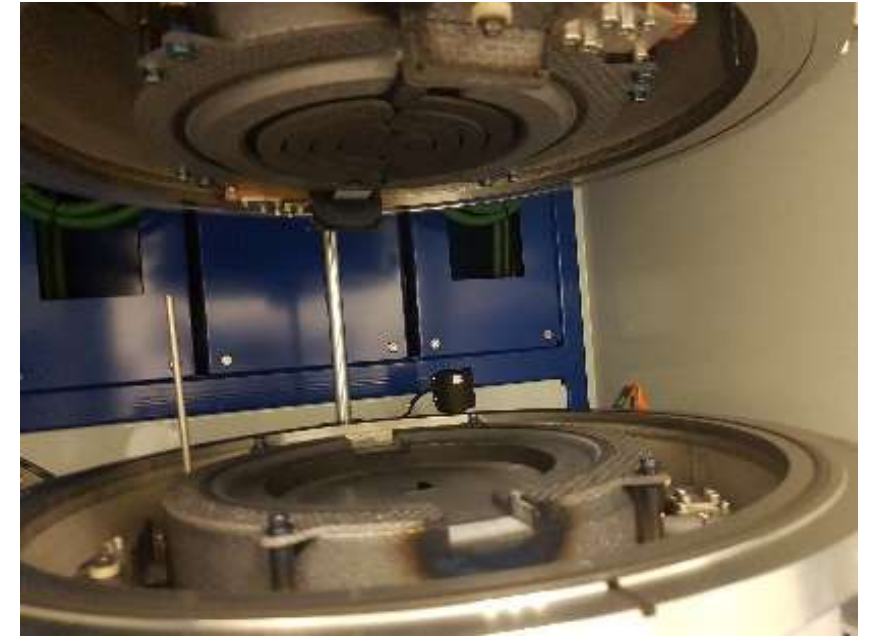
Resist → Graphite layer

Formation of p-n diodes

1. METHOD (patented)



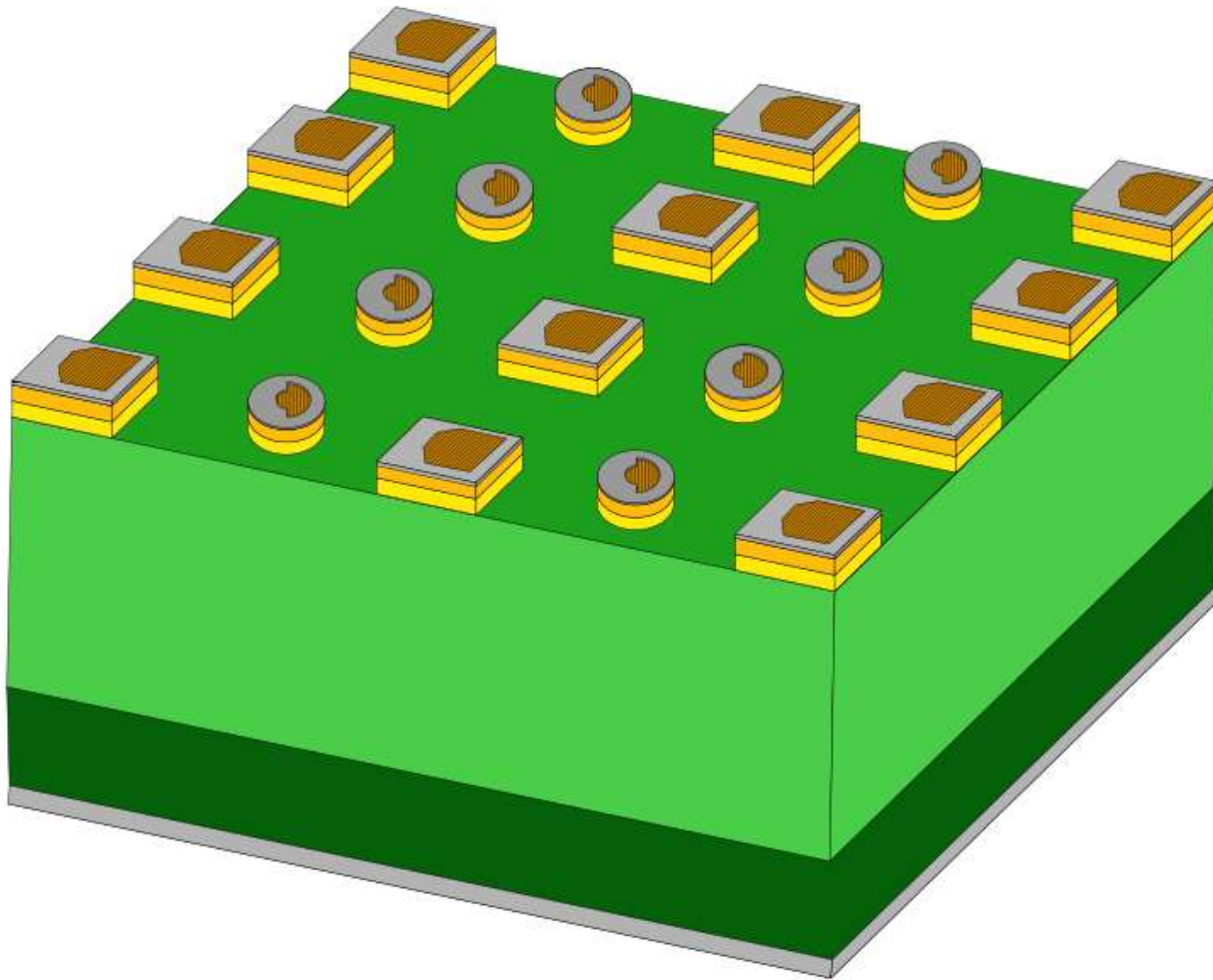
HIGH-TEMPERATURE ANNEALING



- AET RTP graphite resistive furnace
- 2°C/s heating ramp
- Heating at 1500, 1600, or 1700°C for 30min

Si sublimation → Rough surface

Formation of p-n diodes



OHMIC CONTACTS

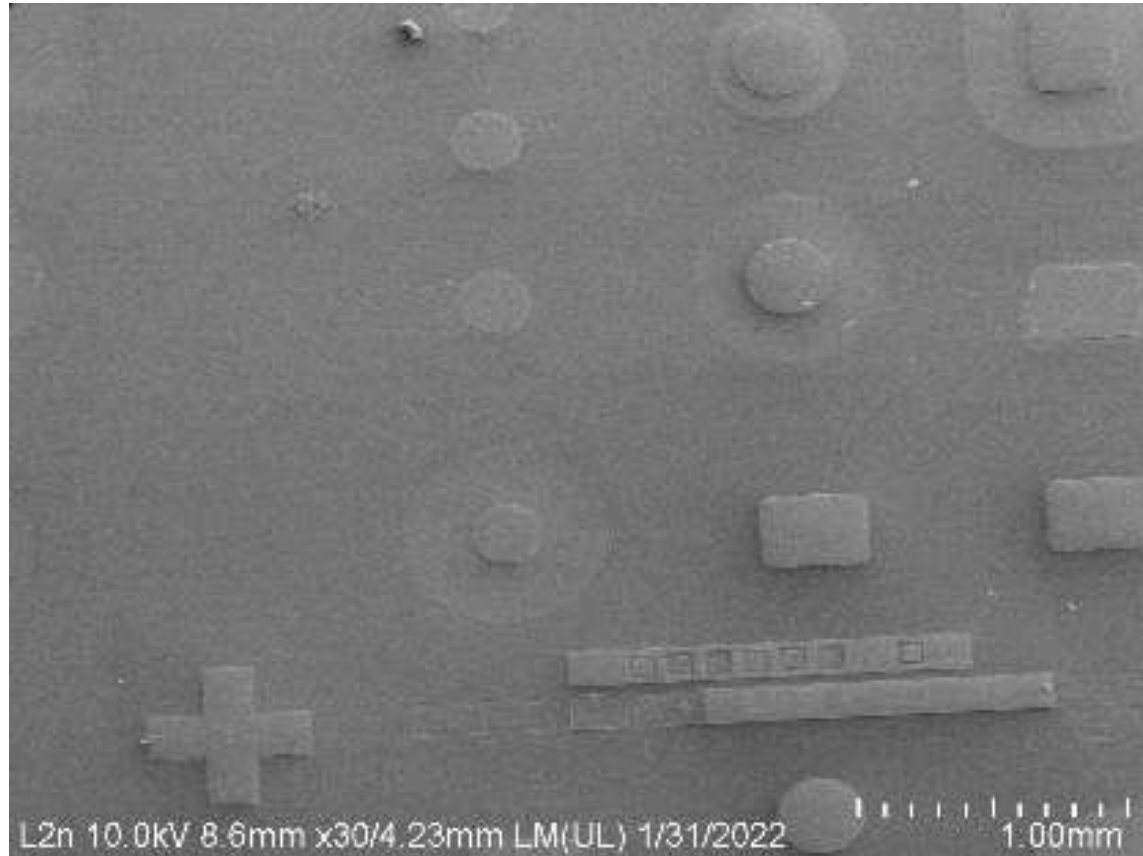
- E-beam evaporation
- Vacuum at $\sim 5 \times 10^{-6}$ bars
- Ti/Ni on the back
- Ti/Ni/Al/Ni on top
- 90s-annealing at 800 (top) or 900°C (back)

Vertical C-V measurements

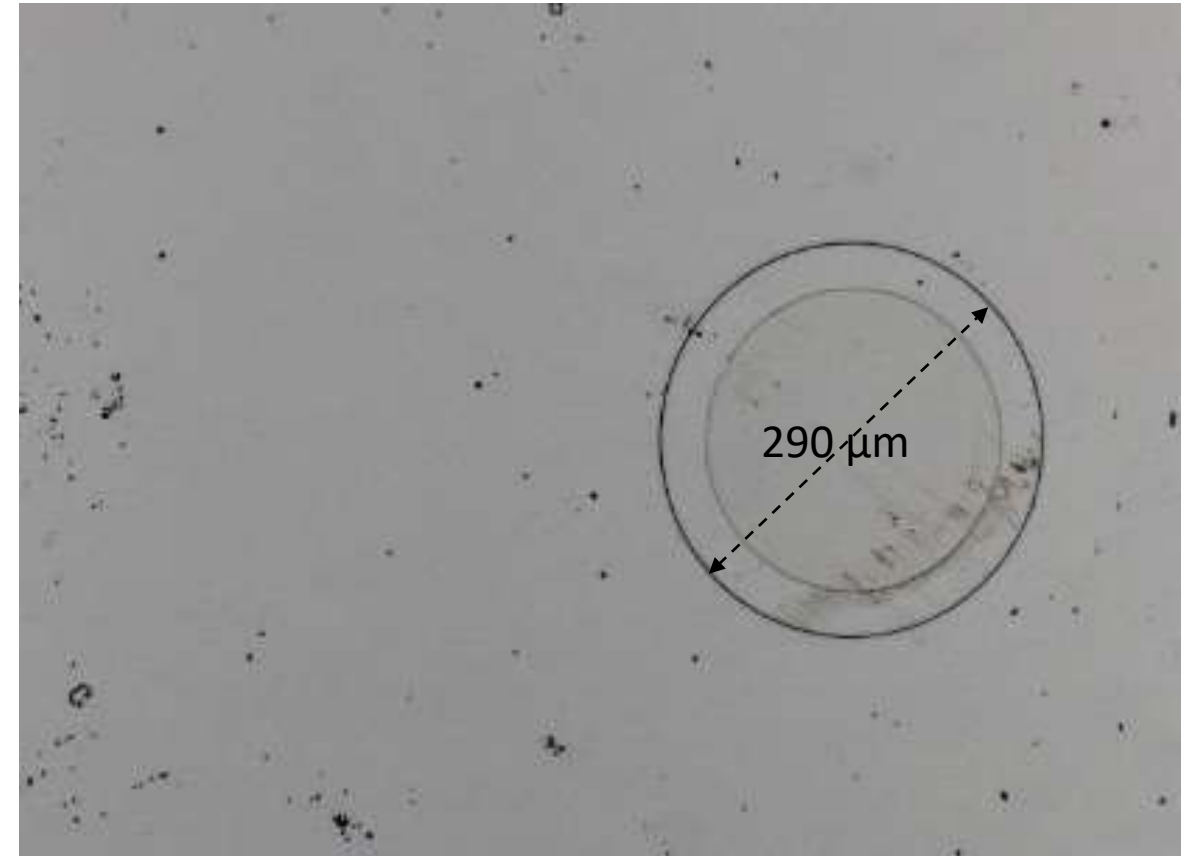
Patent: Création d'une fenêtre de sortie de rayonnement pour un composant photoémetteur, *Mihai Lazar, Dominique Planson, Hervé Morel, Gilles Lerondel, Komla Dunyo Nomenyo*. France. N° FR2201067. 2022.

2. SURFACE ANALYSIS

Surface aspect after annealing at 1700°C



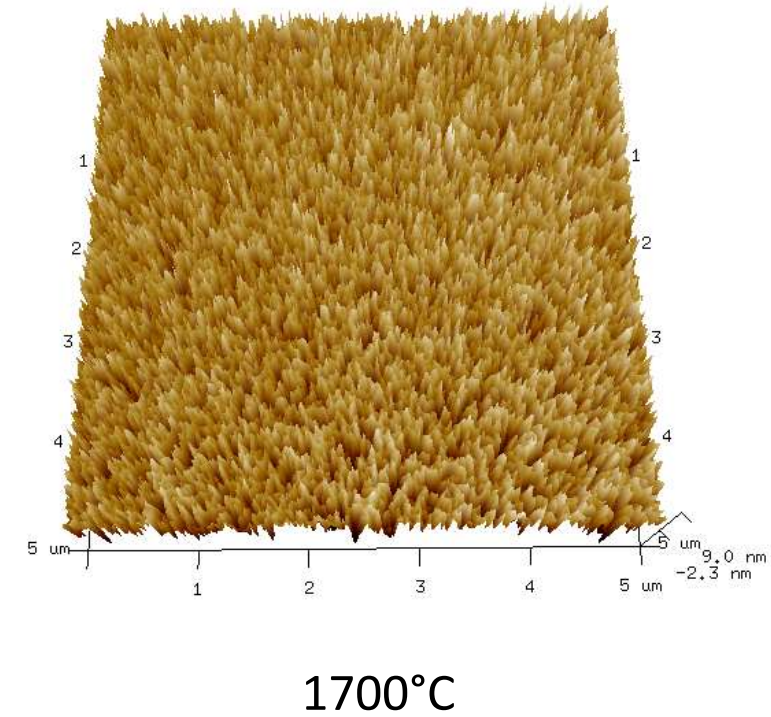
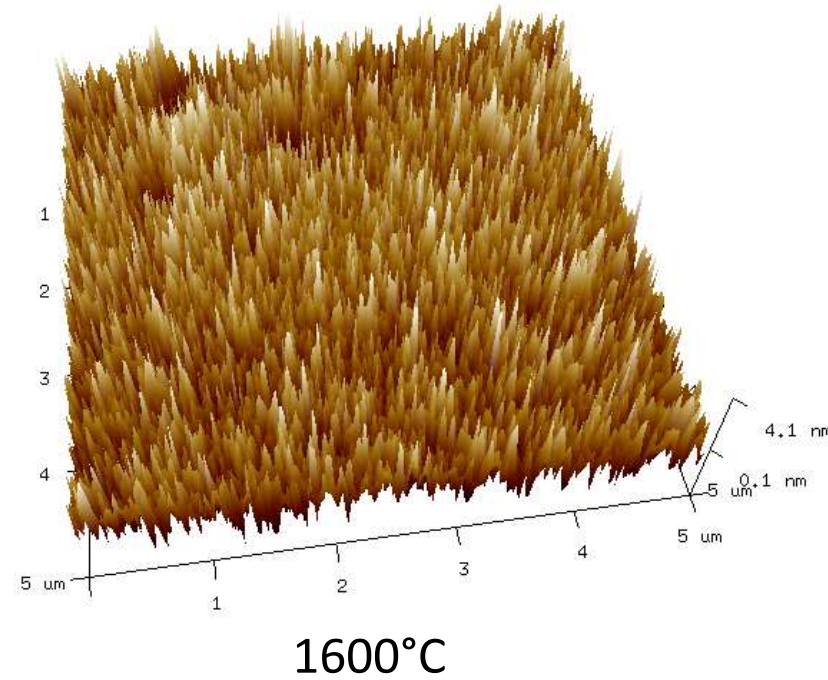
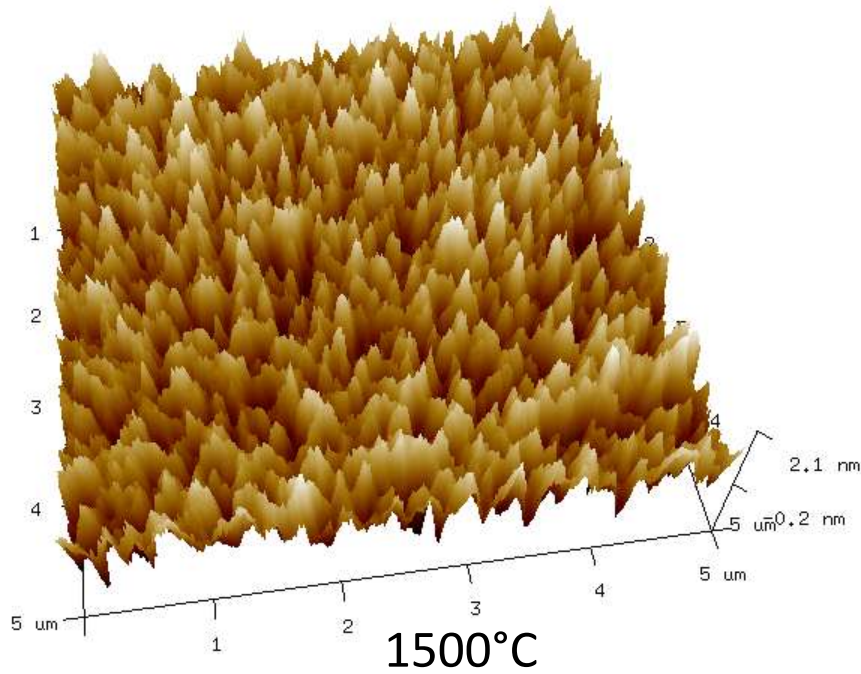
SEM



Optical microscope

2. SURFACE ANALYSIS

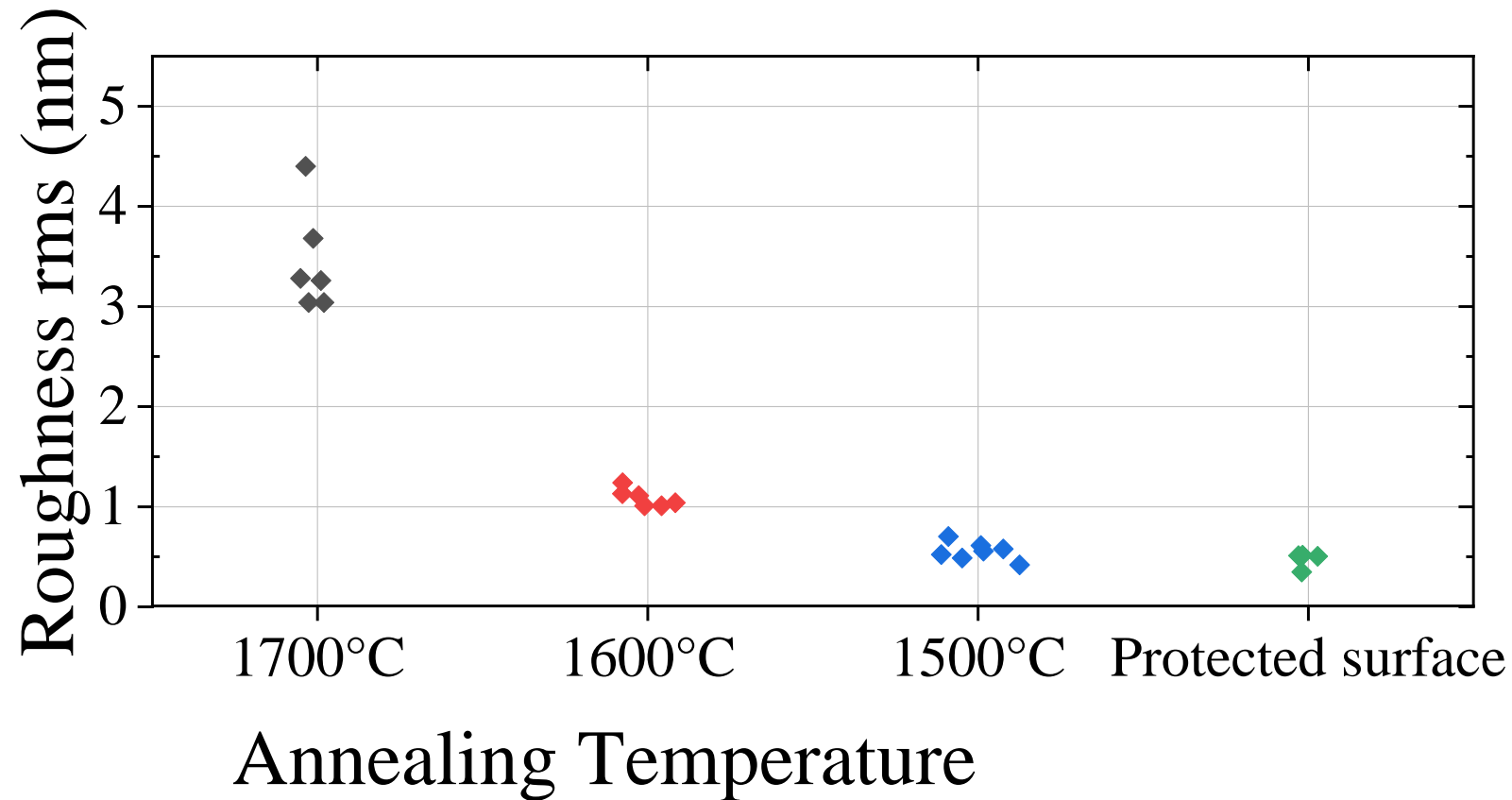
Roughness of the surface after annealing (AFM)



- Needle-shape morphology of the surface
- The needles are thinner when the annealing temperature increases

2. SURFACE ANALYSIS

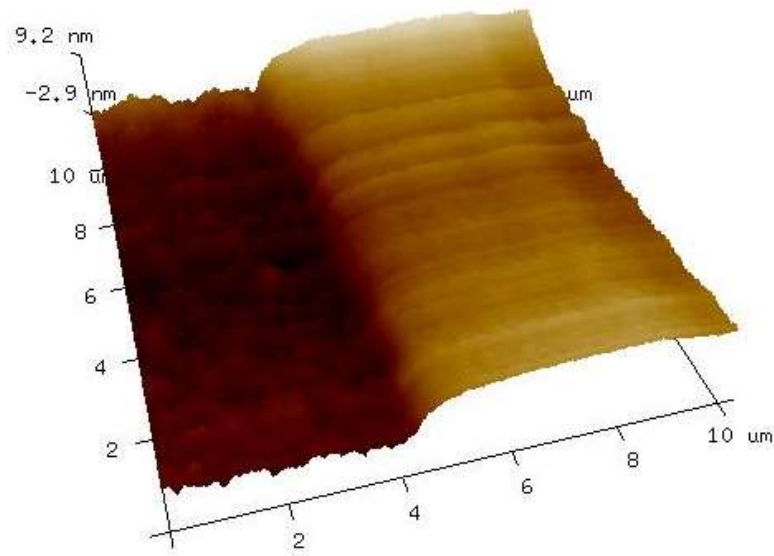
Roughness of the surface after annealing (AFM)



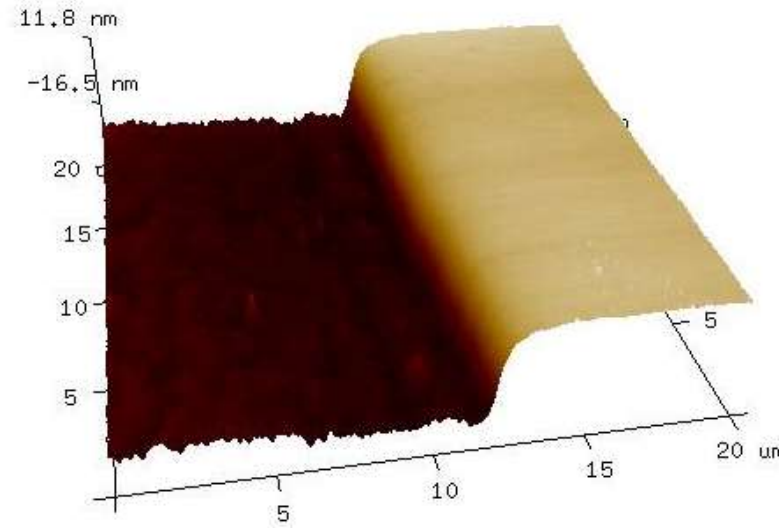
- Needle-shape morphology of the surface
- The needles are thinner when the annealing temperature increases
- The roughness increases with the annealing temperature

2. SURFACE ANALYSIS

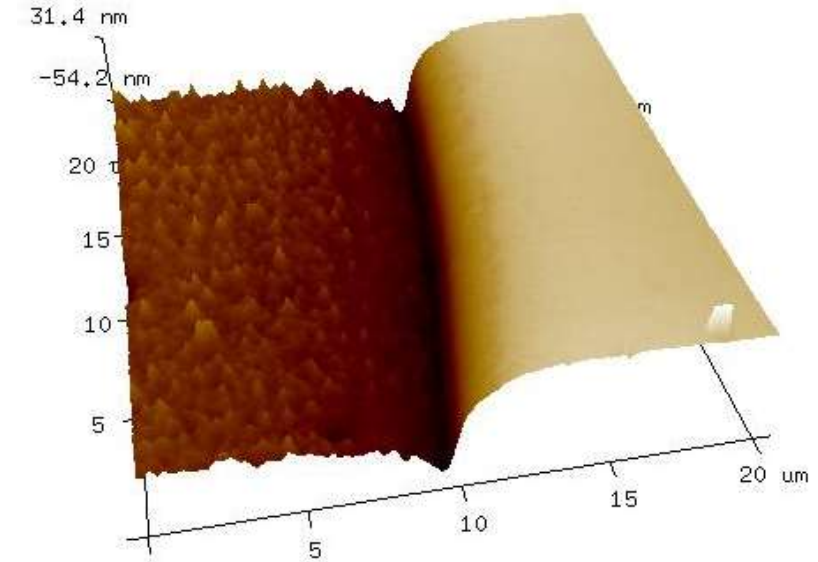
Etching of the surface after annealing



1500°C

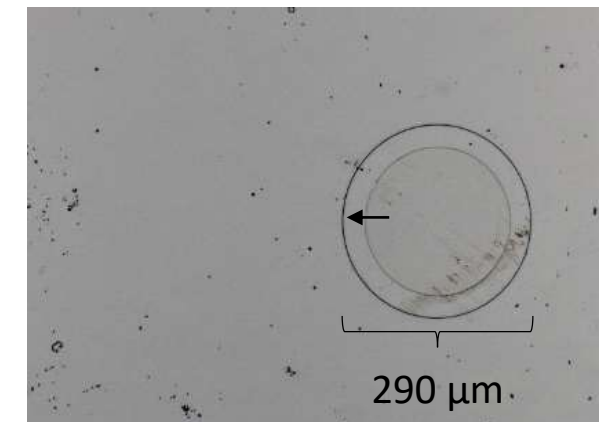


1600°C



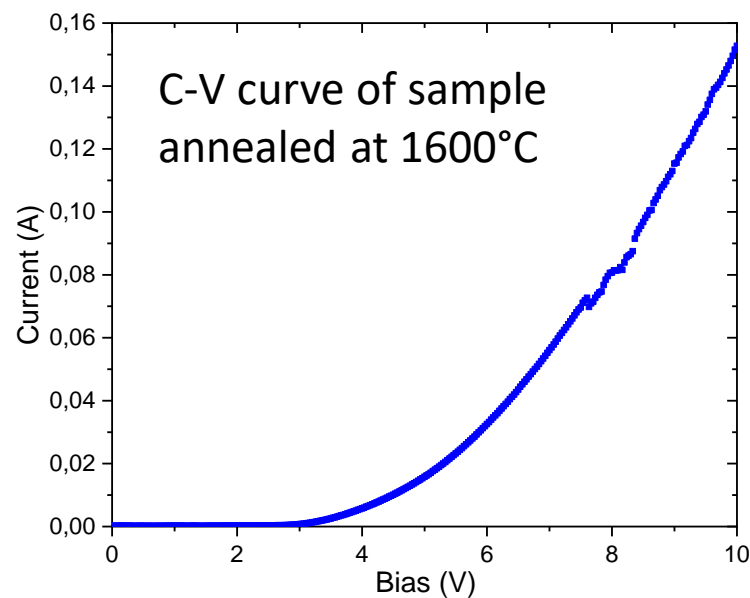
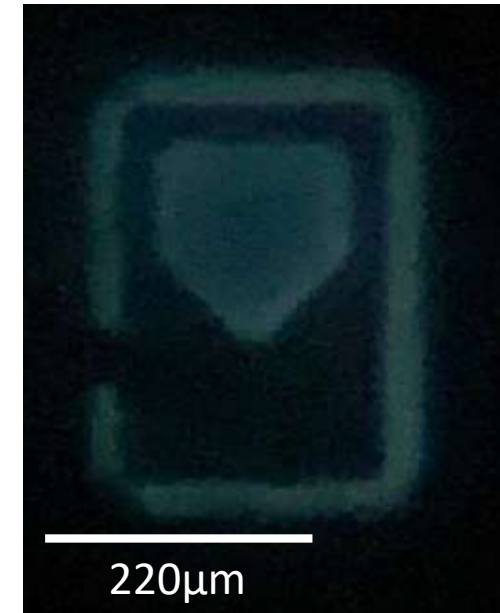
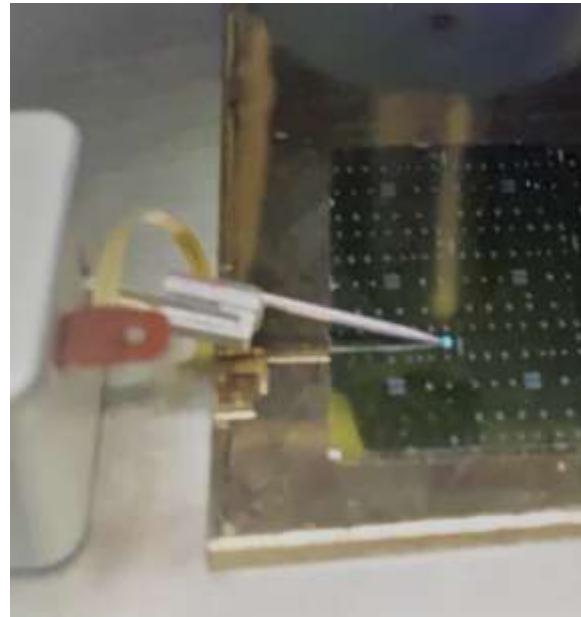
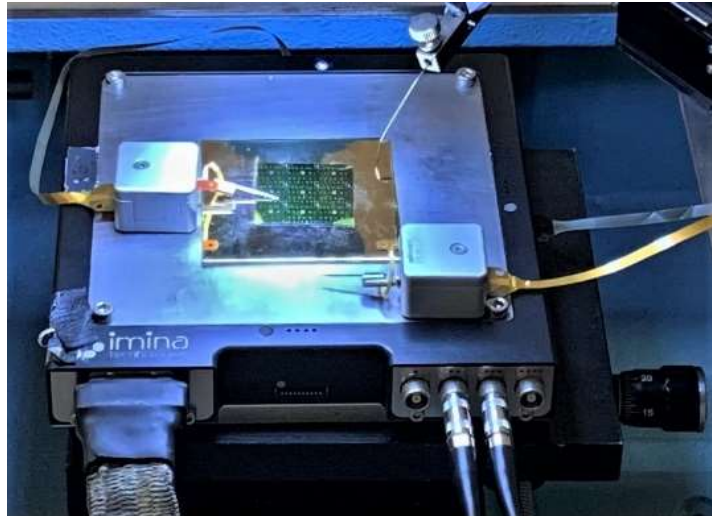
1700°C

Annealing T° (°C)	1500	1600	1700
Height of the steps (nm)	10	35	80



3. ELECTROLUMINESCENCE

Electroluminescence

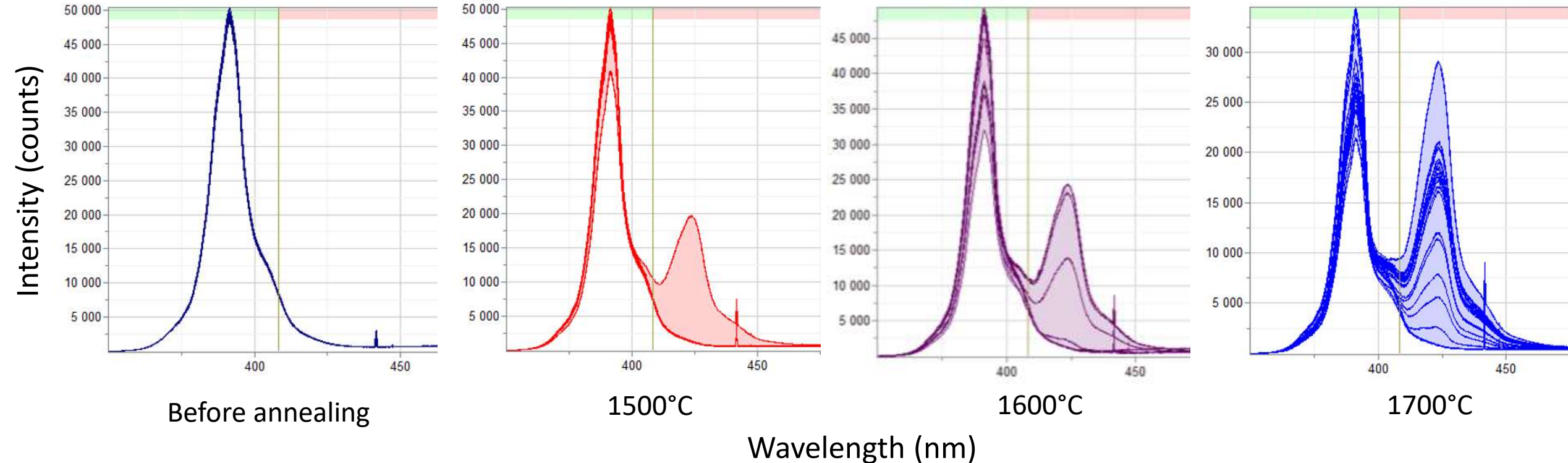


- Blue-green electroluminescence at 5V → extraction of light
- No change in intensity was seen under the microscope between the different annealing temperatures

4. PHOTOLUMINESCENCE

PL: Raman bench

UV excitation 325nm



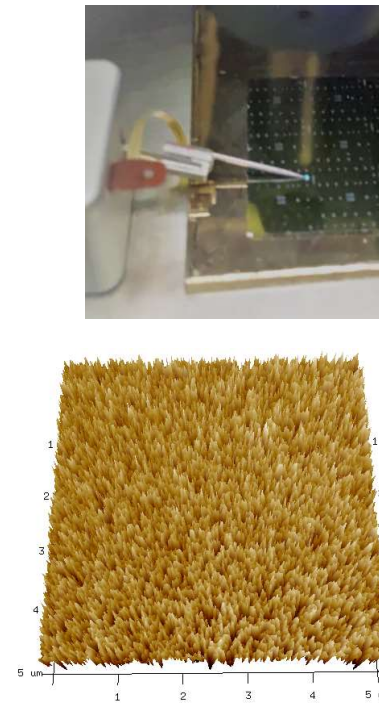
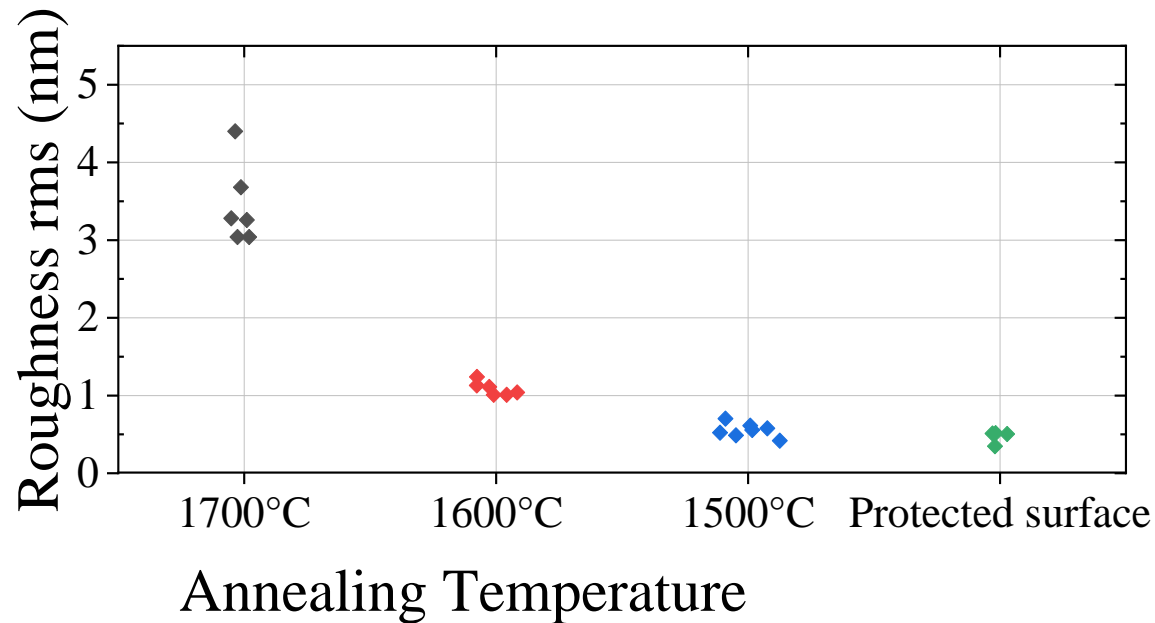
PL at 390nm \searrow when $T \nearrow \rightarrow$ phonon-assisted band-to-band recombination

PL at 420nm \nearrow when $T \nearrow \rightarrow$ peak looks like induced by stacking faults (SF)

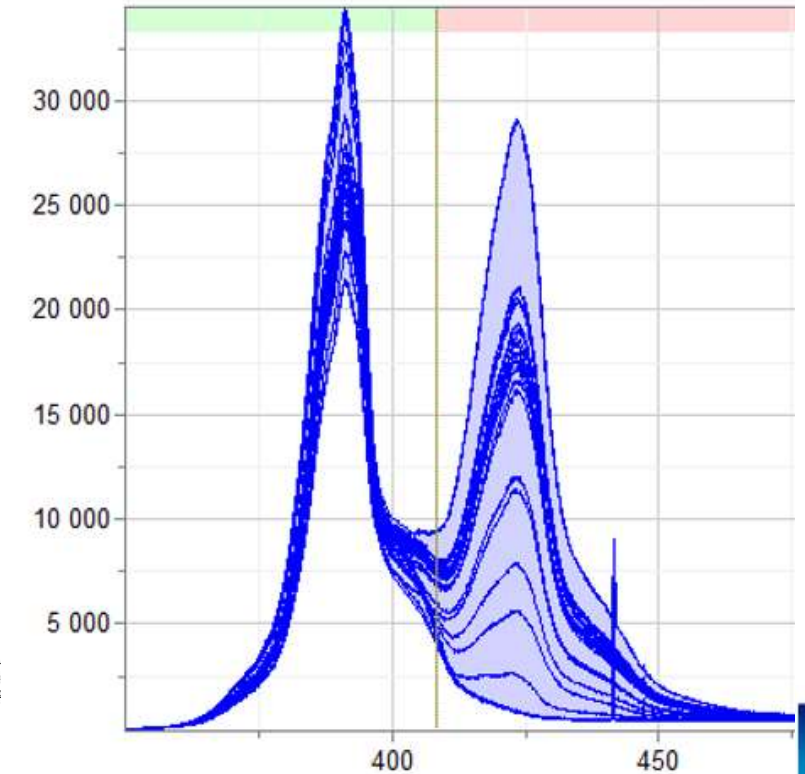
- Bipolar degradation (SF expansion)?
- Does annealing favor bipolar degradation?

CONCLUSION

- High-temperature annealing changed the surface morphology and roughness
- Slight etching of the surface occurs due to Si sublimation
- Electroluminescence of the p-n diodes obtained but not quantified (set up under revisions)
- PL measurements: high-temperature annealing induced stacking faults generation so we obtained a peak at 420nm



1700°C



1700°C

Thank you !