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# Resistive Feedback LNA design using a 7-parameter design-oriented model for advanced technologies

Mohamed K. Bouchoucha<sup>1,2</sup>, Dayana A. Pino-Monroy<sup>1,2</sup>, Patrick Scheer<sup>1</sup>, Philippe Cathelin<sup>1</sup>, Jean-Michel Fournier<sup>2</sup>, Manuel J. Barragan<sup>2</sup>, Andreia Cathelin<sup>1</sup> and Sylvain Bourdel<sup>2</sup>

<sup>1</sup>STMicroelectronics, 38920 Crolles, France, <sup>2</sup>TIMA Laboratory, Grenoble INP, Université Grenoble Alpes, 38000 Grenoble, France

**Abstract**— This paper presents a simple and efficient methodology for LNA design which uses the inversion level of the transistor as a design parameter in order to optimize the energy efficiency. The method uses a simple but accurate 7 parameter-based model valid in all regions of operation and allows an accurate preliminary sizing based on an analytical study. The proposed model describes the main short-channel effects in advanced technologies and allows an analytical evaluation of the LNA nonlinearity. A use case using a 28 nm FD-SOI technology is proposed to reflect that the methodology is well suited for designs at weak to moderate inversion level in an advanced technology for which simulation-based studies are often used for early sizing.

**Keywords**— LNA, resistive feedback, low power, inversion coefficient, 28 nm FD-SOI, design-oriented, model, non-linearity.

## I. INTRODUCTION

The new generation of IoT devices are exponentially growing all over the world [1] providing simple solutions that are improving our lifestyle. To allow a large access to these features with less impact on the environment and energy resources, the power consumption should be lowered to the minimum. These applications impose strict requirements on RF transceivers that should be designed based on new strategies targeting good performances at low power budget. This can be broken down into constraints on the Low Noise Amplifier (LNA) which is the key block in the overall receiver chain performance (excluding mixer-first receivers).

Taking advantage of advanced CMOS technologies with their high  $f_T$  and  $f_{max}$ , RF designs outside of the classical strong inversion region become possible. However, designing in moderate and weak inversion regions in advanced nanometric technologies is a challenging task, usually relying on lengthy simulation-based optimization loops due to the complexity of short-channel transistor behavior. In this regard, different simplified design methodologies have been proposed for exploring the moderate and weak inversion regions of operation. A branch of these solutions is based on some figures of merits (FoM) such as  $g_m f_T / I_D$  [2] or  $g_m^2 / I_D$  [3]. More recent strategies rely on optimizing a particular FoM by selecting the optimal inversion level of the transistors [4]. Although using FoM or even Look Up Tables (LUT) [5], is accurate and provides good design solutions, it does not explicitly capture the drain voltage  $V_D$  dependence of the transistor metrics and does not provide explicit analytical relationships of the nonlinearity effects. In this paper, we propose a design methodology for a resistive feedback (Rfeedback) LNA. It is based on the  $g_m / I_D$  efficiency factor and the inversion coefficient  $i_d$  that bridge the gap between LNA constraints and transistor sizing and bias conditions. It replaces the LUT with a simple design-oriented model [6] to describe the transistor behavior in all

regimes taking into account the  $V_D$  variation and, for the first time, describes accurately the nonlinearity performance. Hence, as an improvement of [7], for a set of power, gain, noise and linearity specification targets, the designer can navigate the design space selecting the optimal inversion level and component sizes.

The rest of the paper is organized as follows. In Section II, the analytical equations of the Rfeedback-LNA are introduced. Section III presents the design-oriented model [6] used in this work. Then, section IV describes the sizing method and details the implementation in a 28 nm FD-SOI technology with performance comparison between analytical and simulation results. Finally, section V summarizes our main contributions.

## II. RESISTIVE FEEDBACK LNA

The basic architecture of the RFeedback LNA is shown in Fig. 1. The equivalent load resistor  $R_l$  corresponds to  $R_{l0}$  in parallel with  $r_o$  (equivalent admittance equals to the transimpedance  $g_{ds}$ ). It is related to the real part of the input impedance at the gate of the transistor  $V_1$  expressed in (1).

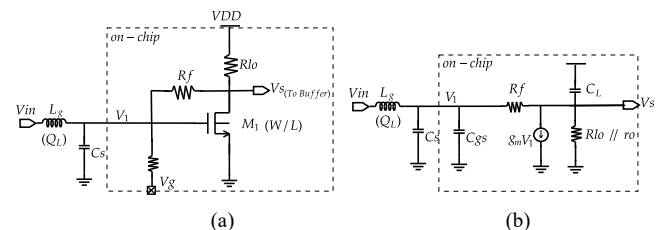


Fig. 1: RF-LNA topology a. and its small signal equivalent circuit b.

$$R_p = \frac{R_l + R_f}{1 + g_m R_l} \quad (1)$$

The quasi-static voltage gain can be expressed as,

$$|G_v| = \left| \frac{V_s}{V_1} \right| = \frac{|g_m R_f - 1| R_l}{R_l + R_f} \quad (2)$$

As the operation frequency increases, this gain is attenuated by the effect of the bandwidth limitation as,

$$|G_o| = \frac{|g_m R_f - 1| R_l}{(R_l + R_f) \sqrt{\left(1 + \left(\frac{\omega_0}{2\pi B_w}\right)^2\right)}} \quad (3)$$

where  $\frac{\omega_0}{2\pi}$  is the operating frequency and  $B_w$  is the bandwidth that can be estimated as,

$$B_w = \frac{R_l + R_f}{2\pi R_f R_l C_l} \quad (4)$$

The maximum noise factor of the on-chip circuit considering the transistor channel and the source,  $R_g$ , the feedback and

$$F_{max} = 1 + \frac{(1 + g_m R_g)^2 R_f}{R_g (1 - g_m R_f)^2} + \frac{\gamma g_m (R_g + R_f)^2}{R_g (1 - g_m R_f)^2} + \frac{(R_g + R_f)^2}{R_g R_l (1 - g_m R_f)^2} \quad (5)$$

the load resistances contributions is expressed as, where  $\gamma$  is the excess noise factor of the MOS transistor.

For impedance matching considerations, an  $LC$  network composed of an inductor  $L_g$  in series and a parallel capacitor  $C_s$ , is inserted at the input of the LNA. The main objective is to cancel the capacitive imaginary part of the input impedance and set its real value to  $50 \Omega$ , so it matches  $R_g$  for higher power transmission. Also, it improves the gain and reduces the noise. The input impedance at the on-chip input node of the LNA ( $V_1$ ), denoted by  $Z_p$  can be expressed as,

$$\frac{1}{Z_p} = \frac{1}{R_p} + C_t p, \quad (6)$$

where  $R_p$  is the equivalent real part expressed in (1) and  $C_t$  is the total capacitance at the input expressed as,

$$C_t = C_s + C_{gs} + C_p, \quad (7)$$

where  $C_{gs}$  is the transistor gate to source capacitance of the transistor.  $C_s$  is the off-chip added capacitance to ensure impedance matching and  $C_p$  is the equivalent capacitance at  $V_1$  expressed by the gain and the loads of the LNA as,

$$C_p = \frac{R_l^2 C_l (g_m R_f - 1)}{(R_l + R_f)^2} \quad (8)$$

Using the parallel to series impedance conversion, the input resistance  $R_{in}$  to be matched to the source  $R_g$  is expressed in (9) and the input capacitance  $C_{in}$  is expressed in (10) as,

$$R_{in} = \frac{R_l + R_f}{(1 + g_m R_l)(1 + Q^2)} \quad (9)$$

$$C_{in} = \frac{C_t(1 + Q^2)}{Q^2} \quad (10)$$

Hence, by introducing the series inductor  $L_g$  the quality factor expression becomes,

$$Q = \frac{L_g \omega}{R_{in}} \quad (11)$$

$L_g$  resonates with  $C_{in}$ , at the working frequency  $\omega_0$ ,

$$\omega_0 = \sqrt{\frac{1}{L_g C_{in}}} \quad (12)$$

As a result, the complete total gain can be expressed as,

$$G_t = G_o \sqrt{1 + Q^2} \quad (13)$$

The linearity performances of the on-chip circuit can be evaluated through the input referred third intercept point  $IIP_3$  at  $V_1$ . The equivalent  $V_{IIP_3}$  voltage can be approximated using the transistor metrics by,

$$V_{IIP_3} \cong 2 \sqrt{\frac{2g_m}{g_{m3}}} \quad (14)$$

with  $g_{m3}$  is the third derivative of the drain current.

### III. 7-PARAMETER DESIGN-ORIENTED MODEL

A wide variety of design-oriented models have been developed to describe the MOS transistor in all regions of operation as CMOS technologies advance. The most used are the ACM [8] and EKV [9] models, which are both charge-based models that use a similar set of equations. In this work,

we use the ACM terminology and equation sets but the given methodology can be also derived following the EKV formalism. For the sake of simplicity, and with the aim of deriving simple analytical expressions which can be easily handled for design, we used a simplified design-oriented model which takes into account the most important short-channel effects (SCE). It is based on 7 physical parameters (7PM) as an extension of the basic 3-parameter version used in [7]. The 3 basic parameters in the model describe the long channel transistor behavior via the slope factor  $n$ , the normalized specific current  $I_{S0}$  and the threshold voltage  $V_{T0}$ . The 4 additional parameters in the 7PM model allow a calculation of the current as a function of  $V_D$  from the linear to the saturated region of the transistor and for all inversion regimes thanks to taking into account the main SCEs. These 4 additional parameters include the drain induced barrier lowering parameter,  $\sigma$ , the velocity saturation,  $\zeta$ , the carrier mobility reduction effect,  $\theta$  and the channel length modulation  $V_E$ . This version of the model has shown good accuracy in all regimes validated through measurements. An example of the  $I_D$ - $V_G$  characteristic comparison with measurements is shown in Fig 2.a. The interested reader is referred to [6] for a detailed description of this model. Given the very high available  $f_T$  of the 28 nm FD-SOI,  $L = 60 \text{ nm}$  is chosen to increase the gain margin. The main parameters of the transistor are given in TABLE I for  $W = 1 \mu\text{m}$ .

TABLE I. 60 nm LVT-RF MOS CHARACTERISTICS

$n$	$I_{S0}(\mu\text{A})$	$V_{T0}(\text{mV})$	$\sigma$	$\zeta$	$\theta$	$V_E(\text{V})$
1.138	3.25	390.5	0.018	0.056	0.079	15

The model is based on the normalized inversion charges at the source and drain terminals of the transistor,  $q_S$  and  $q_D$  given by,

$$q_{S(D)} = \frac{Q'_{IS(D)}}{Q'_{IP}} \quad (15)$$

where,  $Q'_{IS}$  and  $Q'_{ID}$  are the inversion charges at source and drain, respectively.  $Q'_{IP} = -nC'_{ox}U_T$ , is the inversion charge density at pinch-off, and  $C'_{ox}$  is the oxide capacitance per unit area. Under saturation condition,  $q_D$  is noted by  $q_{Dsat}$  and is directly linked to the saturation current  $i_{Dsat}$  by  $i_{Dsat} = \frac{2q_{Dsat}}{\zeta}$ . Hence,  $q'_D$  is used to express the drain density in all regions.  $q_S$  and  $q'_D$  can be related to the terminal voltages as,

$$\frac{V_p - V_{S(D)B}}{U_T} = q_{S(D')} - 1 + \ln(q_{S(D')}) \quad (16)$$

where  $V_p$  is the pinch-off voltage, linearly approximated by

$$V_p = \frac{V_{GB} - V_{T0} + \sigma(V_{SB} + V_{DB})}{n} \quad (17)$$

The specific current  $I_{S0}$  is given by,

$$I_{S0} = \mu_n C'_{ox} n \frac{U_T^2 W}{2L} \quad (18)$$

where  $\mu_n$  is the electron mobility,  $U_T = kT/q$  is the thermal voltage,  $L$  and  $W$  are the transistor length and width respectively. As a result, in the MOS transistor, the drain current with the main SCE can be expressed as,

$$I_D = I_{S0} \frac{(q_S - q_{D'}) (q_S + q_{D'} + 2)}{1 + \theta \left( \frac{q_S + q_{D'}}{2} \right)} \left( 1 + \frac{V_{DS} - \sqrt[4]{\frac{V_{DS}}{1 + \left( \frac{V_{DS}}{V_{DSsat}} \right)^4}}}{V_E} \right) \quad (19)$$

with  $V_{DSSat} = U_T \left( q_s - q_{Dsat} + \ln \left( \frac{q_s}{q_{Dsat}} \right) \right)$

The presented model accurately captures the DC and small-signal characteristics of the transistor [6], with simple expressions of the current and its derivatives. The small-signal behavior description is fundamental for a design-oriented model since it provides explicit analytical expressions of  $g_m$ ,  $g_{m2}$  or  $g_{m3}$  that are directly related to the main LNA performances such as the gain, noise figure and  $IIP_3$ . For instance, the normalized expressions of the transconductance  $g_m$ , which is the derivative of  $i_d = I_D/I_{S0}$  with respect to the normalized gate voltage,  $v_g = V_G/U_T$ , and the second and third derivatives of the drain current  $g_{m2}$  and  $g_{m3}$  are expressed as.

$$g_m = \frac{\partial i_d}{\partial v_g} = 2 \frac{E}{D + \frac{\theta}{2} E} \frac{1}{n} \frac{q_S}{A} \quad (20)$$

$$g_{m2} = \frac{2}{n^3 B} \left[ \frac{q_S}{A} - \frac{q_D}{C} - \frac{\theta}{4} \left[ 2n g_m \left( \frac{q_S}{A} + \frac{q_D}{C} \right) + i_d \left( \frac{q_S}{A^3} + \frac{q_D}{C^3} \right) \right] \right] \quad (21)$$

$$g_{m3} = \frac{2}{n^3 B} \left[ \frac{q_S}{A^3} - \frac{q_D}{C^3} - \frac{\theta}{4} \left[ 3n^2 g_{m2} \left( \frac{q_S}{A} + \frac{q_D}{C} \right) + 3n g_m \left( \frac{q_S}{A^3} + \frac{q_D}{C^3} \right) + i_d \left( \frac{q_S(1-2q_S)}{A^5} + \frac{q_D(1-2q_D)}{C^5} \right) \right] \right] \quad (22)$$

With  $A = 1 + q_s$ ,  $B = 1 + \frac{\theta}{2}(q_s + q_D)$ ,  $C = 1 + q_D$ ,  $D = 1 + \zeta - \frac{\theta}{2} + q_{Dsat} \left( \zeta + \theta + \frac{\theta^2}{2\zeta} \right)$ ,  $q_{Dsat}$  is  $q_D$  under saturation and  $E = \sqrt{1 + q_{Dsat} \left( 2 + \frac{2}{\zeta} - \frac{\theta}{\zeta} \right) + q_{Dsat}^2 \left( 1 + \frac{\theta}{\zeta} + \frac{\theta^2}{4\zeta^2} \right)}$ .

As an illustrative example, the  $g_m/I_D$  efficiency factor,  $g_m$  and  $g_{m3}$  are shown in Fig 2. b, c and d respectively, for a  $L=60$  nm transistor in the selected 28 nm FD-SOI technology.

#### IV. LNA SIZING

The design methodology relies on the analytical expressions of the LNA main characteristics shown in section II together with the 7PM transistor equations that capture the behavior of the device in all regimes while varying  $V_D$ . For gain, noise figure, linearity and power budget requirements, the strategy allows to navigate in the design space until reaching the optimal component sizes and working points.

##### A. Design Methodology

In the context of low power application, we target sub-1mW circuits. For a minimum intrinsic gain  $G_{vmin} = 10$  and maximal noise figure  $F_{max}$  close to 2 (before improvement using  $Q$ ), the resistances values and the sizes of the transistor are determined for a maximum of  $IIP_3$ . Actually, with the current constraint, a direct relationship can be derived between  $R_l$  and the drain voltage  $V_{DS}$  as,

$$R_l = \frac{V_{DD} - V_{DS}}{I_D} \quad (23)$$

In the other hand, the gain and noise figure ((2) and (5)) set conditions on  $g_m$ ,  $R_f$  and  $R_l$  while the  $IIP_3$  is directly related to  $g_m$  and  $g_{m3}$ . In this work, we use analytical expressions derived from the 7PM model to link the transistor parameters  $g_m$ ,  $g_{m3}$  and  $g_m/I_D$  to the inversion level  $i_d$  taking into account the dependency on  $V_{DS}$ , which in turn allows a direct extraction of the optimal design parameters  $V_{GS}$  and  $W$ .

For the matching network, the input impedance  $R_p$  is computed following (1). The value of the quality factor to

match the LNA to  $50 \Omega$  is derived from (9). At the target working frequency  $f_0 = 2\pi w_0$  the inductor  $L_g$  value is selected from (11). And the adequate parallel capacitance  $C_s$  completes the sizing for a given load capacitance. Then the bandwidth and the total gain are evaluated from (4) and (13) respectively and are compared to the specifications. This allows to rapidly decide on relaxing some constraints when no solution is found and repeat the procedure until the sizing is completed.

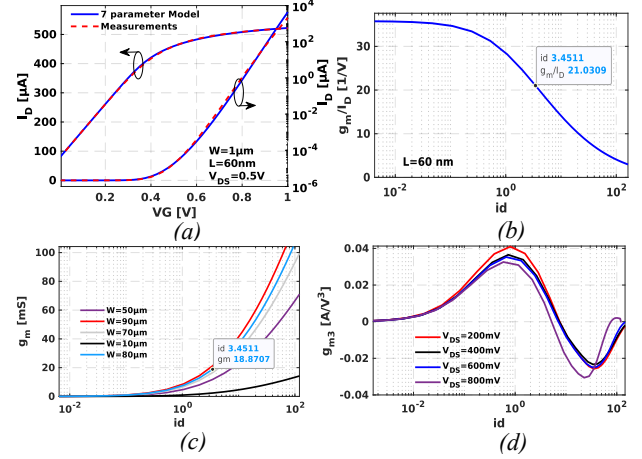


Fig. 2: a. 7PM model and measurements comparison of  $I_D$ - $V_G$  characteristic of the NMOS for  $W=1 \mu\text{m}$ ,  $L=60$  nm and  $V_{DS}=0.5$  V, b.  $g_m/I_D$  relationship for  $L=60$  nm, c.  $g_m$  as function of  $i_d$  for different  $W$  at  $V_{DS}=0.4$  V. d.  $g_{m3}$  as function of  $i_d$  for  $W=1 \mu\text{m}$  and  $L=60$  nm for different  $V_{DS}$ .

##### B. Design Cases

To demonstrate the efficiency of the model and its ability to deal with different drain voltages (which is appealing for ultra-low voltage design) three design case studies are described in this paper. Thus, we will target three different LNA designs with a  $V_{DS}$  of 200 mV, 400 mV and 600 mV while  $V_{DSSat} = 160$  mV in the 28 nm FD-SOI technology with  $V_{DD} = 1$  V and  $L = 60$  nm. The corresponding circuits are noted circuit I, circuit II and circuit III respectively. To illustrate the methodology, the sizing procedure for circuit II is detailed in this section.

In this case study we target a power consumption of 0.9 mW, a gain higher than 20 dB with  $NF < 2$  dB. Also, an  $IIP_3 > -10$  dBm and a  $B_w > 3$  GHz are required. Thus, for  $V_{DD} = 1$  V it follows that  $I_D = 0.9$  mA and  $R_l = 660 \Omega$ . For an intrinsic voltage gain higher than 10 ( $G_{vmin} = 10$ ) so that the total gain  $G_t$  could exceed 25 dB and a 10% variation of the maximal noise factor close to 2 (without the effect of  $Q$ ) will set the relationship between  $g_m$  and  $R_f$  as shown in Fig 3 allowing to explore the design space. The minimal  $IIP_3$  requirement of -10 dBm sets the inversion level  $i_d$  as shown in Fig 4.a. Selecting  $g_m = 18.92$  mS and  $R_f = 2650 \Omega$  results in an intrinsic gain  $G_v = 10.2$  and  $F = 2.089$ . For  $IIP_3 = -8.7$  dBm,  $g_{m3} = 2.8$  A/V<sup>3</sup>. Then the  $g_m/I_D$  factor that is independent on geometrical sizes is verified and equals  $21$  V<sup>-1</sup>. As shown in Fig 2.b this corresponds to an inversion level  $i_d = 3.45$ . At this condition, the width of the transistor is  $W = 80 \mu\text{m}$  and  $V_{GS} = 387$  mV as shown in Fig 2.c.

The input impedance (1) is  $R_p = 248.5 \Omega$ . Hence, the required quality factor  $Q$  of the input matching network (9) is  $Q = 1.99$ . Then the inductor  $L_g$  and the capacitor  $C_s$  are derived at 2.4 GHz. The obtained values are  $L_g = 6.6$  nH and

$C_s = 0.34$  pF for a load capacitance  $C_l = 0.1$  pF. The total gain  $G_t$  is computed and equals 22.7 which results in 27 dB for perfect matching without input attenuation. The 3-dB bandwidth is  $B_w = 3.04$  GHz which is in line with our set of specifications.

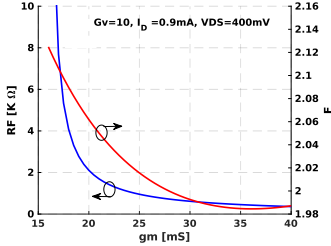


Fig. 3:  $R_f$  and  $g_m$  for  $G_v=10$ ,  $I_D=0.9$  mA and  $V_{DS}=0.4$  V

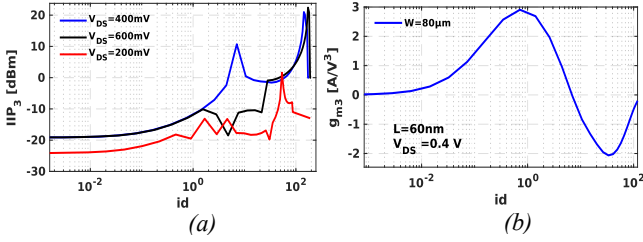


Fig. 4: a.  $IIP_3$  as function of  $i_d$  for different  $V_{DS}$ . b.  $g_{m3}$  as function of  $i_d$  for the case of circuit II

TABLE II. COMPONENT VALUES FOR THE THREE CIRCUITS WITH NOISE, GAIN AND CURRENT REQUIREMENTS

	Circuit I	Circuit II	Circuit III
$V_{DS}$ (mV)	200	400	600
$I_{Dmax}$ (mA)	0.8	0.9	0.8
$(G_{vmin}, F_{max})$	(10, 2)	(10, 2)	(10, 2)
$R_l$ ( $\Omega$ )	1000	660	500
$R_f$ ( $\Omega$ )	1825	2650	5360
$g_m$ (mS)	18.1	18.9	19.1
$R_p$ ( $\Omega$ )	147.2	248.5	555.5
$Q$	1.39	1.99	3.17
$L_g$ (nH) ( $Q_L=23, 2.4$ GHz)	4.6	6.6	5.8
$C_s$ (pF)	0.22	0.34	0.32
$G_t$	19.4	22.7	28.8
$B_w$ (GHz)	2.5	3.04	2.4
$g_m/I_D$ (1/V)	22.62	21	23.87
$W$ ( $\mu m$ )	110	80	110

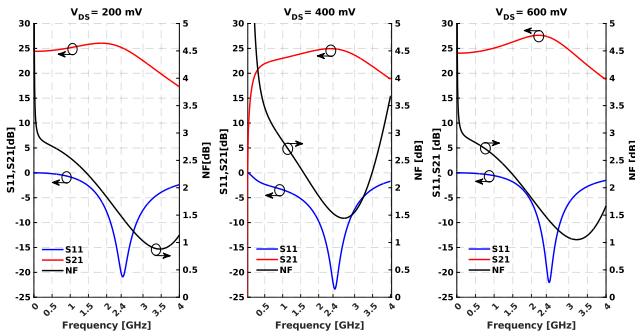


Fig. 5: UTISOI2 simulation results of  $S_{21}$ ,  $S_{11}$  and NF for  $V_{DS}=200$  mV, 400 mV and 600 mV over frequency with sizes from the design methodology.

For the three design cases, the sizing parameters and the analytical performance values are reported in Table II. The S parameters and total noise figure are shown in Fig 5. The  $IIP_3$  simulation results at 2.4 GHz are also shown in Fig 6.

Based on the design methodology and the 7-parameter model, our first analytical sizing using hand calculations show good agreement with simulation results using the UTISOI2 [10] model of the technology. A comparison

between analytical and simulated LNA performances are reported in TABLE III. As it is shown, the LNAs are well matched at the frequency of interest with good gain and bandwidth performance. The noise figure is optimized using the analytical constraints and the input matching network leading to good performances at the limited sub-1mW power budget. Also, the variation of the linearity performances through the drain voltage is captured. As it can be observed, low  $V_{DS}$  (0.2 V) results in poor linearity ( $IIP_3 = -21.2$  dBm), for  $V_{DS}$  close to the half range dynamic (0.4 V) the linearity is optimized and the  $IIP_3$  reaches -9.6 dBm. However, higher  $V_{DS}$  (0.6 V) and larger Q push the transistor to early saturation since  $IIP_3$  decreases to -12.7 dBm.

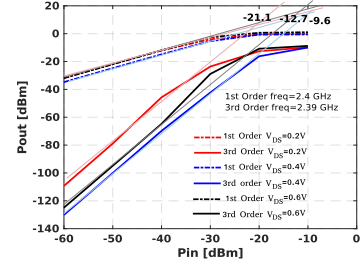


Fig. 6: UTISOI2 simulation results for  $V_{DS}=200$  mV, 400 mV and 600 mV at 2.4 GHz with sizes from the design methodology.

TABLE III. PERFORMANCE COMPARISON BETWEEN ANALYTICAL METHOD AND SIMULATION FOR THE THREE CIRCUITS

Performances	Circuit I	Circuit II	Circuit III
Analytical @ 2.4 GHz	$I_D = 0.8$ mA	$I_D = 0.9$ mA	$I_D = 0.8$ mA
	$G_t = 25.7$ dB	$G_t = 27.1$ dB	$G_t = 29.1$ dB
	$NF < 1.5$ dB	$NF < 1.5$ dB	$NF < 1.5$ dB
	$B_w = 2.54$ GHz $IIP_3 = -19$ dBm	$B_w = 3.04$ GHz $IIP_3 = -8.7$ dBm	$B_w = 2.4$ GHz $IIP_3 = -11$ dBm
Simulation @ 2.4 GHz	$I_D = 0.776$ mA	$I_D = 0.88$ mA	$I_D = 0.81$ mA
	$G_t = 24.9$ dB	$G_t = 25.6$ dB	$G_t = 28.4$ dB
	$NF = 1.42$ dB	$NF = 1.5$ dB	$NF = 1.39$ dB
	$B_w = 2.8$ GHz $IIP_3 = -21.1$ dBm	$B_w = 2.96$ GHz $IIP_3 = -9.6$ dBm	$B_w = 2.08$ GHz $IIP_3 = -12.7$ dBm

## V. CONCLUSION

This work presents a simple design method using a  $g_m/I_D$  and inversion level approach suited for low power LNAs in advanced technologies. It allows a fast and first-time right design of the LNA, based on a simple analytical study by using an accurate model of the MOS transistor valid in all regions of operation. The model is based on only 7 technological parameters that captures the main short-channel effects of the transistor. The proposed methodology directly links the transistor bias conditions and size to the main LNA performances, including for the first time the analytical modeling of the LNA nonlinearity. Three design examples in 28 nm FD-SOI technology based on the Rfeedback topology for different drain voltages are detailed. Thanks to the proposed methodology, the adequate inversion level of the transistor and the sizes of the passive components are determined systematically to fulfill gain, noise figure and linearity performances with a limited sub-1mW power budget. The analytical and simulated performances are compared showing the accuracy of the proposed methodology. This fast strategy based on simple hand calculations shortens the design time in comparison with CAD-based approaches that are generally used for such advanced technologies.

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