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Performance benchmark of State-of-the-art Sub-6-GHz wideband LNAs Based on an Extensive Survey

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Abstract— This work presents a survey based on more than 200 published papers related to sub-6 GHz wideband LNAs [1]. It investigates the trends with respect to the technology node. Moreover, it proposes a comparison between the most used topologies regarding their main performance metrics such as the gain, bandwidth, noise figure, power consumption and linearity. Based on this study, analytical predictions can be verified and appropriate architectures targeting a given set of specifications can be easily selected. The analysis highlights also the performance improvements and design trade-offs of design enhanced solutions such as noise cancelling and gm-boosting architectures.

Keywords—LNA, wideband, sub-6GHz, IoT, Common gate, enhanced topology

I. INTRODUCTION

Internet of Things (IoT) aims at connecting heterogeneous devices to offer explicit smart services. This drives an ever-increasing demand of communication technologies and various wireless standards, such as Bluetooth, Wi-Fi, GPS, and 2G/3G/4G/5G cellular [2]. These wireless standards operate mostly in bands up to 6-GHz. Multi-standard radio architectures, also classified as Software-defined radio (SDR) architectures, have been widely used and optimized in the past decades [3]. Moving forward with such architecture requires the design of wideband efficient receivers (RX). The receiver must meet complex set of requirements imposed by the different standards. This can be broken down into constraints on the Low Noise Amplifier (LNA) which is highly implied in the overall RX performances in receiver chain that does not use the mixer-first technique.

There are many options to design a broadband LNA given the wide variety of topologies and design techniques proposed in recent years and the development of advanced integrated technologies. The optimal design choice for a given set of target specifications should leverage the raw performance of the technology and the design complexity of the LNA topology. Generally, there are two ways in which a designer can evaluate *a priori* the potential performance of a given LNA architecture: using analytical formulas describing the amplifier behavior available in reference texts such as [4] and/or based on some Figures of Merits (FoM) to directly compare state-of-the-art designs published in the literature. The first approach allows the definition of some common topologies; however, no simple analytical derivations exist for all performances and all published LNA architectures. In addition, in most cases second order effects are neglected to

simplify the analysis which are important factors in improving some metrics. On the other hand, using FoMs could also be cumbersome. Given the existing correlations and trade-offs between the different LNA specifications, proposed FoMs may hide the strengths and weaknesses of the general topologies to highlight only the strengths of implementations. A similar problem was faced in the field of ADC [5] and PLL [6] design. In the case of ADC design community, a very powerful tool to explore the topologies and their achievable performance is proposed by Boris Murmann in [5]. Moreover, as this survey is regularly updated and has been maintained for years, design trends have emerged allowing to correlate technology development and conversion performance.

In this context, an interesting initiative has been recently proposed for the LNA design community in [7]-[8]. This first effort classifies LNAs by technology with the aim of proposing dedicated FoMs that may be useful for tracking the evolution of the LNA designs. This database collects the main performances of more than 500 published LNAs according to the used technology node and the center frequency. However, this previous work does not compare the different LNA topologies within a given technology or even the application range (with LNAs ranging from a few hundred MHz to the mm-Wave realm) which is a major interest for designers.

In this present work we employ the data in [8] to directly compare performances of the wideband LNA topologies published in the last twenty years. Towards this goal, we have revisited more than 200 sub-6-GHz wideband LNAs from IEEE publications such as ISSCC, JSSC, TMTT, RFIC, MWCL, TCAS and NEWCAS. Instead of using FoM based comparisons for which particular performances are not captured, the trade-offs, strengths, and weaknesses of each particular topology, in terms of gain, bandwidth, power consumption, linearity and noise, are evaluated based on a statistical analysis of the database. This analysis allows to put the theoretical performance predictions into perspective and to allow designers to gain insight when choosing the optimal design style for a given set of specifications. We have identified four common LNA topologies as represented in Fig. 1 namely common source with resistive feedback (CS RF), inductive degeneration CS, complementary CS RF and the common gate (CG).

These topologies are compared among themselves based on the average value of each performance considering the number of associated papers in the database. In this way, for the same target application and frequency range, the above topologies are compared according to the achieved

Gain, Noise figure (NF), Power consumption (P_{dc}), Input-referred third order Intercept Point (IIP3) and the relative bandwidth BW_r which is the bandwidth normalized to the center frequency (f_0) leading to $BW_r = BW/f_0$. Furthermore, some metrics are regrouped to highlight the LNA efficiency such as the normalized gain defined by the ratio of the linear gain by the power consumption, and the ratio of the gain, relative bandwidth product by the power consumption. In addition, a special attention is dedicated to some design techniques such as gm-boosting and noise canceling.

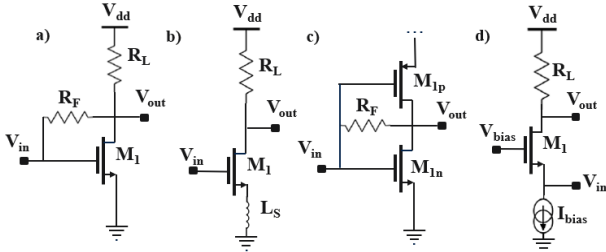


Fig. 1. a) Common source with resistive feedback, b) Common source with inductive source degeneration c) complementary common source with resistive feedback d) common gate.

The rest of this paper is organized as follows. In section II, the LNA performances are grouped according to the technology node to extract some trends. Section III shows the classification of the common topologies, creating a performance signature of each architecture. Section IV focuses particularly on the comparison of design enhanced solutions such as noise cancelling and gm-boosting. Section V classifies the noise reduction topologies and section VI concludes the paper.

II. LNA PERFORMANCE TECHNOLOGY TRENDS

First, to get a sense of the lay of the land, the collected wideband LNAs are classified according to the technological nodes to emphasize the appearance of trends for some performance parameters. Fig. 2 shows the distributions of the main parameters of the LNA, namely the gain, the power consumption, the input-referred third order intercept point and the noise figure using a box plot format.

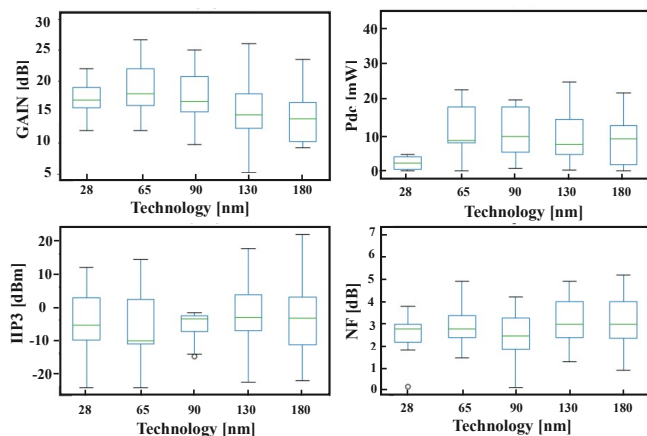


Fig. 2. Box plots of the gain (dB), power consumption (mW), IIP3 (dBm) and noise figure (dB) grouped by technology (nm) from 56 papers in 180 nm, 43 papers in 130 nm, 23 papers in 90 nm, 31 papers in 65 nm and 13 papers in 28 nm.

The technology, with the corresponding f_i and f_{max} , often sets the achievable bandwidth of the architecture [9]. Also, with some design techniques, one can take advantage of advanced nodes to improve some performances, for instance the power consumption and the maximal achieved gain as shown in Fig. 2. Moreover, there is a breakthrough in power consumption for LNAs designed in 28 nm. This could be explained by the particularly good power efficient performances of the FD-SOI technology which represents more than 60% of the 28 nm-based articles in our analysis. However, the relatively small number of publications in more recent nodes compared to older technologies could also push them aside from the trends. As previously reported in [7], there are low correlations between NF, IIP3 and the technology. Actually, the NF relies on the sensitivity requirements from the standards as well as the design techniques employed. The selectivity of the receiver chain towards blockers sets its linearity accordingly.

III. COMPARISON OF COMMON LNA TOPOLOGIES

As mentioned above, topology selection is one of the key decisions in the design of an LNA. In this section, we provide a comparison of the average reported performance of the most used wideband LNA. This comparison can be a very useful tool to guide the design of this circuits and reveal the design trade-offs associated with each architecture. Again, results are represented as web charts. Normalized efficiency charts and individual performance charts are considered for a better insight into the design trade-offs.

A. Efficiency charts

Fig. 3 compares the identified LNA topologies regarding their gain-power ratio, relative gain bandwidth product normalized by power consumption, NF and IIP3. Since gain, bandwidth and power consumption are correlated and depend on specific design methodologies, investigating the ratios seems to be relevant for a fair comparison between different architectures. This statistical analysis reveals that the complementary CS circuits yield the best tradeoff in terms of power efficiency, noise and linearity. It is expected that this topology presents the highest gain since this topology takes advantage of the current-reuse technique between both main transistors which finally leads to higher efficiency. Nevertheless, when comparing the topologies with respect to the gain-power ratio, Fig 3. demonstrates that the CG topology achieves the highest values. This is due to the reduced power consumption as it will be highlighted in the next section. It is also clear that CG architectures privilege a different trade-off than CS ones, offering the best gain-power ratio and gain-bandwidth product normalized to the power consumption, at the expense of worse linearity and noise than their CS counterparts.

B. Comparison of individual performances

Certainly, the FoMs such as the two relative ratios introduced in section A state a clear comparison among the architectures. However, this does not reflect a complete comprehensive comparison concerning all its parameters. Considering separately each performance metric provides additional insight to compare the topologies even though the

circuits are not designed under the same conditions and are implemented with different technologies.

Fig. 4 shows the comparison of the LNA's topologies according to the gain, power consumption, NF, IIP3 and BW_r . This direct comparison reveals that CG LNAs achieve, in average, the lowest power consumption but not the highest gain which is difficult to highlight through the gain-power ratio since the variation ranges are different. On the other hand, the complementary CS architecture, with its transistor pair, enhances inherently the equivalent transconductance of the LNA which allows better amplification as seen through the gain axis in Fig 4. Besides, compared to a basic CS RF topology, through the current reuse technique, it achieves low power consumption occupying the second position behind the CG.

The CG topologies are characterized by weak noise performances compared to other topologies. Actually, in this topology, the transconductance, which is a major contributor in the noise mechanism, can't be controlled separately from the matching condition. In most of the cases, as described in section IV, many techniques are associated to CG-based LNA to improve the noise figure such as the gm-boosting architectures. On the other hand, CS topologies, especially CS complementary structure exhibit a very good noise performances.

We focused our survey on wideband LNAs. As shown in Fig. 4 most of the topologies achieve large bandwidths in average. It is shown that the CG, RF CS and complementary CS allow wideband operation, however, the inductive degenerated CS architectures, which are better suited for narrowband applications, succeed to achieve wideband LNA. However, Fig. 4, shows their poor performances especially in terms of gain and bandwidth which is not expected with such topologies [4]. This can be explained in part by the fact that increasing the bandwidth requires lower quality factor at the input stage, which has negative consequences on the gain and noise figure and consequently on power consumption.

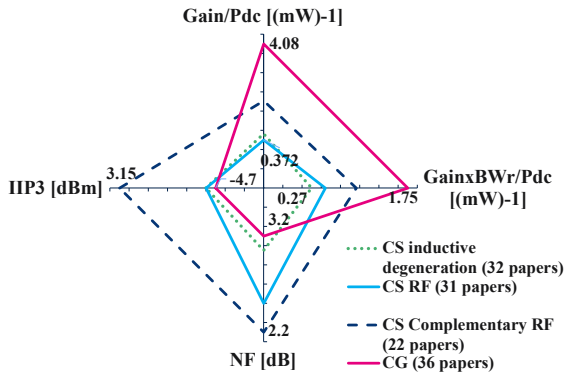


Fig. 3. Wideband LNA's topologies comparison from averaged results of previous published works.

The IIP3 is conventionally used to express the linearity of LNAs. The nonlinearity of MOSFET drain current comes from the nonlinear transconductance gm as well as the nonlinear drain conductance gds [4]. The complementary CS configuration has inherently good linearity performances [10]. In fact, with properly matched transistors by setting equal gm 's, the CMOS pair output current could be second

order distortion free. However, a general conclusion could not be driven out from the other topologies since many techniques are added to conventional architectures to boost the linearity performances. The trade-off between the linearity, gain and power consumption is analytically expected, although, not considered statistically

Considering all the performance metrics, the complementary CS topologies potentially present an appealing structure that satisfies the different tradeoffs by achieving, in average and according to the set of analyzed papers, the lowest NF, highest gain, IIP3 all together with acceptable relative bandwidth and relatively low power consumption.

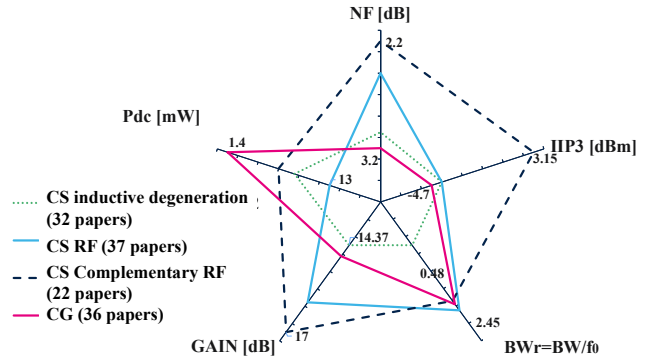


Fig. 4. Performance comparison of the different LNA topologies from the collected data

IV. DESIGN ENHANCED SOLUTIONS

For IoT applications, reduced power consumption is a major requirement to increase the battery lifetime of the solutions. The CG is attractive for its power and bandwidth characteristics; however, it suffers from inherent limitations in noise figure affecting the sensitivity of the receiver. Many efforts have been focusing on enhancing the CG topology to optimize the LNA performances [11] [12] [13]. In the literature, two main techniques are introduced: the common gate-common source (CGCS) topology known as noise canceling (NC), and the transconductance boosting gm-boost CG topology. The generic circuits of both architectures are shown in Fig. 5.

The CGCS principle consists in sensing the CG noise contribution and canceling it through an auxiliary out of phase forward path based on CS amplifier [11]. As shown in Fig. 5.b, the CG as input stage is used for wideband input matching and a balancing condition is applied on the CS branch to allow the noise canceling and operate as active single to differential structure. Recently, further modifications of the CGCS cell are proposed [12] [13] to improve the LNA performances.

The gm-boost CG principle consists in introducing a gain of $(-A)$ in the RF path between the source and the gate of the CG transistor to improve the v_{gs} swing and thus, improve the effective transconductance gm of the device by a factor of $(1+A)$. Hence, the choice gm is decorrelated from the input matching condition allowing performance enhancement of the classic CG circuit. The auxiliary gain cell can be passive or active. Passive topologies can be using the cross-coupled

capacitor technique for gain-enhancement of differential circuits [14], [15] or operation the boosting thanks to off-chip or integrated transformers [16]. Active-boost solutions take benefits from the CS amplifier [17] or introduce two feedback loops as in [18], or even insert a third positive feedback loop as in [19] and many other techniques reported in literature.

Despite of the performance enhancement of classic CG topology, both techniques have a variety of proposed architectures and sometimes are difficult or complex to be described with analytical derivations. In such cases, the state of the art can be helpful to work out some trends for a given configuration. In Fig. 6, CGCS and gm-boost topologies are compared among themselves and with respect to CG based circuits considering the LNA main performances: NF, gain, IIP3, power consumption and bandwidth.

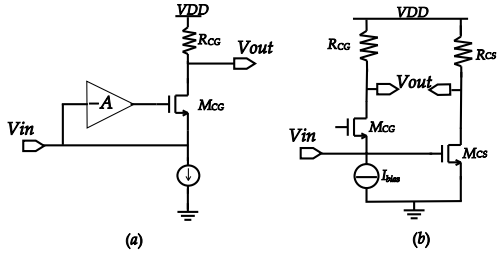


Fig. 5. Generic circuits for a) gm-boost CG LNA and b) CGCS LNA.

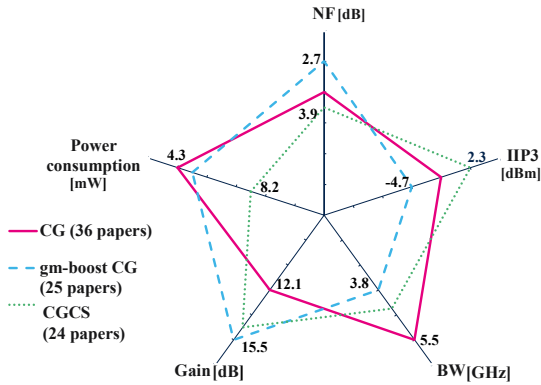


Fig. 6. Performance comparison of the CG, CGCS and gm-boost CG LNA topologies from the collected data

As expected, both the CG enhanced topologies increase the gain of the basic CG with small power penalty for the gm-boost technic. Although the CGCS topology is usually introduced as a noise cancelling architecture [11], it does not achieve the best noise performance among other CG LNA types. This is explained by the fact that the additional CS transistor in the noise cancelling structure, eliminates the noise contribution of the CG transistor but, in a practical implementation, it is difficult to reduce its contributions sufficiently to challenge the gm-boost CG topologies especially passive based without extra-noise penalty. On the other hand, the noise cancelling architectures CGCS performs a good linearity enhancement of the CG circuit. In fact, the design conditions leading to the absorption of the thermal noise of the main CG transistor are valid for distortion reduction [11]. However, the gm-boost architectures IIP3 performances are affected by the large voltage swing of the CG transistor.

V. NOISE REDUCTION ARCHITECTURES

One of the main characteristics for receivers benchmarking is their sensitivities, that relies on the noise performances. Since the LNA is the dominant building block among the noise contributors in the receiver chain, reducing its NF has been an attractive topic for RF designers. In Fig. 7, a comparison of 60 state of the art ultra-wide band noise reduction LNAs in terms of power consumption and NF is shown. As it can be observed, most of the published works are based on the CGCS topology (>35%), represented by green squares. However, these topologies are not dominating the extremely low noise solutions. As an example, sub-2dB NF, which is challenging for wideband, is achieved by different topologies such as the CS enhanced by transformers, the gm-boost CG and other complex noise-oriented propositions using fancy circuits. This distribution as presented, breaks with the general idea assuming that decreasing the noise figure has a big power consumption penalty. It is shown that, for a NF value, the power consumption depends on the topology, the used technique, and also intrinsic technology-related properties. Besides, it is shown another time that CG-based topologies are adequate for limited power budget requirements.

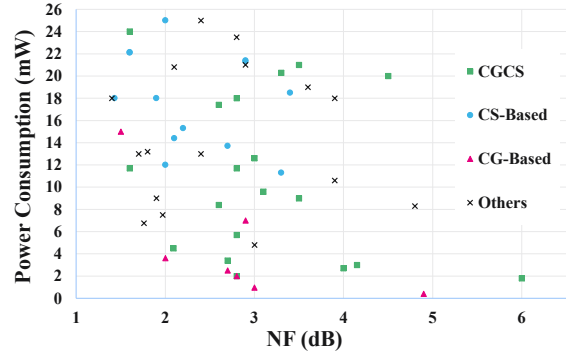


Fig. 7. State of the art of Sub-6-GHz wideband noise-reduction LNAs sorted by power consumption-noise figure trade-off.

VI. CONCLUSION

In this article, more than 200 sub-6-GHz wideband LNAs published in the literature are reviewed and compared in terms of their performance metrics. We explore the trends related to the technology advance. Direct performance comparisons between the most common LNA topologies are provided. These comparisons, based on simple efficiency figures as well as on individual performances, clearly show the strengths, weaknesses, and trade-offs of each LNA topology and highlight design trends that could not be intuitively anticipated otherwise in the context of wideband LNA especially through the analysis based on compact FoMs. The CS complementary RF topology is highlighted as a very interesting architecture, achieving a good tradeoff between all performance metrics for wideband LNAs when compared to other conventional architectures. Finally, design enhancement solutions are explored for different topologies to show the performance boosting thanks to advanced techniques that are hard to be described and compared by simple analytical systems. The presented approach could be exploited to propose an extended survey on LNA topologies operating at different frequency ranges.

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