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High Quality Single Crystal Recrystallization of Thin 4H-SiC Films Deposited by PVD Techniques, a Way for New Emerging Fields

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Abstract. SiC sputtered and e-beam evaporated layers have been deposited on 4H-SiC substrates. High temperature annealing with two plateaus at 1400°C and 1700°C is performed to recrystallize the layers. The crystallinity was investigated by Raman spectroscopy with laser lines of 785, 405 and 325nm. To determine the electrical conductivity of the layers, electrical measurements are made. Only the electron beam evaporated layers presents a recrystallization close to homoepitaxial quality but, contrary to sputtered layers, they don't have an electrical conductivity.

Introduction

Silicon carbide is a compound semiconductor material well known in power electronics applications with already commercialized SiC devices such as Schottky diodes and transistors (BJT, JFET, MOSFET). Its remarkable physical and chemical properties compared to other semiconductors make it also as an ideal material for devices under high temperature and pressure. SiC is also more and more studied for applications in photonics and quantic with emissions from the UV to the IR [1]. However, bulk and homo-epitaxial growth of SiC crystals is quite expensive and time consuming. 150-mm-diameter wafers are currently produced by seeded sublimation method at ~2300 °C, on which homo-epitaxial growth of SiC is performed typically at 1500-1650°C by chemical vapor deposition [2]. The layers obtained with these sophisticate and specific techniques are difficult to be directly localized at the substrate surface and thus device fabrication with limited architectures needs post-growth plasma etching.

Fabrication of SiC devices requires also engineering and recovery of defects. The controlled introduction of defects in SiC have a high impact on the operational performances devices and can determine its properties such as its conductivity or photoluminescence. Most common utilized methods of defects engineering in SiC are ionic implantation and doping steps. However, amorphisation of the surface of SiC is possible due to high defect densities implanted at room temperature (RT). High temperature annealing is then needed to recrystallize these layers. Characterization techniques which can determine the crystallinity and the defect proportion of SiC are thus required, such as Raman spectroscopy.

In this paper, high quality 4H-SiC layers obtained by more classic physical vapor deposition (PVD) techniques are presented, opening a way to design new SiC devices exploiting these PVD thin films for power applications and also other emerging fields, such as bio sensors, high temperature sensors, and optoelectronics or quantum nanophotonics. Raman spectroscopy is used to determine the polytype and level of recrystallization of the SiC layers.

Experimental Part

Commercialized n-type 4H-SiC samples have been utilized for this study, substrates with and without n-type epitaxial layers on the Si face. Both physical vapor deposition (PVD) techniques, sputtering amorphous SiC target and electron-beam (EB) evaporation, were used to deposit the amorphous SiC layers on the surface of the samples. Sputtering was realized with MP400 Plassys equipment whereas an Elettrorava machine was used for electron-beam evaporation. Table 1 shows information about the SiC samples and their amorphous layer. The surfaces of the samples f and g were cleaned by in-situ etching before deposition.

Table 1: Conditions of deposit of the amorphous SiC layer

	a	b	c	d	e	f	g
Substrate orientation	on-axis	on-axis	4° off-axis	7.88° off-axis	4° off-axis	4° off-axis	4° off-axis
Structure of the substrate	n ⁺⁺ /n ⁺ /n	n ⁺⁺ /n ⁺ /n	n ⁺⁺ /n ⁺ /n	n ⁺⁺ /n ⁺ /n/p ⁺	n ⁺⁺ /n ⁺ /n	n ⁺⁺	n ⁺⁺
PVD technique	N.A	Sputt.	Sputt.	Sputt.	Sputt.	Sputt.	EB evap.
Thickness [nm]	N.A	400	400	500	200	1500	150
Temperature [°C]	N.A	400	400	700	RT	RT	750

In order to (re)crystallize the thin amorphous layers (0.15 at 1.5 μm) samples have been cut in pieces of 25×25 mm and annealing steps under Ar have been performed in a dedicated 150-mm AET RTP graphite resistive furnace with two plateaus at 1400°C and 1700°C of 30 minutes each (Fig. 1). For the samples to be annealed at these high temperatures without damage, AZ9260 photoresist is deposited and spin-coated on both sides of the samples beforehand. The encapsulation of the samples is then pyrolyzed at 750°C under Ar in a second chamber (in quartz) of the AET furnace. The obtained graphite cap is removed by oxygen plasma reactive ion etching (RIE) after RTP annealing. The samples are then cleaned with Piranha and diluted hydrofluoric solutions.

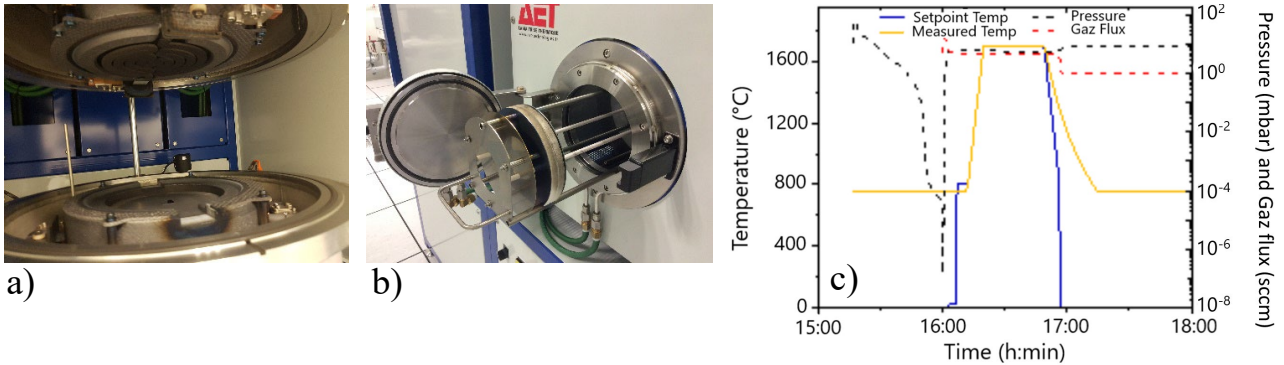


Fig. 1. 150 mm AET furnace for this study: RTP chamber with graphite resistors (a), pyrolyzed quartz chamber (b) and typical temperature and Ar pressure profiles for the RTP 1700°C 30 min plateau (c).

Before and after the RTP annealing the samples have been analyzed by Scanning Electronic Microscopy (SEM) with the FEG SU8030 Hitachi machine and by μRaman Spectroscopy in back-scattering geometry excited at RT with the LabRAM HR Evolution equipment from Jobin Yvon Technology. SEM has been realized at normal incidence and with a tilt of 30°. For Raman spectroscopy, several laser lines from UV to IR were used with wavelengths of excitation (λ_{ex}) of 325, 405 and 785nm. However, the penetration depth in SiC during Raman measurements depends strongly on the wavelength of the laser. Indeed, UV light penetrates less deep in SiC than visible and IR light [3, 4]. To analyze only the deposited amorphous SiC layer and to limit the influence of the substrate on the Raman spectra, the 325nm UV line is favored in this study. With this wavelength, a 40× long-focus objective lens was used and the time of excitation of the samples was 30s. The power

of the 325nm laser was 25mW. For all μ Raman measurements, a 100 μ m confocal pinhole and a grating of 300g/mm were used.

To confirm the thickness of the SiC PVD layers, surface profiles were measured with a DektakXT® Bruker stylus profilometer. Finally, current-voltage (I-V) measurements have been performed with a two-point probe-station in order to test the electrical conductivity of the layers after annealing at 1700°C. The measurement of the sheet resistance of sputtered PVD layers deposited at RT and 400°C are also performed before annealing. To determine the sheet resistance of the PVD layers, circular transfer length method (TLM) structures [5] were fabricated, with a metallic Ni layer which has been deposited by lift-off, on the surface of the samples. SiC uncovered rings of different lengths are thus realized (Fig.2) and the measurement of their resistances allows us to determine the sheet resistance of the SiC sputtered layers.

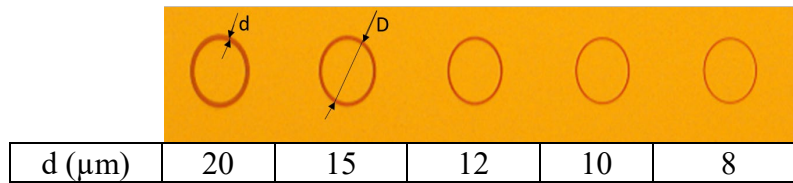


Fig. 2. SiC sample with a sputtered SiC layer deposited at RT for 20min (darker color), partially covered with CTLM metallic structures (lighter color) observed under x50 microscope. D is constant, 100 μ m, and d , the length of the uncovered SiC rings varies from 8 to 20 μ m.

Results and Discussion

The thickness of the SiC layers formed by PVD and measured with the stylus profilometer, is directly correlated to the time of deposition. SiC layers around 200nm, 400nm and 500nm thick are obtained for deposition time of 20min, 40min and 49min respectively for samples b to e of the Table 1.

Raman spectrum of 4H-SiC is characterized by the intense TO and LO peaks [6] situated at 776 and 964 cm^{-1} respectively (Fig. 3.a). These peaks are obtained on our 4H-SiC substrate before the deposition of the SiC layers by PVD. Several second-order Raman bands are also present in the region between 1400 and 1800 cm^{-1} [7] as shown in the Raman spectrum of the 4H-SiC substrate in the Figure 3.b.

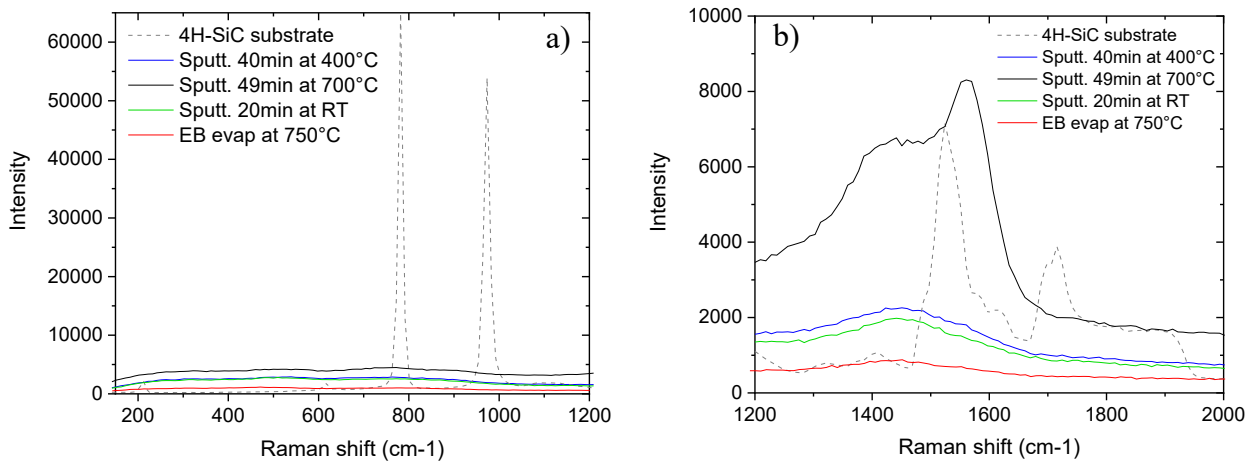


Fig. 3. Raman spectra of the amorphous SiC layers before annealing compared to the 4H-SiC substrate, with UV 325nm excitation, from 150 to 1200 cm^{-1} (a) and from 1200 to 2000 cm^{-1} (b).

Before annealing, the Raman spectra of the sputtered and evaporated SiC layers lack the LO and TO peaks as well as the second-order Raman bands. However, a large band appears around 1450 cm^{-1} which can be associated to the sp^2 - sp^3 vibration between two carbon atoms [8]. For the

sputtered layer at 700°C, two bands at 1430cm⁻¹ and 1560cm⁻¹ replace the one at 1450cm⁻¹. In the literature, the D and G bands of amorphous carbon with sp² bonds are generally situated around 1350 and 1580cm⁻¹ respectively [9]. The G band corresponds to the stretching vibrations in the basal plane of ideal graphite whereas the D band is attributed to a defect or disorder in the hexagonal planar graphite structure [10]. Thus, the bands present at 1430cm⁻¹ and 1560cm⁻¹ can be attributed to the D and G bands of sp² carbon atoms. Therefore, when an amorphous SiC layer is deposited at higher temperature (700°C), bonds between sp² carbon atoms seems to be present.

Once the amorphous SiC layers are annealed at high temperature, 1400°C and 1700°C, their Raman spectra, show LO and TO peaks characteristic of 4H-SiC but they don't reach the intensity obtained on the 4H-SiC substrate (Fig. 4). The deposits follow the crystallinity of the substrate. This fact denotes a solid phase epitaxy from the PVD layer/substrate interface. It is also visible that the thicker layers present less intense LO and TO peaks, especially for the layer deposited at 700°C (around 500nm thick) which present these peaks only after annealing at 1700°C and with very low intensity (Fig. 4.b). In the case of the sputtered layers, the band found at 1430cm⁻¹ before annealing is divided into two bands at 1415 and 1585cm⁻¹ after annealing at 1400°C and 1700°C. The position of these bands shifts when the wavelength of excitation is changed. The peak originally at 1415cm⁻¹ shifts at 1375cm⁻¹ under 405nm excitation and at 1305cm⁻¹ under 785nm excitation whereas the peak at 1585cm⁻¹ shifts at 1605cm⁻¹ under 785nm excitation (Fig. 5). These peaks can then be attributed to the D and G peaks of sp² carbon atoms. Thus, bonds between sp² atoms appear after annealing at high temperature. When the temperature of annealing increases, the intensity of the LO and TO peaks also increases as well as the one of the G band whereas the intensity of the D band remains quite stable. Therefore, considering the Raman spectra obtained, it is concluded that the PVD SiC layers are not totally recrystallized even after annealing at 1700°C.

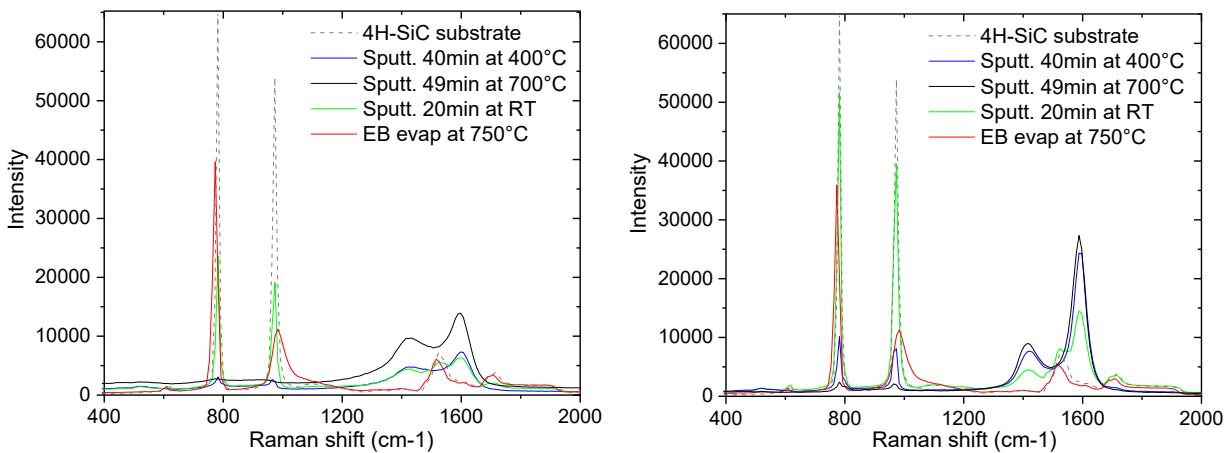


Fig. 4. Raman spectra of the SiC layers compared to the 4H-SiC substrate with UV 325nm excitation after annealing at 1400°C (a) and 1700°C (b).

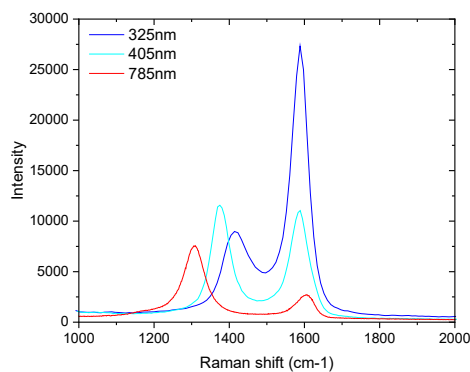


Fig. 5. Raman spectra at different excitation wavelengths of a sputtered SiC layer at 700°C after annealing at 1700°C.

On the contrary, the Raman spectrum of the EB evaporated SiC layers doesn't have bands associated to the presence of C-C bonds anymore and the intensity of their LO and TO peaks is quite intense and doesn't change between the annealing at 1400 and 1700°C. Therefore, the EB evaporation technique seems more efficient than sputtering to obtain layers of recrystallized SiC. If sputtering is used instead, the layers still have sp^2 - sp^2 C-C bonds and the intensity of the TO and LO peaks tends to decrease when the temperature of sputtering increases. Nevertheless, by EB evaporation, the thickness of the PVD SiC layers obtained with our equipment is limited to few hundred of nm while by sputtering much greater thicknesses can be reached.

SEM images presented in Figure 6 correspond to the surface of the PVD SiC layers obtained after 1700°C second annealing (C-cap retired). Compared to the surface of the 4H-SiC substrate, the evaporated layer deposited at 750°C and annealed at 1700°C presents a homogenous surface with a slightly undulating grainy morphology typical of those obtained on recrystallized SiC amorphous layers created by high doses RT ion implantation [11]. In the case of the sputtered layers annealed at 1700°C, the surface is slightly porous and less smooth than the evaporated layer.

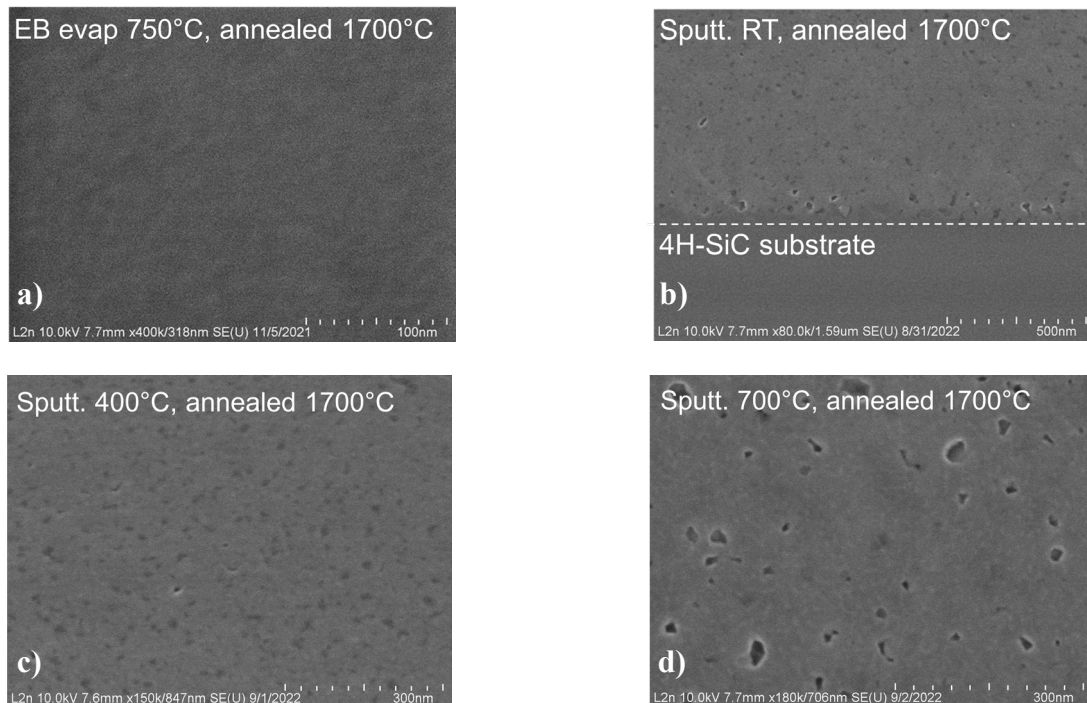


Fig. 6. SEM images from the PVD layers after recrystallisation (C-cap removed by O_2 plasma): SiC e-beam deposited at 750°C and annealed up to 1700°C/30min (a) and SiC sputtered layers deposited at RT (b), 400°C (c) and 700°C (d) and annealed up to 1700°C/30min.

To determine the sheet resistance of the sputtered PVD SiC layers before annealing, current-voltage measurements are performed (Fig.7) on the layers with circular TLM metallic structures on surface as shown in the Figure 2. The linearity of the curves obtained shows their conductivity, even before post deposition high temperature annealing. The sputtered layer deposited at RT presents I-V curves more linear than the one deposited at 400°C and, for a same bias applied, the intensity of the current measured is also a bit higher for the deposit at RT compared to the one deposited at 400°C. Therefore, the PVD layer deposited at RT seems a bit more conductive than the one deposited at 400°C. Nevertheless, the current measured is also very low (around 1×10^{-5} A) under the applied bias (from -3V to 3V) suggesting a strong resistivity of both layers. The slope of these curves gives us the resistance of sputtered layers measured between the circular TLM structures.

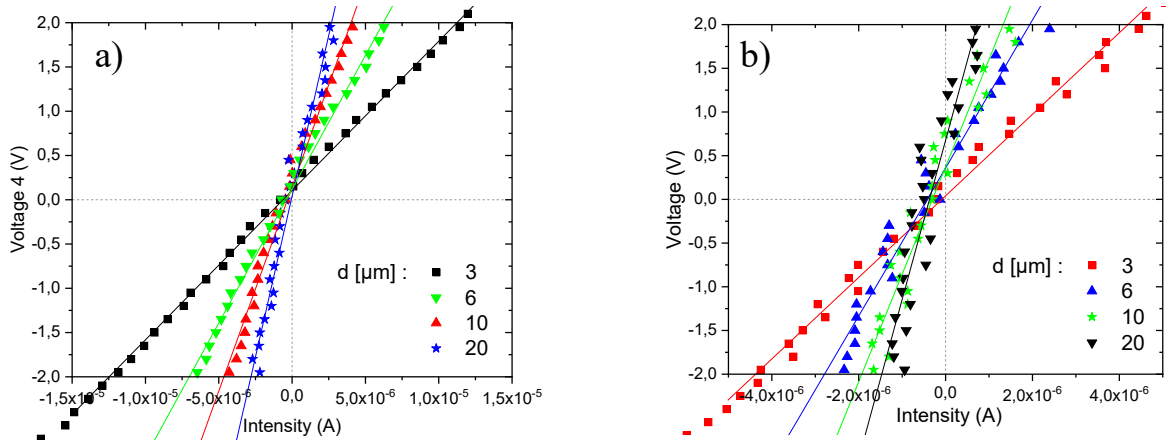


Fig. 7. I-V measurements of SiC sputtered PVD layers deposited at RT (a) and 400°C (b).

The obtained resistance of the sputtered layers can be expressed by the formula [5]:

$$R = \frac{R_{sh}}{\pi D} (d + 2 L_T) C \quad \text{with the correction factor } C = \frac{D}{2d} \ln \left(1 + \frac{2d}{D} \right), \quad C \sim 1 \text{ for } d \ll D.$$

R_{sh} is the sheet resistance of the layers, D the diameter of the rings, d the length of the uncovered SiC rings and L_T the length transfer (Fig.2). The correction factor allows the correct determination of the contact resistance. However, this factor is not calculated here because on one hand, $d \ll D$ so the factor is negligible and on the other hand, we are only interested in measuring the sheet resistance, not the contact resistance.

As D is fixed and d varies, the sheet resistance of the sputtered layers, R_{sh} , can be determined by the slope of the curve representing the measured resistance of the sputtered layers in function of d (Fig.8). High sheet resistance values are thus calculated, $R_{sh} > 1 \text{ M}\Omega/\text{square}$ (Table 1), for both sputtered layers deposited at RT for 20min and at 400°C for 40min. Therefore, the sputtered PVD layers are conductive before annealing but present a very high resistance.

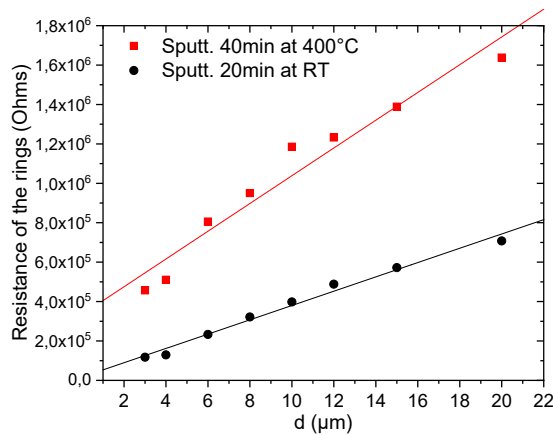


Fig. 8. Measured resistances on the circular TLM structures in function of their widths for PVD layers deposited at RT and 400°C.

Table 2: Determination of the sheet resistance by circular TLM structures on sputtered PVD layers deposited 20min at RT and 40min at 400°C.

Sputtered PVD layers	20min at RT	40min at 400°C
Slope of the curve [$\Omega/\mu\text{m}$]	36308	70433
Interception with the y-axis - $2 \times R_c$ [$\text{k}\Omega$]	16.939	334.260
Fitting parameter (COD)	0.986	0.951
Sheet resistance [$\text{M}\Omega/\text{square}$]	11.41	22.13

After high temperature annealing, even if the sputtered SiC layers are not entirely recrystallized, they have a higher n-type conductivity. Figure 9 shows electrical measurements, both in lateral and vertical configuration, for the sample f (Table 1). On this sample the SiC sputtered layer is $1.5\ \mu\text{m}$ thick. Circular TLM structures have not been fabricated as the SiC sputtered layer is not insulated from the 4H-SiC substrate with junctions or low doped epitaxial layers. The tungsten tips are put directly on the SiC surface without metallic electrodes. The linearity of the I-V curves gives evidence of the high doping of the layers obtained.

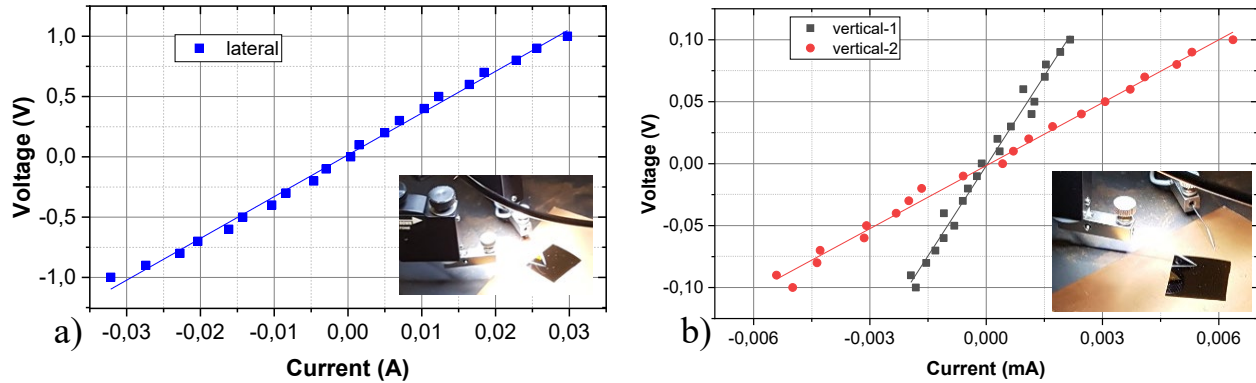


Fig. 9. I-V measurements performed on the SiC RT sputtered layers and crystallized up to $1700^{\circ}\text{C}/30\text{min}$ annealing: in lateral configuration with both tips on the sample surface (a) and in vertical configuration (b). Optical images from measurement set-up are inserted.

Linear current-voltage measurements have not obtained on the evaporated SiC (sample g in Table 1). The same recrystallization annealing with the two high temperatures plateaus have been performed as for the samples with sputtered SiC layers. Compared to the recrystallized sputtered SiC layers, the evaporated layer does not present this electrical conductivity which is explained by the higher vacuum level with lower impurity incorporation during this process. Annealing at 1700°C during 30min are typical conditions to activate doping in SiC single-crystal [11]. The presence of nitrogen contamination in the sputtered PVD equipment could explain the high conductivity obtained for the sputtered SiC layer, especially for the sample f after high temperature annealing.

Conclusion

The SiC amorphous layers deposited by sputtering and electron beam evaporation are partially recrystallized after annealing at 1400 and 1700°C . EB evaporation allows a better recrystallization for thin layers but the layers obtained have low conductivity compared to the layers deposited by sputtering due to the high vacuum level of the process. Thus, PVD of SiC allows us to form homo-epitaxial layers on a 4H-SiC substrate at lower cost compared to the methods currently used. However, the quality of the sputtered layers still needs improvements. Defects or impurities can also be introduced into the EB evaporated layers to increase their conductivity.

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