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A (0.75–1.13) mW and (2.4–5.2) ps RMS Jitter Integer-N-Based Dual-Loop PLL for Indoor and Outdoor Positioning in 28-nm FD-SOI CMOS Technology

Mateus B. Moreira, Francois Rivet, Magali de Matos, Hervé Lapuyade, and Yann Deval

Abstract—This brief presents the design of a dual-loop PLL for indoor and outdoor positioning. The proposed architecture is a dual-mode frequency synthesizer. It allows addressing either GNSS or WiFi. Thus, WiFi can assist GNSS for indoor positioning, while GNSS takes care of outdoor positioning. It achieves a high bandwidth with fine resolution without using the fractional-N approach. The PLL operates for the WiFi mode with 57 channels from 5.16 GHz to 5.72 GHz with a 10 MHz channel spacing and for the GNSS mode at frequency bands of GPS, Galileo, GLONASS, Beidou, and IRNSS. The Phase Noise of the designed PLL at 1 MHz offset from the carrier is -97.37 dBc/Hz and -104.58 dBc/Hz for WiFi and GNSS, respectively, and the power consumption is 1.127 mW and 0.749 mW. The total active area is 0.346mm^2 . This architecture is the first of its kind for both indoor positioning and outdoor positioning.

Index Terms—Dual-loop phase-locked loop (PLL), LC-VCO, ring oscillator, frequency synthesizer.

I. INTRODUCTION

THE BILLIONS of portable devices that incorporate connectivity to the WiFi network and a satellite navigation system have encouraged the investigation of circuits that could offer indoor and outdoor positioning using WiFi and GNSS standards. The Global Navigation Satellite System (GNSS) standard which includes GPS, Galileo, GLONASS, Beidou, and IRNSS, presents good outdoor positioning coverage. However, WiFi assistance might be essential for indoor positioning, as GNSS signals collapse in many buildings. Consequently, dual-mode systems with WiFi and GNSS capabilities are expected to achieve full and accurate coverage of positioning [1], [2], [3].

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In addition to the requirements regarding WiFi and GNSS standards, the concern is to reduce the power consumption of the transceiver during its operation to avoid recharging or replacing the device battery. When it comes to receivers, one of the most power-consuming circuits is the Phase-Locked Loop (PLL). Indeed, Phase Noise (PN) is inversely proportional to power consumption. Reducing the power of the transceiver without deteriorating noise is a technological bottleneck [4]. The challenge of generating a carrier frequency for a transceiver with good PN prompts the study of new PLL topologies to perform a good selectivity in the receiver. The need to increase bandwidth to reduce system PN is a well-identified solution [5]. The fundamental issue linked to this approach is to obtain a wide bandwidth and, at the same time, a fine frequency resolution. Due to the required value of the frequency division, the integer-N topology cannot achieve fine frequency resolution with a large bandwidth. This brief proposes a unified and optimized frequency synthesis for both indoor and outdoor positioning and provides an alternative to fractional-N PLLs with a dual-loop topology. The topology consists of two mixed integer-N loops as proposed in [6]. It achieves low power, wide bandwidth, and fine frequency resolution with the requirements of jitter imposed by both standards. The proposed PLL is designed and fabricated in 28nm CMOS FD-SOI technology from STMicroelectronics.

This brief is organized as follows: Section II presents the proposed architecture, and Section III describes its operational modes. The results of the measurements and the comparison with the state-of-the-art are presented in Section IV. Finally, Section V concludes this brief.

II. PROPOSED PLL ARCHITECTURE

This integer N-based dual-loop PLL is proposed to avoid the drawbacks of fine frequency resolution obtained with the complexity of the fractional divider [7], [8], [9]. The architecture introduced in Fig. 1 is composed of two loops, with the secondary loop combined with the primary loop using a mixer. In this configuration, the relationship between the output frequency and the reference frequency can be derived by

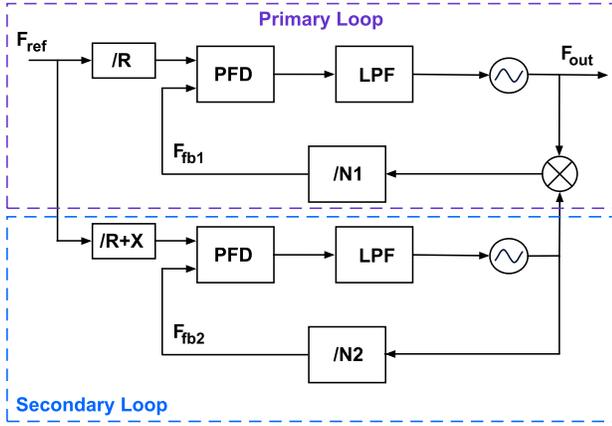


Fig. 1. Proposed dual-loop PLL architecture.

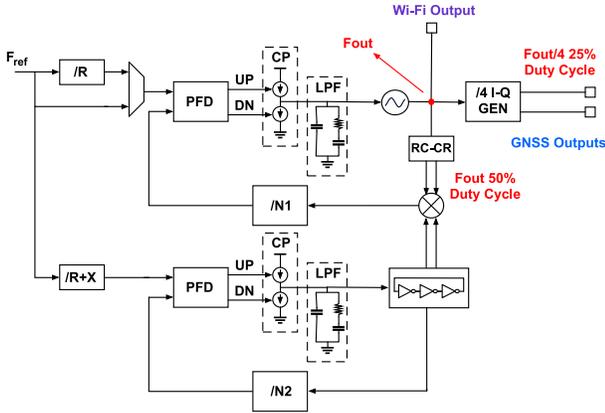


Fig. 2. Detailed dual-loop PLL architecture.

Eq. (1) with $N_1 + N_2$ kept constant.

$$f_{out} = \frac{f_{ref}}{R+X}(N_1 + N_2) + \frac{f_{ref} \cdot X}{(R+X) \cdot R} N_1 \quad (1)$$

N_2 is a slave of N_1 : an increase (or decrease) of 1 in N_1 is followed by a decrease (or increase) of 1 in N_2 . The first term of the Eq. (1) is a constant and the frequency resolution is given by $\frac{f_{ref} \cdot X}{(R+X) \cdot R}$. Therefore, this proposed PLL architecture achieves a fine frequency resolution even using a relatively large reference frequency, paving the way for a large PLL bandwidth.

III. CIRCUIT IMPLEMENTATION

A. GNSS Mode

Figure 2 shows the complete architecture of the proposed PLL. While the PLL is in GNSS mode, only the primary loop is used by disabling the VCO (the Ring Oscillator (RO)) of the secondary loop. The mixer outputs a signal with the same frequency as the primary loop input. The primary loop oscillator is an LC oscillator to achieve better performance in terms of PN compared to RO. The multiplexer at the input selects the reference frequency to go directly to the PFD of the primary

loop without passing through the divider. An N-path down-converter is used in the receiver, so the output signals must be in quadrature with a duty cycle of 25%. One way to reach this goal is to use a signal operating at four times the required frequency and combine its divisions. The signal frequencies at the output of the VCO of the primary loop are 4705.8 MHz, 4828.56 MHz, 4910.4 MHz, 5115 MHz, and 6301.68 MHz. The largest common divider of 40.92 MHz is used as the reference frequency to obtain the GNSS frequency bands L1, L2, L3, L5 and E6 from the same reference, reached by switching N_1 between 115, 118, 120, 125 and 154 [10]. Oscillator specifications for the GNSS mode require an in-band average PN lower than -70 dBc/Hz [2].

B. 5 GHz-WiFi Mode

The two loops are used in WiFi mode to reach the 57 WiFi channels from 5.16 GHz to 5.72 GHz with a channel spacing of 10 MHz. In this configuration, the multiplexer selects the divided signal to address the PFD. The mixer, which ideally outputs a signal at frequency $f_1 - f_2$ (input frequencies), requires a signal with only an approximate quadrature and 50% duty cycle. In addition, the implemented mixer architecture is based on an all-digital architecture that does not require the usual filters to produce the wanted frequency. An additional quadrature signals generator (RC-CR polyphase filter) is used for the primary loop.

A common 400 MHz reference signal is used for the two loops, and this reference frequency is divided down to 50 MHz (division by 8) for the primary loop and 40 MHz (division by 10) for the secondary loop. Considering a bandwidth of 200 kHz with a receiver sensitivity of -72 dBm and an SNR of 15 dB, the oscillator specifications for the WiFi mode require an in-band average PN lower than -70 dBc/Hz [11], [12], [13], similar to the GNSS mode specifications.

C. Primary Loop Oscillator

The noise from the secondary loop VCO is high-pass filtered by the secondary loop filter and low-pass filtered by the primary loop. However, the VCO of the primary loop is only high-pass filtered up to the bandwidth of the primary loop, resulting in a high-frequency noise dominated by the VCO noise of the primary loop. Consequently, the VCO in the first loop is an LC-VCO due to its better free-running PN performance compared to RO.

The topology of the LC-VCO is a complementary cross-coupled topology as shown in Fig. 3. A switched capacitor bank was used for coarse tuning to control the frequency by means of a 7-bit tuning word from an SPI block. The minimum resolution achieved with the least significant bit is 8 MHz. The fine-tuning control comes from the loop and is performed by a differential PMOS varactor. The LC-VCO covers a frequency range of 4.7 GHz to 6.3 GHz to ensure the two operating modes of the PLL, GNSS and WiFi.

The design methodology for sizing the transistors is based on the UICM model [14] described by [15]. The minimum supply voltage to start the oscillator can be described by

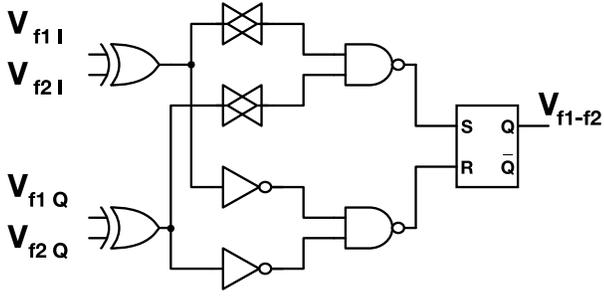


Fig. 3. Primary Loop LC-VCO architecture.

TABLE I
ELECTRICAL PARAMETERS OF THE LC-VCO

Parameter	Value
(w/l) NMOS cross-coupled pair	2.63 $\mu\text{m}/60\text{ nm}$
(w/l) PMOS cross-coupled pair	16.30 $\mu\text{m}/60\text{ nm}$
(w/l) PMOS Current Mirror	32.6 $\mu\text{m}/60\text{ nm}$
(w/l) Varactor (half)	200 $\mu\text{m}/30\text{ nm}$
L	1.8 nH
Q	12.15 @ 4.7 GHz
n	2
Outer diameter	311 μm
Inner diameter	245 μm
Inductor width	11 μm
Varactor _{Cmin} \rightarrow Varactor _{Cmax}	55.7 fF \rightarrow 62.3 fF
Binary _{Cmin} \rightarrow Binary _{Cmax}	5 fF \rightarrow 320 fF

Eq. (2).

$$VDD_{min} = \phi_t \left[\sqrt{1 + i_f} - 2 + \ln(\sqrt{1 + i_f} - 1) \right] + \frac{V_{TON} - V_{TOP}}{n} + V_{dstail}, \quad (2)$$

where V_{TON} and V_{TOP} are the threshold voltages of the NMOS and PMOS transistors. i_f , n and ϕ_t are the inversion level, the slope factor, and the thermal voltage. Finally, V_{dstail} is the saturation voltage of the tail transistor. As one can notice, the minimum supply voltage is strongly dependent on the threshold voltage of the transistor and, therefore, on the technology. Furthermore, it can be observed that the minimum supply voltage also depends on the inversion level. Thus, the inversion level was set to 25 (i.e., moderate inversion) to obtain a good PN, and a wide frequency range, and to minimize the impact of the process variations. Table I summarizes the electrical parameters of the LC-VCO.

D. Secondary Loop Oscillator

The VCO topology of the secondary loop is an inverter chain RO composed of 13 inverters depicted in Fig. 4. It was chosen instead of an LC topology because of the relaxed noise requirements of the secondary loop VCO. In the same way as the LC VCO, the RO must have in-phase and quadrature outputs. A RO can provide near-quadrature signals, which can drive the digital mixer. The in-phase output is taken from the output of the first inverter and the quadrature output is taken from the output of the sixth inverter. The RO covers the band from 800 MHz to 960 MHz to achieve the required tuning frequency range. For this purpose, coarse tuning was performed by the main supply line control. Furthermore,

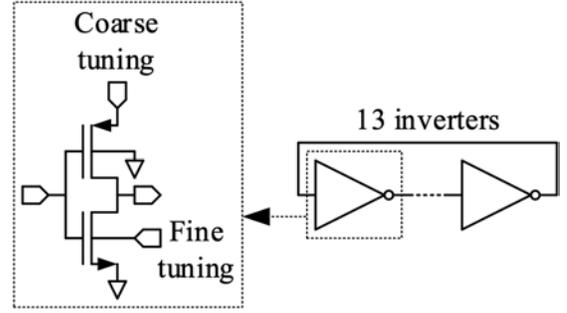


Fig. 4. Proposed architecture for the Ring Oscillator.

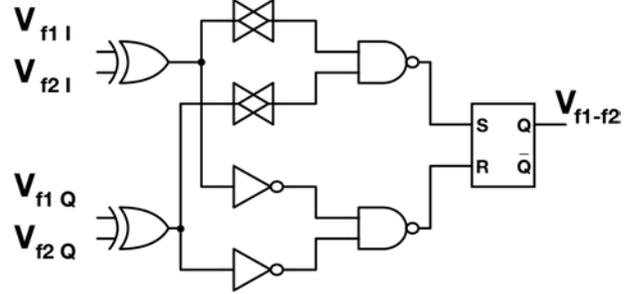


Fig. 5. Mixer Topology.

fine-tuning was performed by the body bias of the NMOS transistors of each inverter [16], as shown in Fig. 4.

E. Mixer

A mixer computes the product of two sinewaves at f_1 and f_2 producing mixing products. Classically, a highly selective filter is required to recover only the useful signal at $f_1 - f_2$ and that filter contributes significantly to the total surface of the PLL. Based on an all-digital architecture, the down-conversion frequency mixer (DFM) does not require any filter to produce the wanted frequency (cf. Fig. 5). The DFM mixer works as a single side band mixer (SSB) that results in a reduction in spurs [6], [17]. The XOR gate carries out the multiplication, the NAND gate the addition, the NOT gate the phase shift, and the SR-latch the synchronization. This mixer requires only near-quadrature signals; it is thus suitable for RO.

IV. MEASUREMENT RESULTS

The dual-loop PLL prototype has been fabricated using 28nm FD-SOI CMOS technology from STMicroelectronics. The die photography is depicted in Fig. 6 with a total active area of 0.346 mm^2 . The total power consumption is 0.749 mW in GNSS mode and 1.127 mW in WiFi mode, where both loops are active. The main power-hungry block is the LC-VCO, which consumes 0.596 mW. The RO has a power consumption of 0.033 mW and the digital part, including the PFD, the charge pump, the dividers, and the mixer, has a power consumption of 0.498 mW.

In GNSS mode, Fig. 7 shows the output spectrum of the PLL at the frequency of 1.27875 GHz with a feedback divider configured to divide by 125. Figure 8 presents the PN analysis of the reference frequency and GNSS mode, respectively. The PN at 1 MHz offset from the carrier is -104.58 dBc/Hz. The

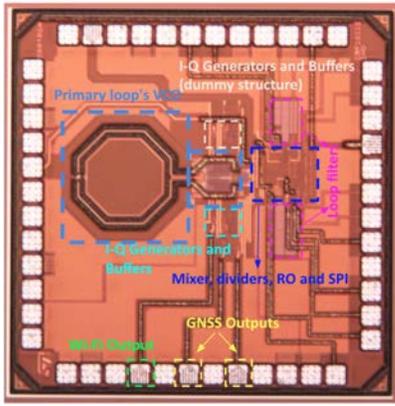


Fig. 6. Die photography.

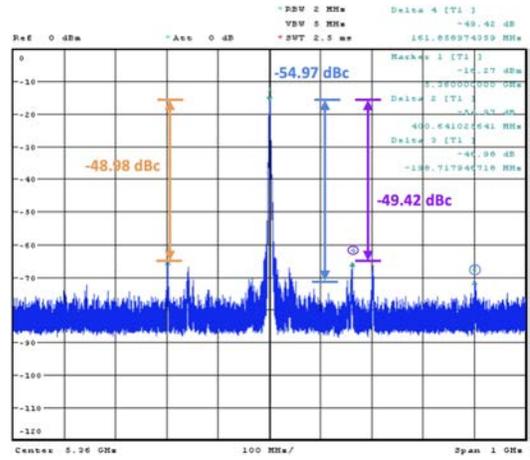


Fig. 9. Frequency spectrum of the WiFi mode output.

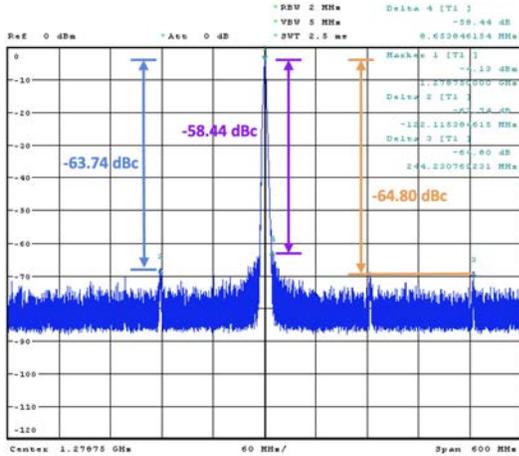


Fig. 7. Frequency spectrum of the GNSS mode output.

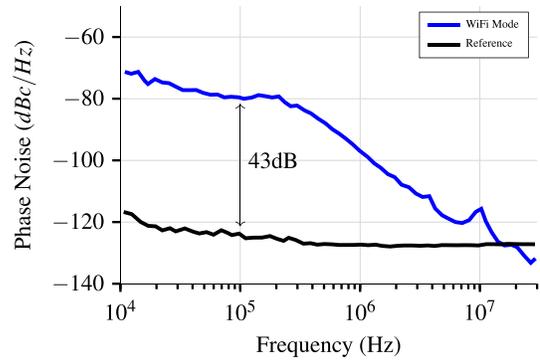


Fig. 10. Phase Noise results from the WiFi mode.

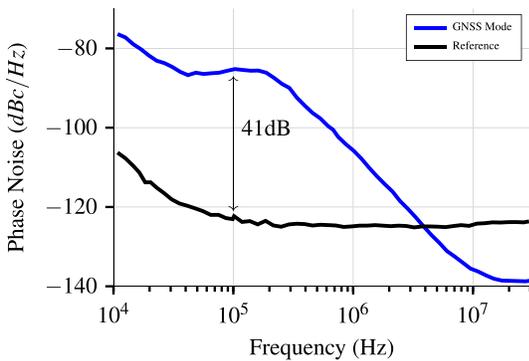


Fig. 8. Phase Noise results from the GNSS mode.

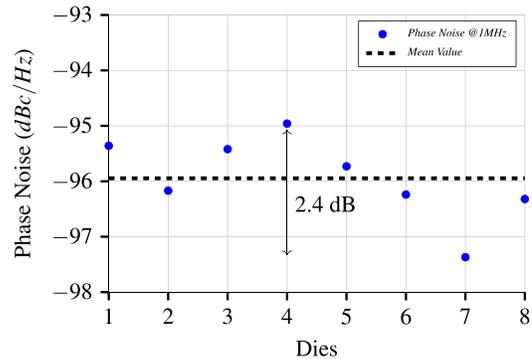


Fig. 11. Phase Noise results (WiFi mode) for 8 different dies.

multiplication of the reference PN by a rate of $20\log(N_1)$ can be seen in the low-frequency behavior of the GNSS PN result. The PN was integrated from 10 kHz to 100 MHz to figure out the RMS jitter, which resulted in 5.2 ps.

In WiFi mode, Fig. 9 shows the output spectrum at the frequency of 5.36 GHz with a configuration of the reference dividers R and $R + X$ to divide by 8 and 10, respectively, and the feedback dividers N_1 and N_2 to divide by 88 and 24. The secondary loop output frequency of 960 MHz is then obtained. Additionally, the mixer output frequency is 4400 MHz. Figure 10 presents the PN analysis of the

reference frequency and WiFi mode, respectively. The PN at 1 MHz offset from the carrier is -97.37 dBc/Hz. The in-band PN at the output depends on the values given by the frequency dividers N_1 and N_2 . The reference dividers also contribute to the low-frequency PN by multiplying the reference noise by a factor of $(N_1/R) + (N_2/R + X)$. The PN was integrated from 10 kHz to 100 MHz to compute the resulting jitter, which is 2.38 ps.

The PN variability analysis shows a robust result on the measurements of eight dies as depicted in Fig. 11. The worst-case results in -94.96 dBc/Hz at 1 MHz offset from the carrier. The measured dies of the same wafer show only a 2.4 dB variation around the mean value of -95.95 dBc/Hz. The performance of

TABLE II
COMPARISON WITH THE STATE-OF-THE-ART

	This Work	[4]	[5]	[7]	[8]	[9]	[2]	[3]
Technology(nm)	28	40	65	40	65	65	65	40
Standard	WiFi 5 GHz	GNSS	N.A.	N.A.	N.A.	N.A.	GNSS	GNSS
Frequency bands	N.A.	L1/L2/L3/L5/E6	N.A.	N.A.	N.A.	N.A.	L1/L2/L5/S	L1
Frequency range (GHz)	5.16-5.72	1.17-1.57	0.5-0.8	4.5-6.0	3.3-4.5	3.0-5.2	N.A.	1.47-1.67
Output frequency (GHz)	5.36	1.28	0.6	5.5	4.41	3.6	5.05	1.58
Ref. frequency (MHz)	400	40.92	37.5	100	100	32	31.25	26
Frequency resolution (MHz)	10	40.92	0.0021	0.0031	N.A.	N.A.	N.A.	N.A.
Ref. spur (dBc)	-49.42	-63.74	-55	N.A.	N.A.	-102.3	-77	N.A.
RMS jitter (ps)	2.38	5.2	10	0.648	0.292	1.78	1.22	N.A.
Integ. range (Hz)		10k-100M	20k-100M	1k-30M	10k-10M	10k-100M	1k-30M	N.A.
Phase noise (dBc/Hz) ^a	-97.37	-104.58	-95	-110.1	-110.97	-96 ^d	-101.6	-113.7
Supply voltage (V)		1	0.9	N.A.	1.1	1	1	1.3
Power consumption(mW)	1.127	0.749	0.253	9.88	2.4	18.1	10.1	N.A.
FOM (dB) ^b	-231.95	-226.93	-208.5	-233.8	-246.9	-222.4	-228	N.A.
Area (mm ²)		0.346	0.0166	0.108	0.36	0.338	0.54	N.A.
Power spending per frequency (mW/GHz) ^c	0.21	0.58	0.42	1.80	0.54	5.02	2	N.A.

^a@1 MHz.

^bFOM=20log(RMS jitter/1s)+10log(Power/1 mW).

^cPower spending per frequency=Power Consumption (mW)/Output frequency (GHz).

^d@300 kHz.

the proposed dual-loop PLL in its entire operation is summarized and compared with the state-of-the-art in Table II. This brief performs similar FoM for WiFi mode compared to [5] and for L1 band compared to [3]. These results demonstrated that the proposed architecture is an alternative to the fractional-N topology with lower complexity, good power efficiency, and achieving comparable PN performances.

V. CONCLUSION

This brief presents a dual-loop PLL in 28nm CMOS FD-SOI technology. The proposed architecture appears as an alternative to the fractional-N architecture to overcome the technological bottleneck of bandwidth and frequency resolution trade-off for indoor and outdoor positioning on a single integrated circuit. It can operate according to GNSS and WiFi standards thanks to its ability to reach the frequency bands L1, L2, L3, L5, and E6 together with the 57 WiFi channels. This dual-mode architecture is the first of its kind for indoor positioning with WiFi assistance and outdoor positioning with GNSS. Its milliwatt-range power consumption allows long-life battery operation, even when the continuous-time operation mode is required.

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