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Design and fabrication of nanometer measurement platform for better understanding of silicon mechanical properties

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ABSTRACT

Semiconductor industry is experiencing unprecedented growth, still driven by Moore's law, which is continually delivering devices with improved performance at lower costs. The continuation of this development places the industry in a divergent trade-off between economic attractiveness, technological feasibility, and the need for further performance improvement. Since the mainstream semiconductor technologies are silicon-based, new disruptive innovations are needed to gain additional performance margins. The use of nanowires is the preferred approach for preserving electrostatic control in the MOS transistor channel, and the application of mechanical stress is a booster of carrier mobility. It is in this context that this paper presents the design, fabrication, theoretical modeling, and characterization of a measurement platform to characterize the mechanical tensile stress of extremely narrow Si nanowires as small as 14.2 ± 1.12 nm in width. The proposed measurement platform enables a precise control of uniaxial strain, in terms of both amplitude and location, through the implementation of a stoichiometric Si_3N_4 pulling strand exerting a high tensile force on silicon nanowires. Reported devices are fabricated using a silicon-on-insulator wafer with fully complementary metal-oxide-semiconductor-compatible processing and top-down approach. It is observed that the mechanical strength of nanostructured Si is size-dependent and increases with miniaturization. Characterization revealed a record tensile strength value of $7.53 \pm 0.8\%$ (12.73 ± 1.35 GPa) for the narrowest nanowires fabricated using a top-down approach.

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I. INTRODUCTION

Silicon (Si) is a cornerstone material for modern electronics for more than 60 years,^{1–5} laying foundations for the unprecedented growth of the semiconductor industry, which continually delivers smaller [Fig. 1(a)], cheaper [Fig. 1(b)], and faster [Fig. 1(c)] devices owing to enormous progress in Si-based technologies, e.g., complementary metal-oxide-semiconductor (CMOS).

To define directions and targets for progress, the semiconductor industry agreed to create an International Technology Roadmap

for Semiconductors (ITRS), which was subsequently integrated into the International Roadmap for Devices and Systems (IRDS). ITRS/IRDS roadmaps are providing reliable forecasts of the semiconductor industry development. IRDS/ITRS also makes it possible to trace the historical evolution of the key performance of semiconductor devices.

For about five decades,^{1,6,7} the semiconductor industry was driven by Moore's law,⁸ which imposed miniaturization and a down-scaling trend in nanoelectronics [see Fig. 1(a)]. However, it is

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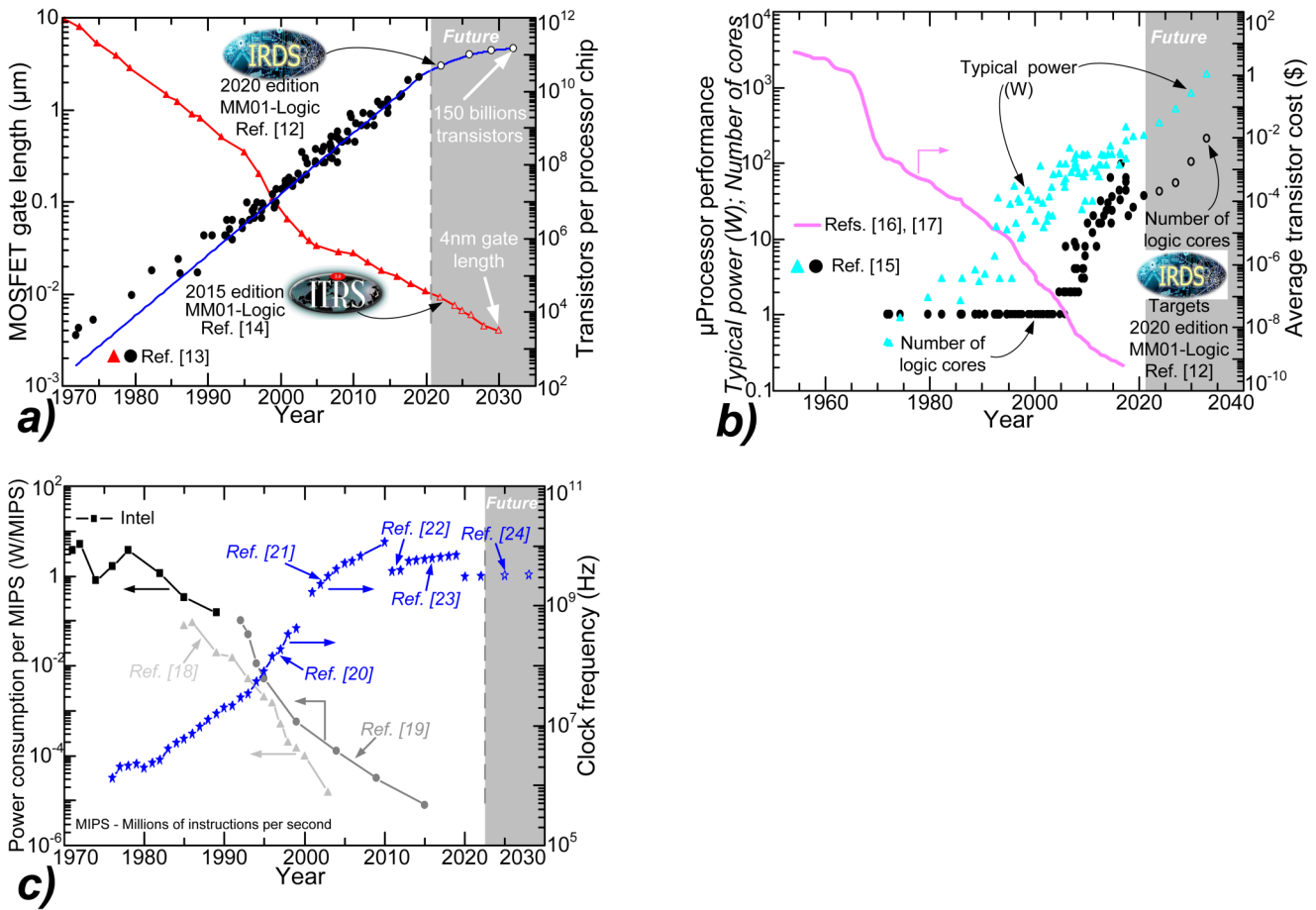


FIG. 1. An historical perspective and future forecast of digital industry and devices. Filled symbols for reported historical data and unfilled symbols for forecasted future data. (a) Miniaturization and densification trend in electronics,^{12–14} (b) past¹⁵ and predicted¹² μ Processor performance benchmarked with historical transistor price,^{16,17} and (c) power consumption per millions of instructions per second (MIPS)^{18,19} confronted with clock frequency.^{20–24}

impossible to continually decrease the device's size due to enormous cost involved, and the limit of granularity at the atom-bond scale irrevocably approaches.⁹ This is why Moore's law has been developing since the 2000s in tandem with an approach for diversifying integrated electronic functions referred to as More-than-Moore.^{10,11} The saturation of integration density and device dimensionality can be observed, for example, in the forecasted flattening of the curve reflecting the number of transistors per chip [see the blue line in the upper right corner in Fig. 1(a)]. Simultaneously, it is worth pointing out that despite the economic and physical limits of chip miniaturization and densification, their performance is constantly improved. Figure 1 illustrates the exceptional progress in performance, reaching decades for some parameters, with simultaneous cost reduction made possible by Si-based technologies.

Nevertheless, despite years of research and countless experiments, Si still conceals properties and physical effects that inspire the scientific community around the world. The level of miniaturization achieved has recently revealed interesting Si properties of

considerable industrial importance, e.g., thickness-dependent thermal conductivity reduction,^{25–29} carrier separation,^{30,31} advanced optical properties,^{32–37} increased carrier mobility with mechanical strain,^{38–47} terahertz (THz) plasma waves,^{48–54} and CMOS device performance boost.^{55–59} Moreover, as THz devices and the market are developing very rapidly in recent times, the fabrication of such devices on Si is challenging due to doping-dependent THz absorption and low carrier mobilities. Therefore, the application of strain can bring considerable relief to THz applications by enabling the fabrication of low cost and industrially compatible devices for THz emission and detection. Finally, interesting effects have also been observed in the field of plasmomechanics where mechanical stress is introduced into the THz devices.^{60–63}

Even though the miniaturization trend, illustrated in Fig. 1(a), cannot be sustained any longer, the market still needs performance enhancement beyond improvement delivered by scaling. One opportunity for further improving metal-oxide-semiconductor

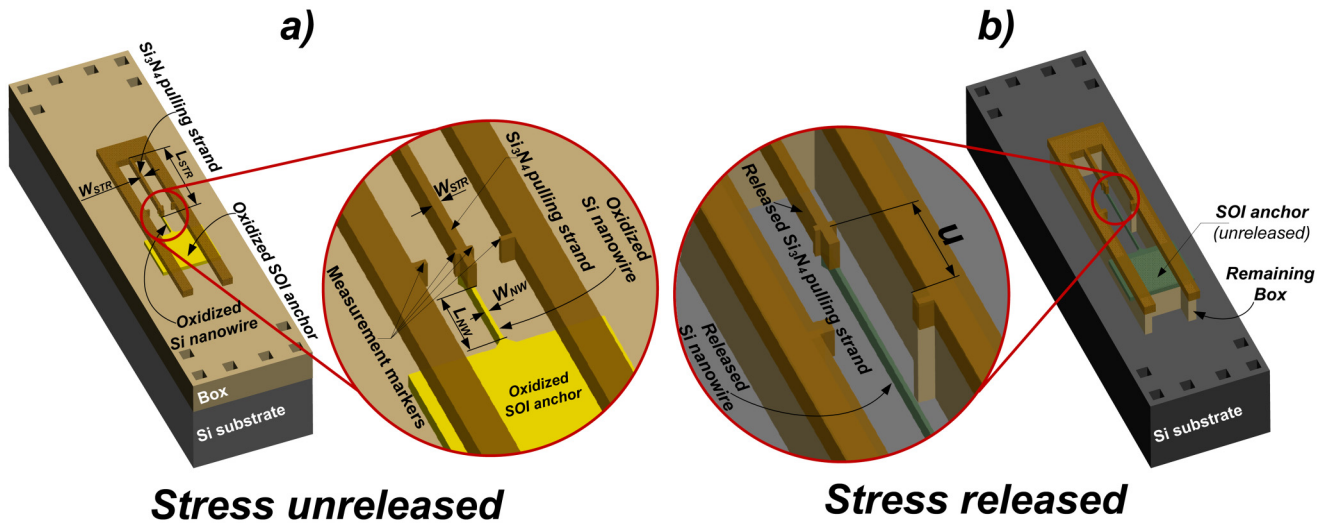


FIG. 2. Principle of operation of the measurement platform for Si nanowire tensile strength characterization: (a) before releasing the Si₃N₄ residual stress; (b) after applying Si₃N₄ tensile stress to Si nanowires.

field effect transistors (MOSFETs) is to increase mobility by introducing mechanical stress into nanometric scale channels^{64–67} or a stress-induced resistance change in Si nanowires (NW).⁶⁸ In this light, research into the mechanical properties of Si at nanoscale is of utmost relevance for the development of latest sub-5 nm CMOS technology nodes and for future evolution of the CMOS industry in general.⁶⁹

The ever-deepening knowledge of Si is not only propelled by scientific curiosity, but Si still remains at the center of attention owing to (i) its low cost (~0.23\$/kg for raw materials⁷⁰), (ii) unlimited reserves, (iii) simplicity, (iv) harmlessness, (v) availability, and

(vi) industrial compatibility (all CMOS technologies use Si wafers produced by millions daily). Spurred on by the evidence that Si remains and will remain the cornerstone of future electronics, this paper investigates the outstanding increase in the mechanical tensile strength in Si nanowires. Last but not least, the use of nanowires is the preferred approach for preserving electrostatic control in the MOS transistor channel and the application of mechanical strain enhances carrier mobility to levels much higher than in any other geometry. In this context, this paper investigates the mechanical properties of Si at the nanoscale using a measurement platform specially designed to apply a variable tensile stress to Si NW until

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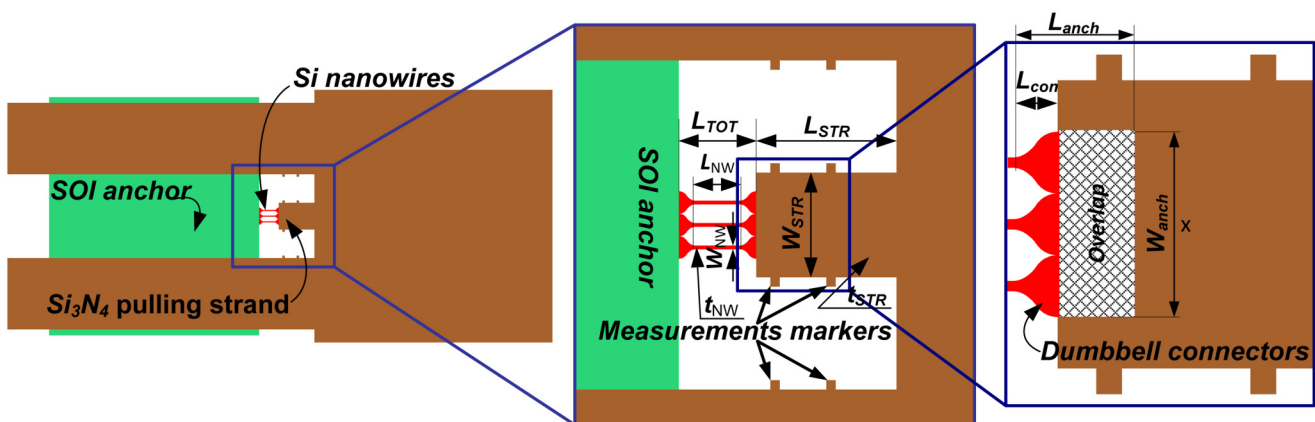


FIG. 3. Detailed layout of a unitary nanometer measurement platform for the evaluation of mechanical properties of three nanowires associated in parallel. Successive zooms present the nanowire geometry that accommodates an increase in width toward the anchoring area in the form of a rounded transition referred to as dumbbell connectors.

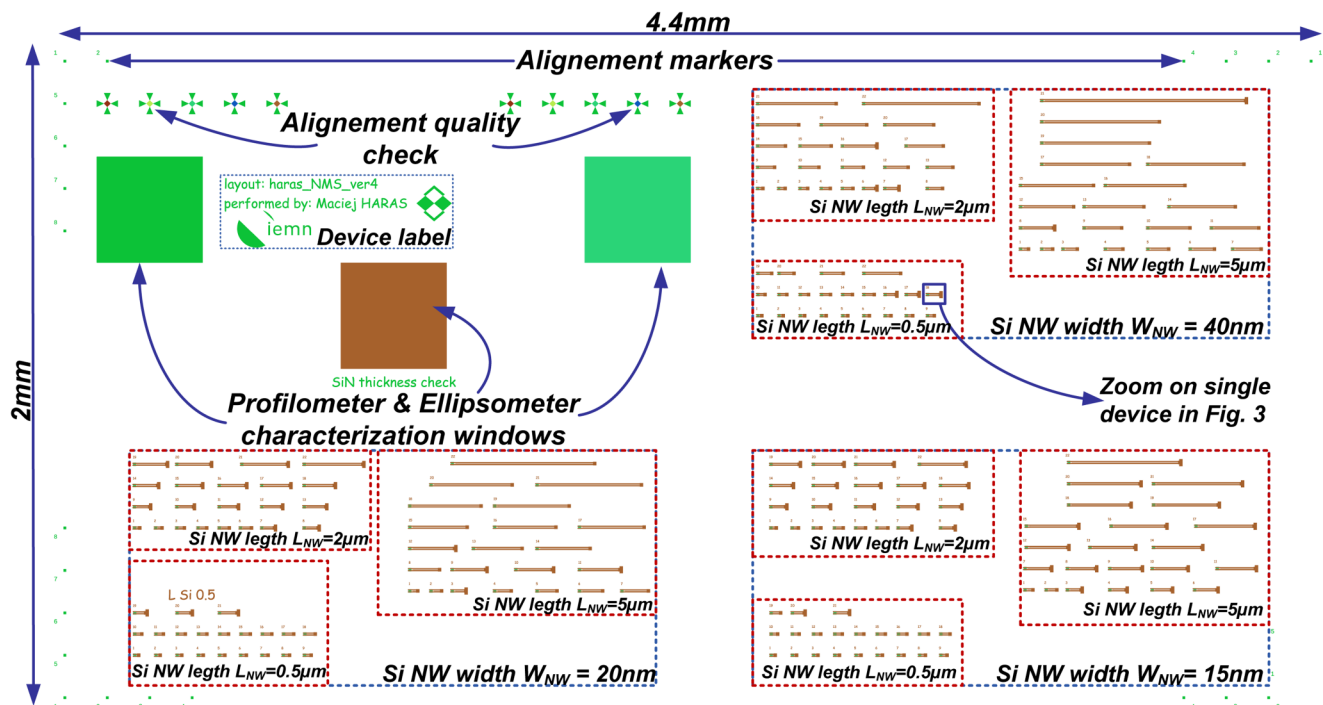


FIG. 4. Layout of the chip comprising three subsets of unitary measurement platforms associated with each nanowire width. Each subset is composed of 66 unitary platforms covering three nanowire lengths and a range of different lengths of pulling strands. A total of 10 chips were fabricated.

breakage. The tensile strength was statistically characterized on a large population of nanowires of different lengths and widths but constant Si thickness. Finally, the experimental results are compared with the theoretical model.

II. METHODS

A. Principle of operation

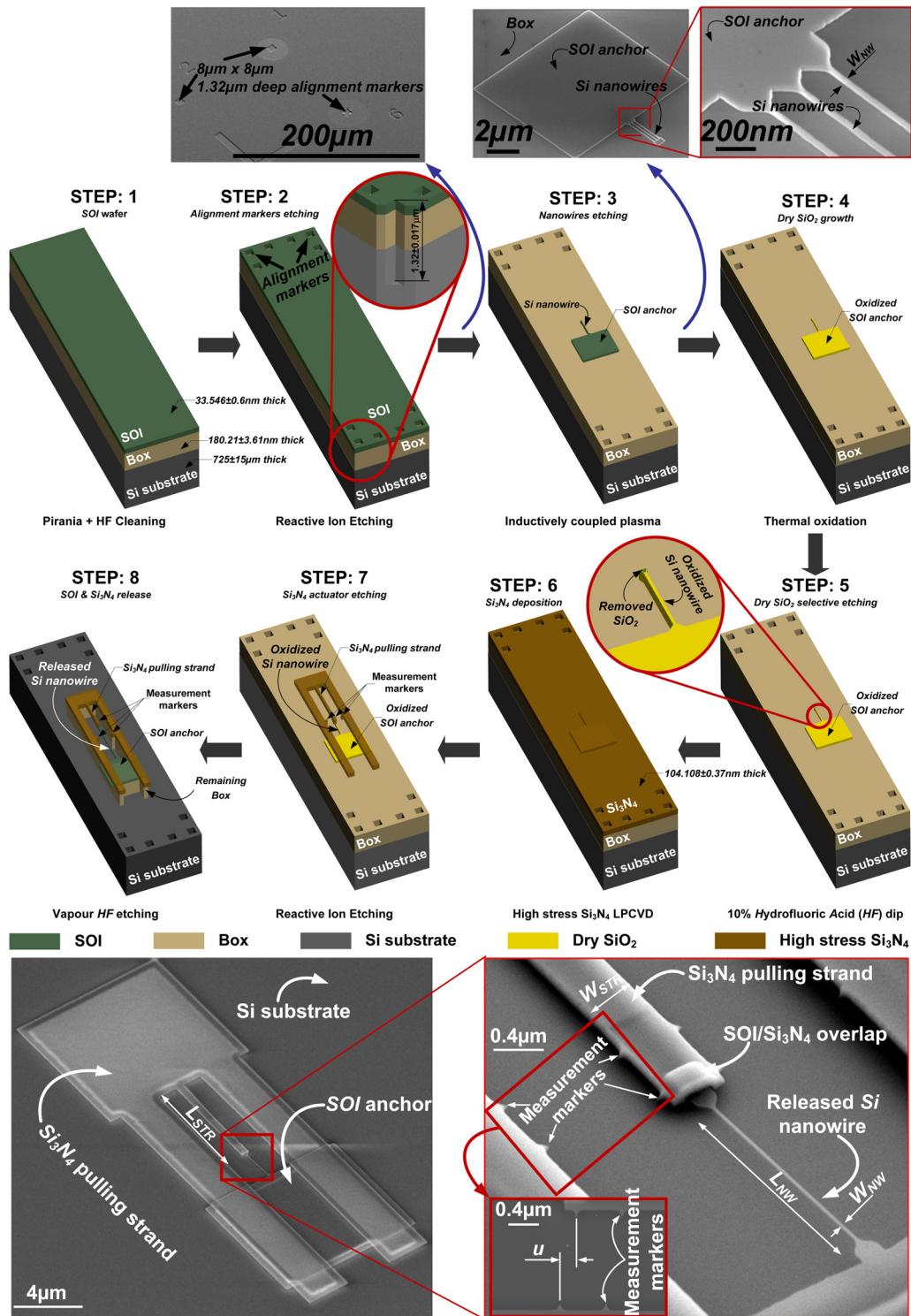
To accurately and efficiently characterize the Si NW tensile strength, an integrated measurement platform must (i) focalize the mechanical stress only on nanowires under tests; (ii) apply only uniaxial stress to the nanowires; (iii) apply the known/predefined value of stress to the wires; (iv) provide variation in the applied stress in order to determine the Si NW mechanical strength; (v) and provide a possibility to use a non-invasive (contactless) measurement technique in order to eliminate measurement interaction with NW under test, which can alter the mechanical characterization. Integrating all these requirements in a single device is a real challenge, as is characterizing the mechanical properties of materials with nanometric size. The literature reports a few examples of such measurement platforms coupled to measurement techniques based on scanning electron microscopy (SEM), Raman spectroscopy, or atomic force microscopy (AFM).^{71–81}

The guiding idea is to evaluate the tensile stress that a Si NW can withstand through the measurement of its elongation (u) under the application of a uniaxial tensile force. This force is

exerted by a silicon nitride (SiN) strand, which acts as an actuator. A distinctive and underlying feature of the associated measurement platform is the suspension of both the NW and the SiN strand. On the one hand, the suspension of the NW ensures that it is only subjected to the mechanical load of the SiN strand on one side, while the other side is clamped to a heavy anchor. On the other hand, the strand is patterned into a layer of SiN whose initial state of tensile stress is released by the suspension process step. This yields a final configuration after suspension where the SiN strand pulls on the NW in a uniaxial mode. This concept is illustrated in Fig. 2, which also gives a detailed view of platform construction. This last illustration highlights two key states in the fabrication of the measurement platform, namely, before and after the nanowire and strand suspension. When the suspension is not yet realized [Fig. 2(a)], all measurement markers are aligned. When uniaxial tensile stress is released after suspension [Fig. 2(b)], the u of the nanowire is observed, which results from the loading of the nanowire by the pulling force of the SiN strand.

B. Experimental implementation

The proposed measurement platform is fabricated using a silicon-on-insulator (SOI) wafer. This measurement platform uses the high internal tensile stress (~ 1 GPa) of SiN in its stoichiometric (Si_3N_4) formula,⁸² which is loading the Si NW. This stress is originating from the Si/Si₃N₄ thermal expansion coefficients mismatch, which



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FIG. 5. Fabrication process flow of a nanometer measurement platform for characterization of Si nanowire mechanical properties. The final device is presented in the SEM micrographs; the inset presents the extension u of the nanowire when applied Si₃N₄ residual tensile stress.

is introduced while performing high-temperature low-pressure chemical vapor deposition (LPCVD) of Si_3N_4 .⁸³ The Si NW is structured in the top layer of the SOI substrate and is connected with a heavy anchor at one end. This anchor features a much larger cross-sectional area than the nanowire. At the other end, the SiN pulling strand is connected mechanically to the nanowire [see Fig. 2(a)]. In order not to generate stress concentration points, each end of the nanowire accommodates an increase in width toward the anchoring area in the form of dumbbell-shaped connectors as shown in Fig. 3. At this stage, before suspension, the whole structure rests on the buried oxide (BOX) so that no stress is yet released. The width of the SiN pulling strand (W_{STR}) and that of Si NW (W_{NW}) are much narrower than the dimensions of the SOI anchor and other parts of the SiN layer, making it possible to remove the BOX layer under the Si NW and SiN pulling strand without totally under-etching other parts of the platform. The removal of the BOX layer under the SiN strand and the Si NW [see Fig. 2(b)] eliminates the mechanical coupling with the BOX layer and loads the Si NW with the pulling force of the SiN strand. It is worth noting that the top Si layer has very low initial residual stress, of the order of 30 MPa,⁸⁴ so that the structural mechanics is dominated by the mismatch stress of the SiN layer. Until the tensile strength of the Si is exceeded, the strand stress is compensated by the nanowire, which is reflected by an elongation of the Si NW length. An accurate

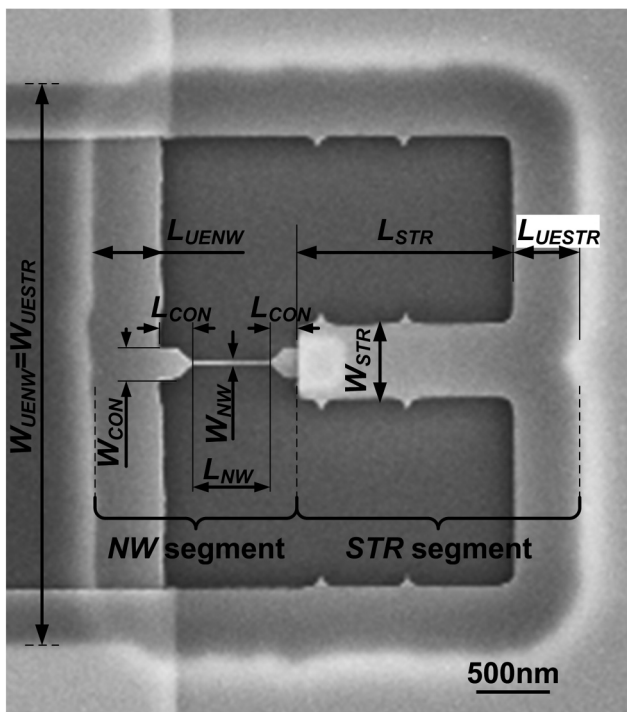


FIG. 6. SEM top view of the strain measurement platform showing the two segments associated with the nanowire (NW) and the SiN strand (STR). Characteristic dimensions used to account for extrinsic contributions due to BOX underetching (L_{UENW} , W_{UENW} , L_{UESTR} , W_{UESTR}) and the relative impact of dumbbell-shaped connections to nanowires (L_{CON} , W_{CON}) are detailed.

measurement of u is possible by means of markers located on the mobile part and on the fixed outer parts of the SiN layer. The distance u is characterized using SEM, which is a contactless method with minimal impact on characterized nanowires.

The loading force exerted by the released SiN strand depends significantly on its length (L_{STR}), thickness (t_{STR}), and width (W_{STR}). Thus, this opens up interesting possibilities for (i) performing a statistical analysis of the tensile stress sustained by the wires and (ii) determining the maximum stress before the fracture of the nanowires.

C. Framing of the experimental design

The characterization of material mechanical properties at the nanoscale requires an adapted approach at both topological and technological levels. Modern nanotechnology opens possibilities to expose deep sub- μm patterns using ultrahigh-resolution e-beam lithography. Using this method, a topology of the nanometer measurement platform for tensile strength investigation in Si nanowires was designed (Fig. 4). Varying the strand dimensions (t_{STR} , W_{STR} , and L_{STR}) changes the pulling force applied to the nanowire and, thus, allows to modulate its amplitude over a wide range. In order to provide as broad a mechanical characterization of the nanostructured Si as possible, a set of nanowires and SiN strands of different dimensions was fabricated. Figure 4 illustrates the entire chip layout with a set of measurement platforms featuring varying dimensions of Si nanowires and SiN pulling strands. Nanowires with identical W_{NW} and L_{NW} are grouped as shown in Fig. 4, and for each group, L_{STR} is varied so as to gradually increase the applied tensile strain. This approach allows us to easily detect the maximal L_{STR} before the nanowire mechanical failure to determine the tensile strength of nanostructured Si.

Finally, two configurations of the platforms were designed: (i) a single nanowire (the bottom SEM picture in Fig. 5) and (ii) three identical nanowires in parallel (the top SEM picture in Fig. 5). Owing to that, an enlargement of the measurement range is achieved because three parallel nanowires will sustain strain from longer (longer L_{STR}) strands.

In general, material parameters are given as a range rather than as a fixed value. This is because their measurement is always subject to error, but also because the parameters may vary slightly due to imperfections, defects, or non-uniformities in the material. The layout of measurement platforms is, therefore, also designed to enable the statistical processing of the data. Each chip consists of 195 unitary measurement platforms. Such a large number of platforms allow a precise sweep of the applied stress achieved by small variations in L_{STR} , forming in addition a large population for statistical data processing.

D. Device fabrication

The fabrication process flow is illustrated in Fig. 5. The starting point is the SOI wafer, with $\sim 1.5 \times 10^{15} \text{ cm}^{-3}$ acceptor concentration (resistivity range $\rho_p = 8.5\text{--}11.5 \Omega \text{ cm}$). First, the SOI is cleaned in piranha solution (30 ml 96% $\text{H}_2\text{SO}_4 + 10 \text{ ml } 30\% \text{ H}_2\text{O}_2$) and native oxide is removed using 10% hydrofluoric acid (10% HF) dip for 1 min (step 1). Next, 49-point ELLipsometric (ELL) mapping was performed in order to determine SOI and BOX thicknesses and

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TABLE I. Values of parameters used in theoretical modeling for all characterized lengths $L_{NW} = 0.5, 2, \text{ and } 5 \mu\text{m}$, number in brackets in underscore represent measurement population.

L_{NW} (μm)	L_{STR} (μm)	Number of nanowires	W_{NW} (nm)	t_{SOI}	t_{NW}	t_{UENW}	W_{STR} (nm)	t_{STR}	t_{CON} (nm)	t_{UESTR} (nm)	L_{CON} (nm)	W_{CON} (nm)	L_{UESTR} (μm)	W_{UESTR} (μm)
0.5	1-30	1	$14.2 \pm 1.1_{(9)}$				620	$88.8 \pm 9.9_{(6)}$	265		205			
2	1-60		$18.2 \pm 1.0_{(13)}$										0.48	
5	1-120	3	$38.8 \pm 1.5_{(20)}$				1060	$73.4 \pm 0.6_{(10)}$	265		650			3.53
			$15.9 \pm 1.6_{(78)}$											
			$20.1 \pm 1.3_{(72)}$											
			$40.6 \pm 1.4_{(72)}$											

wafer uniformity [see Fig. SM1(a) and SM1(b) in the supplementary material for initial SOI and BOX thicknesses mapping, respectively]. ELL characterization determined average thicknesses of $t = 33.546 \pm 0.6$ and 180.21 ± 3.61 nm for top Si (SOI) and BOX layers, respectively. ELL mapping revealed also that the thicknesses of stack materials are very uniform upon the entire wafer. The information of initial thicknesses is needed to tune the duration of etching in further fabrication steps. After ELL characterization, the fabrication of etched alignment markers (step 2) is performed. The alignment markers are transferred into the wafer using electron-beam lithography and, subsequently, etched in an SF_6/Ar and $\text{CF}_4/\text{N}_2/\text{O}_2$ atmosphere by reactive ion etching (RIE) yielding markers with a depth of $1.32 \pm 0.017 \mu\text{m}$. High-resolution e-beam lithography using hydrogen silsesquioxane (HSQ) negative tone resist is subsequently performed in order to structure Si nanowires and SOI anchors. After HSQ development in 25% tetramethyl ammonium hydroxide (TMAH) for 60 s, the SOI is selectively etched to reach the BOX using inductively coupled plasma (ICP) in a chlorine atmosphere (see the corresponding SEM picture in Fig. 5). Consequently, a thin etch stop layer of dry silicon dioxide (SiO_2) is thermally grown (step 4) and a 49-point ELL mapping returned 9.138 ± 0.861 nm of the SiO_2 thickness. In step 5, e-beam lithography is performed to define regions of selective dry SiO_2 removal in 5% HF for 5 s. Those regions will improve the mechanical junction between remaining SOI and Si_3N_4 deposited in step 6 [see Fig. SM1(c), in the supplementary material for Si_3N_4 thickness mapping]. Deposited 104.108 ± 0.37 nm thick stoichiometric Si_3N_4 possesses a residual tensile stress of 622 MPa,⁸² which is applied to the Si NW via a mechanical junction fabricated in step 5. Subsequently, a Si_3N_4 pulling strand is structured using RIE until reaching the dry SiO_2 sacrificial layer (step 7). The fabrication is completed by releasing the Si_3N_4 residual stress, which is done in step 8 where BOX is underetched using HF in the vapor phase.

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III. RESULTS

Based on the measurement principle and physical implementation of the experimental platform described in Secs. I and II, u is determined by evaluating the distance between moving and fixed markers under SEM observation as illustrated in Fig. 5. The breakage mechanism of nanowires under mechanical tension can be induced by very slight process variations or by the presence of extended or point defects. Here, only unbroken nanowires were considered and the measurements are systematically accompanied by the number of nanowires that survived the mechanical stress.

A. Analytical modeling

As a first approximation, the strain (ϵ) in the nanowire is given by Eq. (1),⁷² where L_{NW} is the initial length of the nanowire before the application of the tensile force, i.e., before suspension,

$$\epsilon = \frac{u}{L_{NW}}. \tag{1}$$

The mechanical coupling between the nanowire and the SiN strand can be expressed theoretically by formulating the equilibrium condition of the forces exerted on these two elements.⁷³ The

load condition expressed for the actuator is given by the following equation:

$$F_{STR} = E_{STR} \times S_{STR} \times \left(\epsilon_{STR}^m - \frac{u}{L_{STR}} \right), \quad (2)$$

where E_{STR} is the Young modulus of the Si_3N_4 strand, while $S_{STR} = t_{STR} \times W_{STR}$ is the associated cross-sectional area. ϵ_{STR}^m refers to the mismatch strain between the SiN layer and the underlying SOI layer. This is the strain in the strand resulting from the mismatch stress in the SiN layer before its release by suspension. The difference $\left(\epsilon_{STR}^m - \frac{u}{L_{STR}} \right)$, therefore, constitutes the residual strain that prevents the SiN strand from being totally relaxed because it is loaded by the Si NW . As a result, this strain difference is reflected in the load force F_{STR} exerted by the strand on the nanowire after suspension. Complementarily, the load condition expressed for the Si NW is given by the following equation:

$$F_{NW} = N \times E_{NW} \times S_{NW} \times \left(\frac{u}{L_{NW}} \right), \quad (3)$$

where E_{NW} is the Young modulus of the Si NW oriented along the $\langle 110 \rangle$ direction and $S_{NW} = t_{NW} \times W_{NW}$ is the cross-sectional area of a unitary nanowire with t_{NW} and W_{NW} being its thickness and width, respectively. N is the number of nanowires attached to the SiN strand. In Eq. (3), we have assumed that no mismatch strain exists between the top Si layer and the BOX of the used SOI wafer, as already mentioned hereinbefore. By applying the equilibrium condition $F_{STR} = F_{NW}$, u and the uniaxial strain ϵ_{NW} associated with the Si NW are expressed by the following equations, respectively:⁷³

$$u = \frac{\epsilon_{STR}^m}{N \times \frac{E_{NW} \times S_{NW}}{E_{STR} \times S_{STR}} \times \frac{1}{L_{NW}} + \frac{1}{L_{STR}}}, \quad (4)$$

$$\epsilon_{NW} = \frac{u}{L_{NW}}, \quad (5)$$

where L_{STR} is the length of the SiN strand before suspension. The above mechanical analysis, however, proves to be simplistic in that some of the measured elongation takes place in the dumbbell connectors. To a lesser degree, some of this elongation also comes from the undercutting of the BOX in the anchor area. In order to better take into account these extrinsic contributions in solving the mechanical problem, the measurement platform is divided into two segments associated with the nanowire and the SiN strand, respectively, as shown in Fig. 6.

The nanowire segment can be divided into three parts: (i) the underetched portion of the anchor area (L_{UENW} , W_{UENW} , and t_{UENW}), (ii) the intrinsic nanowire (L_{NW} , W_{NW} , and t_{NW}), and (iii) the dumbbell-shaped connectors (L_{CON} , W_{CON} , and t_{CON}) as shown in Fig. 6. The three variables in parenthesis associated with each part represent the length, width, and thickness of that part. It is worth noting here that $t_{NW} = t_{UENW} = t_{CON} = t_{SOI}$ is the thickness of the top layer of the SOI wafer. Complementarily, the SiN strand segment is composed of two parts: the intrinsic strand (L_{STR} ,

W_{STR} , and t_{STR}) and the under-etched portion of the anchor area (L_{UESTR} , W_{UESTR} , and t_{UESTR}). Here, $t_{STR} = t_{UESTR} = t_{SOI}$ is the thickness of the SiN strand. Following the basic law of deformation summation in objects composed of parts of the varying cross-sectional area, the elongation of the nanowire and strand segments can be expressed by the following equations, respectively, where $F = F_{NW} = F_{STR}$ represents the axial internal load applied to each segment:

$$\begin{aligned} u &= \frac{F \times L_{NW}}{N \times E_{NW} \times S_{NW}} + \frac{F \times L_{UENW}}{N \times E_{UENW} \times S_{UENW}} + \frac{2 \times F \times L_{CON}}{N \times E_{CON} \times S_{CON}} \\ &= \frac{F}{E_{SOI} \times S_{SOI}} \times \left(L_{NW} + L_{UENW} \times \frac{W_{NW}}{W_{UENW}} + 2 \times L_{CON} \times \frac{W_{NW}}{W_{CON}} \right) \\ &= \frac{F}{E_{SOI} \times t_{SOI} \times W_{NW}} \times L_{NWEFF}, \end{aligned} \quad (6)$$

$$\begin{aligned} u &= \frac{F \times L_{STR}}{E_{STR} \times S_{STR}} + \frac{F \times L_{UESTR}}{E_{UESTR} \times S_{UESTR}} \\ &= \frac{F}{E_{SiN} \times S_{SiN}} \times \left(L_{STR} + L_{UESTR} \times \frac{W_{STR}}{W_{UESTR}} \right) \\ &= \frac{F}{E_{SiN} \times t_{SiN} \times W_{STR}} \times L_{STREFF}, \end{aligned} \quad (7)$$

where $E_{SOI} = E_{NW} = E_{UENW} = E_{CON}$ is the Young modulus of Si in the $\langle 110 \rangle$ crystal direction and $E_{SiN} = E_{STR} = E_{UESTR}$ is the Young modulus of stoichiometric Si_3N_4 . The inspection of Eqs. (6) and (7) yields the effective lengths L_{NWEFF} and L_{STREFF} for the nanowire and SiN strand, respectively. The two effective lengths $L_{NWEFF} = L_{NW} + L_{UENW} \times (W_{NW}/W_{UENW}) + 2 \times L_{CON} \times (W_{NW}/W_{CON})$ and $L_{STREFF} = L_{STR} + L_{UESTR} \times (W_{STR}/W_{UESTR})$ can be substituted for L_{NW} and L_{STR} in Eqs. (4) and (5) to properly take into account the extrinsic extensions in the two segments depicted in Fig. 6. Given the position of the measurement markers, it is important to emphasize that the experimental strain, which will be discussed in the following, reflects that of the composite nanowire structure including the dumbbell-shaped connectors and the correction due to the BOX undercut. The experimental strain is, therefore, calculated based on the ratio between the measured elongation and L_{NWEFF} in Eq. (6). Naturally, the contributions from extrinsic elements are more pronounced as the length of the nanowire is shorter. For the sake of completeness, the set of dimensional parameters used in the model developed hereinbefore is summarized in Table I, and structural parameters are given in Table II.

It is worth noting that the thickness of the nitride layer t_{SiN} differs for platforms with one or three nanowires, and in triple nanowire platforms, the nitride layer is $\sim 21\%$ thinner compared to the single nanowire platform, as reported in Table I. Despite that observation, both devices were fabricated on the same wafer and the thickness difference can be explained by different etching durations at the end of the fabrication process flow in step 8 (see Fig. 5). Triple Si nanowire devices have wider Si_3N_4 tensile strands (bigger W_{STR}) than in single nanowires; thus, the etching time in step 8 is adequately extended for three wire platforms in order to achieve total BOX removal under the SiN tensile strand. The etch

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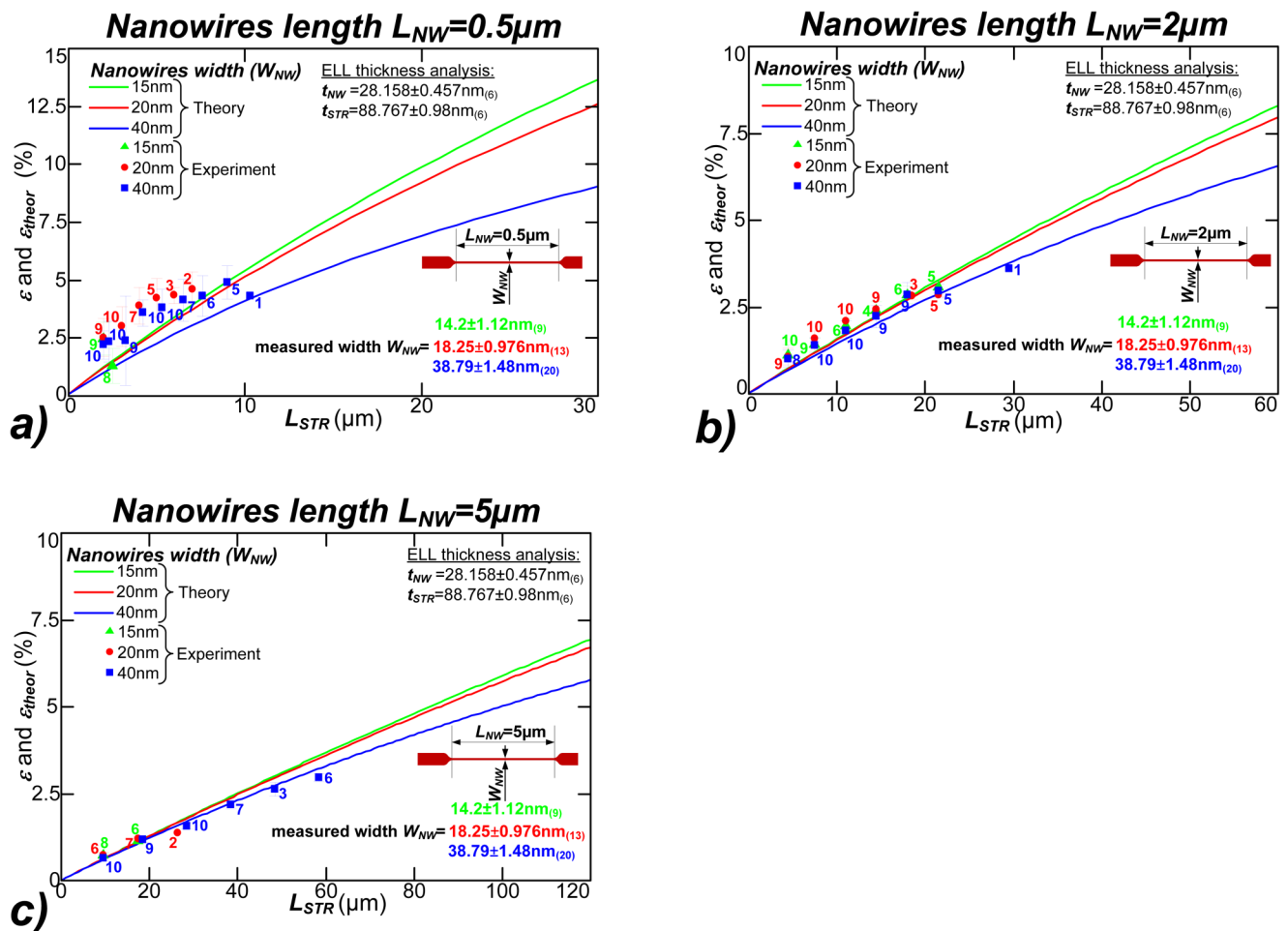
TABLE II Mechanical parameters.

Structural parameter	Variable name	Value	Unit
Silicon Young modulus $\langle 110 \rangle$ ^{72,86-90}	$E_{\text{SOI}} = E_{\text{NW}} = E_{\text{UENW}} = E_{\text{CON}}$	165.8	GPa
Silicon nitride Young modulus (Si_3N_4) ⁸⁵	$E_{\text{SiN}} = E_{\text{STR}} = E_{\text{UESTR}}$	230	GPa
Silicon nitride mismatch strain (measured)	$\varepsilon_{\text{STR}}^m$	0.0033	...

rate of 1–6 nm/min of SiN in vapor HF is reported in the literature depending mainly on the etching temperature.^{91,92}

Figures 7 and 8 compare the experimental data with the theoretical model for measured Si nanowires in single and triple configurations as a function of the length SiN pulling strand. Note that

L_{STREFF} is also substituted to L_{STR} on the horizontal axis in these figures, but this correction only introduces a marginal shift given its magnitude. Markers stand for the experimental data, while continuous lines correspond to the theoretical model. Note that values of nanowires $W_{\text{NW}} = 15, 20,$ and 40 nm are represented by colors:



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FIG. 7. Strain in a single Si nanowire as a function of length of Si₃N₄ pulling strand for (a) $L_{\text{NW}} = 0.5 \mu\text{m}$, (b) $L_{\text{NW}} = 2 \mu\text{m}$, and (c) $L_{\text{NW}} = 5 \mu\text{m}$. The experimental results (points) are taken for all platforms with an unbroken wire. Continuous lines correspond to theoretical modeling. Blue, red, and green colors are for nominal nanowire widths of $W_{\text{NW}} = 40, 20,$ and 15 nm, respectively. Labels close to t_{NW} , t_{STR} , and W_{NW} values indicate the limited number of measurements used to calculate the average value of these parameters. Labels near data points represent the population of successful measurements on unbroken nanowires. The ratio of unbroken to broken nanowires is easy to calculate considering that 10 specimens of each measurement platform were available from 10 fabricated chips.

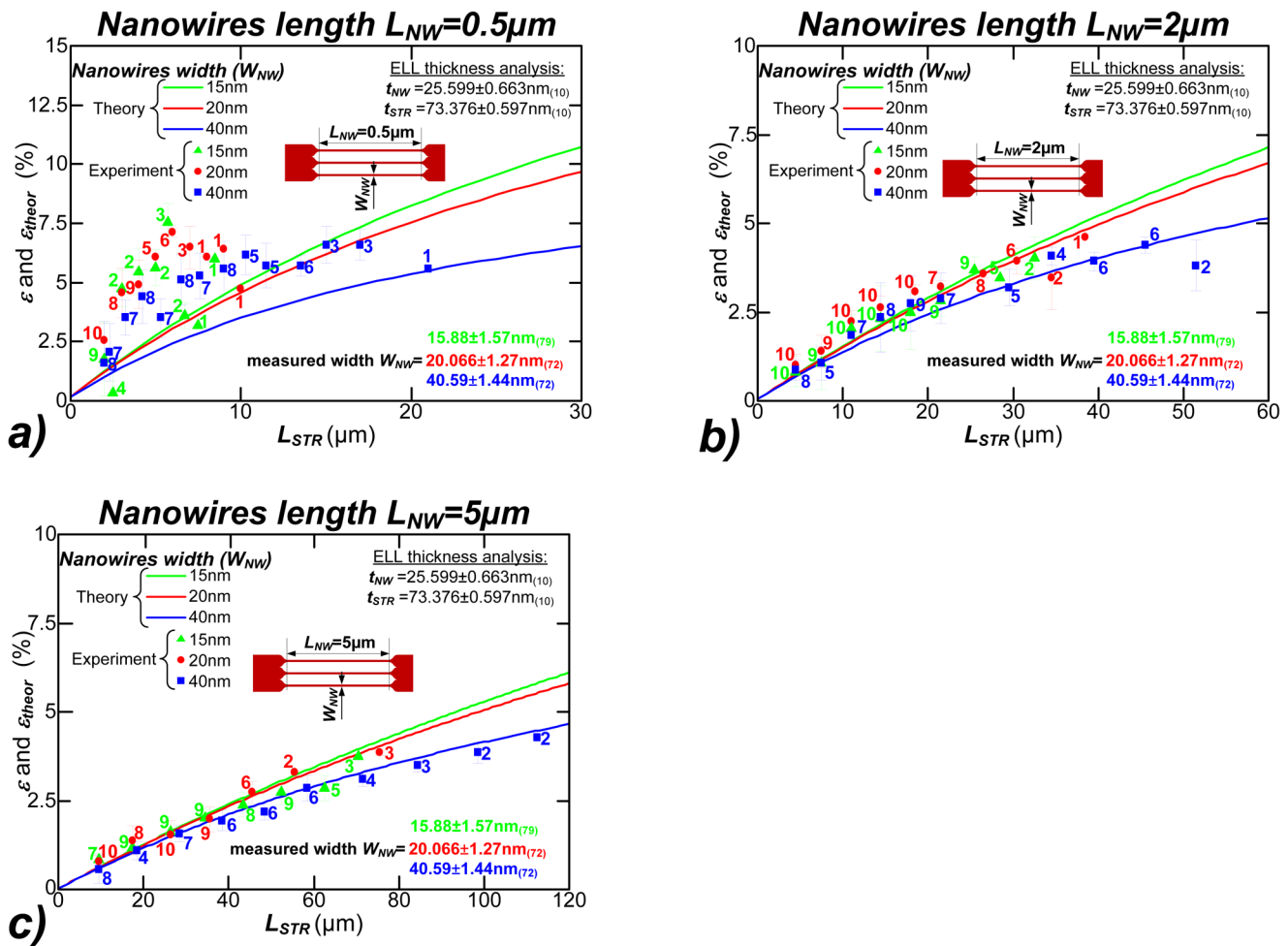


FIG. 8. Strain in three parallel Si nanowires as a function of length of Si_3N_4 pulling strand for (a) $L_{\text{NW}} = 0.5 \mu\text{m}$, (b) $L_{\text{NW}} = 2 \mu\text{m}$, and (c) $L_{\text{NW}} = 5 \mu\text{m}$. The experimental results (points) are taken for all platforms with three unbroken wires. Continuous lines correspond to theoretical modeling. Blue, red, and green colors are for nominal nanowire widths of $W_{\text{NW}} = 40, 20,$ and 15 nm , respectively. Labels close to t_{NW} , t_{STR} , and W_{NW} values indicate the limited number of measurements used to calculate the average value of these parameters. Labels near data points represent the population of successful measurements on unbroken nanowires. The ratio of unbroken to broken nanowires is easy to calculate, considering that 10 specimens of each measurement platform were available from 10 fabricated chips.

green, red, and blue, respectively. In order to reduce the impact of the imprecision of the measurement method, a statistical representation of measured strain was used. Labels close to data points indicate the population of measured platforms.

We report a maximum tensile strain of $4.9 \pm 0.7\%$ (tensile strength $8.28 \pm 1.18 \text{ GPa}$) for single nanowire configuration and $7.53 \pm 0.8\%$ (tensile strength $12.73 \pm 1.35 \text{ GPa}$) for three nanowires in parallel. These strain values lead to the conclusion that nanowires, owing to their dimensionality, are significantly outperforming mechanical parameters of bulk Si (fracture strain of $0.18\% - 0.6\%$ ^{93,94}). Comparing the results between single- and three-nanowire configurations, it can be observed that three nanowires in parallel are extending the measurement range enabling characterization for longer L_{STR} . This is explained by the fact that three parallel nanowires are

mechanically stronger and the Si_3N_4 pulling strand must be longer for the wires to reach the fracture point. The presented characterization method uses the SEM measurements of Si nanowire elongation (u) probed between the measurement markers [see Fig. 2(a)] for graphical definition. The elongation readout is subjected to the error of the operator and the SEM image resolution. After error analysis (see the supplementary material for details), the SEM-induced ϵ inaccuracy is between $\pm 0.223\%$ (for the shortest L_{NW}) and $\pm 0.0225\%$ (for the longest L_{NW}) and has a minor impact on characterization results.

To fairly compare the results depicted in Figs. 7 and 8 with those in the literature, the synthesis technique is an important comparative factor. In the literature, two Si nanowire fabrication techniques are the most popular: (i) vapor-liquid-solid (VLS) growth or (ii) top-down etching. VLS technique produces very small

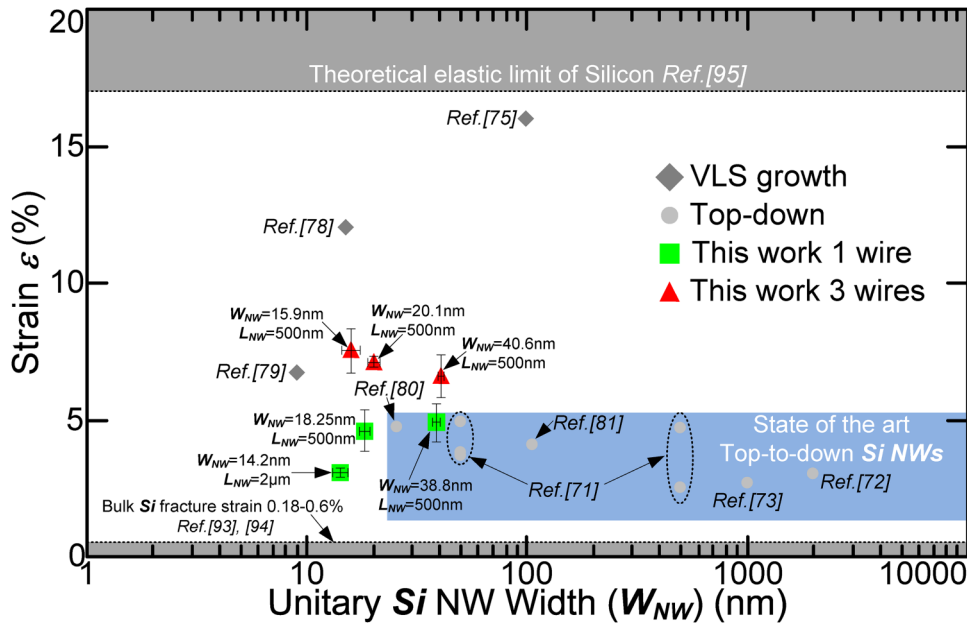


FIG. 9. Maximal supported strain vs width for Si nanowires reported in the literature emphasizing their fabrication technique (VLS growth^{75,78,79}; top-down^{71-73,80,81}) and highlighting the theoretical elastic limit⁹⁵ and bulk fracture strain^{93,94}. Error bars are representing standard deviations for mean Si nanowires width (for x axis bar) and strain (for y axis bar) taken from Figs. 7 and 8, respectively.

nanowires with very pure and regular crystalline structure.^{75,79} However, the VLS-grown Si NW cannot be used on industrial scale due to fabrication technology and high cost related to it. In order to characterize mechanical properties of Si that is widely used in the semiconductor industry, a top-down technique must be used. This approach allows nanowires to be fabricated on the same wafers used industrially. Figure 9 benchmarks the ϵ of the Si NW reported in the literature emphasizing their fabrication technology and width. Its analysis leads to the conclusion that this work presents the narrowest Si nanowires withstanding the highest strain among the top-down etched devices reported in the literature.

B. Finite element method modeling

The above-described analytical model grasps the physics of the nanowire and strand deformation under the law of deformation summation in objects composed of different cross-sectional areas. This model, thus, describes the dumbbell connectors as parallelepipeds. However, the shape of these connectors is precisely aimed at avoiding abrupt transitions between the highly tensioned, small cross-sectional nanowire and the lowly tensioned large cross-sectional strand and under etched parts. It could be argued that simplification explains the small remaining discrepancy between the model and the experiments, especially in the case of short nanowires $L_{NW} = 0.5 \mu\text{m}$ as shown in Figs. 7(a) and 8(a). More precisely, the dumbbell connector in this case could accommodate a greater fraction of the strain exerted by the SiN strand relative to its actual length. To investigate this hypothesis, a series of finite element method (FEM) simulations were performed on a selected subset of parameters. The measurement platform has been modeled using the material parameters, lengths, widths, and thicknesses in accordance with the analytical model and using under etching lengths (L_{UENW}

and L_{UESTR}) and widths (W_{UENW} and W_{UESTR}) (see Fig. 6 for graphical definition) measured after fabrication. While the SEM analysis allows for measurements of the entire Si NW segment, thus integrating the displacement of dumbbell connectors, FEM modeling allows for a separate evaluation of the stress and deformation of all components of Si NW and SiN strand segments. Figure 10(a) shows the u , while Fig. 10(b) corresponds to the local deformation in the vicinity of the nanowire ($L_{NW} = 0.5 \mu\text{m}$). The color maps reflect the local values of displacement and deformation. As expected, the connection between the Si NW and SiN strand corresponds to the largest displacement. It is worth noting that the highest deformation occurs within the Si NW segment and that extrinsic contributions (dumbbell connectors, SiN strand deformation, etc.) are minor compared to deformation occurring in the nanowire. The connectors' shape plays its assigned role to ensure the continuous transition of deformation between the nanowire and external parts. Figure 10(c) compares the results from the analytical model (dark blue lines) and FEM simulations. The strain evaluated by FEM has been split to show the total strain of the NW segment as measured in the experiment (light blue lines) and the sole contribution of the nanowire (magenta lines). It can be underlined that analytical modeling and FEM modeling agree with good accuracy especially in the short SiN strand limit. The discrepancy in the long strand limit is attributed to an increasing out-of-plane deformation of the strand (not depicted here), which is neglected in the analytical model. We now compare the cases of short ($L_{NW} = 0.5 \mu\text{m}$) and longer ($L_{NW} = 2 \mu\text{m}$) nanowires shown in Fig. 10(c). In the case of longer nanowires, the role of extrinsic parts is quite negligible as the strain in the nanowire is almost equal to the strain within the full Si NW segment. However, for short ($L_{NW} = 0.5 \mu\text{m}$) wires, the fraction of strain supported by the dumbbell connectors is less negligible, especially for long strand sizes. The impossibility to separate those

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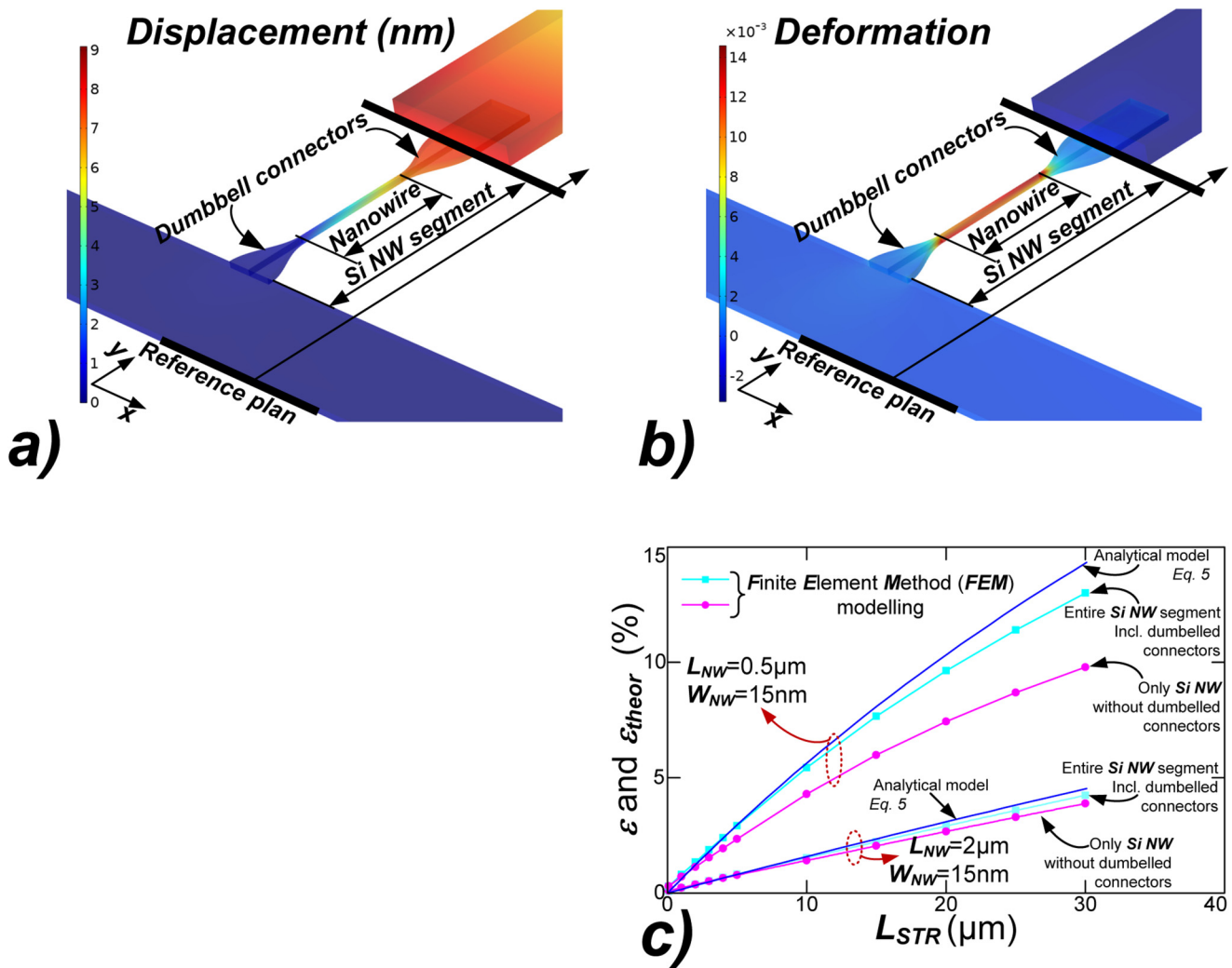


FIG. 10. Finite element method (FEM) modeling of uniaxially loaded Si nanowires: (a) displacement (u) in nm the color map depicts the local displacement with respect to the reference plan, (b) deformation results reveal that highest deformation occurs within the nanowire region, and (c) comparison of strain values obtained from the analytical model (blue continuous line) and FEM simulations (blue square and pink circle) for nanowires width $W_{NW} = 15$ nm and two different lengths $L_{NW} = 0.5$ and $2 \mu\text{m}$, and the strain of the sole nanowire segment is extracted (pink circle).

contributions during measurements can explain the better agreement of the analytical model with measurements in the $L_{NW} = 2$ and $5 \mu\text{m}$ cases.

IV. CONCLUSIONS

In this paper, we have demonstrated the design, fabrication process, characterization, and modeling of an integrated platform for measuring tensile strength in nanoscale Si nanowires. The novelty of our approach lies in the fact that a Si_3N_4 residual tensile strain is applied to Si nanowires in a very wide range using strands of different lengths L_{STR} . The result is the precise control of applied tensile stress, which can be achieved by an appropriate design. The

fabrication process is fully CMOS compatible, with platforms processed in a top-down configuration, which allows the characterization of the material identical to that in the industry. The tensile stress is released by dry etching with HF vapor, a technique that requires no mask, while SiO_2/Si selectivity is naturally assured. The presented process approach enables the fabrication of nanowires with widths (W_{NW}) as small as 14.2 ± 1.27 nm and as short as 500 nm, which is comparable to the channel size of MOSFETs in the most advanced technology nodes.

The characterization of these devices is non-contact and non-invasive, based on u elongation measurements using a SEM. As a result, characterization is easy to perform and has a minimal impact on the nanowires' integrity. In addition, SEM

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characterization makes it easier to build up a statistical representation of the measured nanowire population.

At first glance, Figs. 7 and 8 demonstrate the same trend for single and triple nanowire configurations. It can be observed that the agreement between the theory and experiment is better for longer nanowires (higher L_{NW}), as explained in the FEM analysis. Moreover, the calculation of the strain associated with long nanowires is less prone to error due to smaller and, therefore, more sensitive displacement measurements. The second observation is that, while increasing L_{STR} , the population of measured nanowires is becoming smaller. This is obviously the result of an increase in the stress applied to the nanowires, which increases the fracture probability. The third observation concerns the fact that, with increasing applied tensile strain using a longer strand (L_{STR}), nanowires begin to fail more rapidly when they have a smaller W_{NW} . A plausible hypothesis to explain the more fragile nature of narrow nanowires is that the volume/surface ratio is lower, resulting in a higher density of point defects, which are at the origin of mechanical failure. At low dimensionality, Si increases dramatically its tensile strength. A strain of $\sim 4.5\%$ was reported in Ref. 80 for 30 nm wide nanowires, 5% for 100 nm wide nanowires,⁹⁶ and 3.6% in $1\ \mu\text{m}$ Si nanowires.⁷² For the narrowest and the shortest nanowires, we report a strain of $7.53 \pm 0.8\%$ (tensile strength 12.73 ± 1.35 GPa) for the triple-nanowire configuration and $4.9 \pm 0.7\%$ (tensile strength 8.28 ± 1.18 GPa) for the single nanowire configuration, to date the highest figures achieved in a top-down fabrication approach. The presented topology and fabrication sequence enables, after optimization, to reach $W_{NW} \approx 10$ nm, allowing strain characterization in the range of the theoretical elastic limit of Si, estimated at 17%–20%.⁹⁵

SUPPLEMENTARY MATERIAL

See the supplementary material for more details on (i) the characterization of the SOI wafer material stack thickness and uniformity at the initial stage of the device fabrication and (ii) the measurement error analysis.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Maciej Haras: Conceptualization (lead); Data curation (lead); Investigation (lead); Methodology (lead); Writing – original draft (equal); Writing – review & editing (equal). **Jean-François Robillard:** Formal analysis (supporting); Funding acquisition (equal); Writing – original draft (equal); Writing – review & editing (equal). **Thomas Skotnicki:** Funding acquisition (lead); Supervision (supporting); Writing – original draft (equal); Writing – review & editing (equal). **Emmanuel Dubois:** Data curation (equal); Formal analysis (lead); Funding acquisition (lead); Supervision (lead); Writing – original draft (equal); Writing – review & editing (equal).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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