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Design and fabrication of nanometer measurement platform for better understanding of Silicon mechanical properties

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ABSTRACT

Semiconductor industry is experiencing unprecedented growth, still driven by the Moore's law, which is continually delivering devices with improved performance at lower costs. The continuation of this development places the industry in a divergent trade-off between economic attractiveness, technological feasibility and the need for further performance improvement. Since the mainstream semiconductor technologies are silicon-based, new disruptive innovations are needed to gain additional performance margins. The use of nanowires is the preferred approach for preserving electrostatic control in the MOS transistor channel and the application of mechanical stress is a booster of carrier mobility. It is in this context that this paper presents the design, fabrication, theoretical modelling and characterization of a measurement platform to characterize the mechanical tensile stress of extremely narrow *Si* nanowires as small as 14.2 ± 1.12 nm in width. The proposed measurement platform enables precise control of uniaxial strain, both in terms of amplitude and location, through the implementation of a stoichiometric Si_3N_4 pulling strand exerting a high tensile force on the silicon nanowires. Reported devices are fabricated using a Silicon *On Insulator* (*SOI*) wafer with fully *CMOS*-compatible processing and top-down approach. It is observed that mechanical strength of nanostructured *Si* is size-dependent and increases with miniaturization. Characterization revealed a record tensile strength value of $7.53 \pm 0.8\%$ (12.73 ± 1.35 GPa) for the narrowest nanowires fabricated using a top-down approach.

KEYWORDS: tensile strain, Silicon nanowires mechanical strength, mechanical characterization, nano fabrication, Finite Element Method modelling

INTRODUCTION

Silicon (*Si*) is a cornerstone material for modern electronics for more than 60 years¹⁻⁵, laying foundations for the unprecedented growth of semiconductor industry which continually delivers smaller (*FIG. 1a*), cheaper (*FIG. 1b*) and faster (*FIG. 1c*) devices owing to enormous progress in *Si*-based technologies e.g. Complementary Metal Oxide Semiconductor (*CMOS*).

To define directions and targets for progress, the semiconductor industry agreed to create an *International Technology Roadmap for Semiconductors (ITRS)* which was subsequently integrated into the *International Roadmap for Devices and Systems (IRDS)*. *ITRS/IRDS* roadmaps are providing reliable forecasts of the semiconductor industry development. *IRDS/ITRS* also makes it possible to trace the historical evolution of the key performance of semiconductor devices.

For about 5 decades^{1,6,7} semiconductor industry was driven by the *Moore's Law*⁸ which imposed miniaturization and down-scaling trend in nanoelectronics (*see FIG. 1a*). However, it is impossible to continually decrease the device's size due to enormous cost involved, and the limit of granularity at the atom-bond scale irrevocably approaches.⁹ This is why *Moore's Law* has been developing since the 2000s in tandem with an approach for diversifying integrated electronic functions referred to as *More-than-Moore*,^{10,11}. Saturation of integration density and device dimensionality can be observed, for example, in the forecasted flattening of the curve reflecting the number of transistors per chip (*see the blue line in the upper right corner in FIG. 1a*). Simultaneously, it is worth pointing out that despite the economic and physical limits of chip miniaturization and densification, their performance is constantly improved. *FIG. 1* illustrates the exceptional progress in performance, reaching decades for some parameters, with a simultaneous cost reduction made possible by *Si*-based technologies.

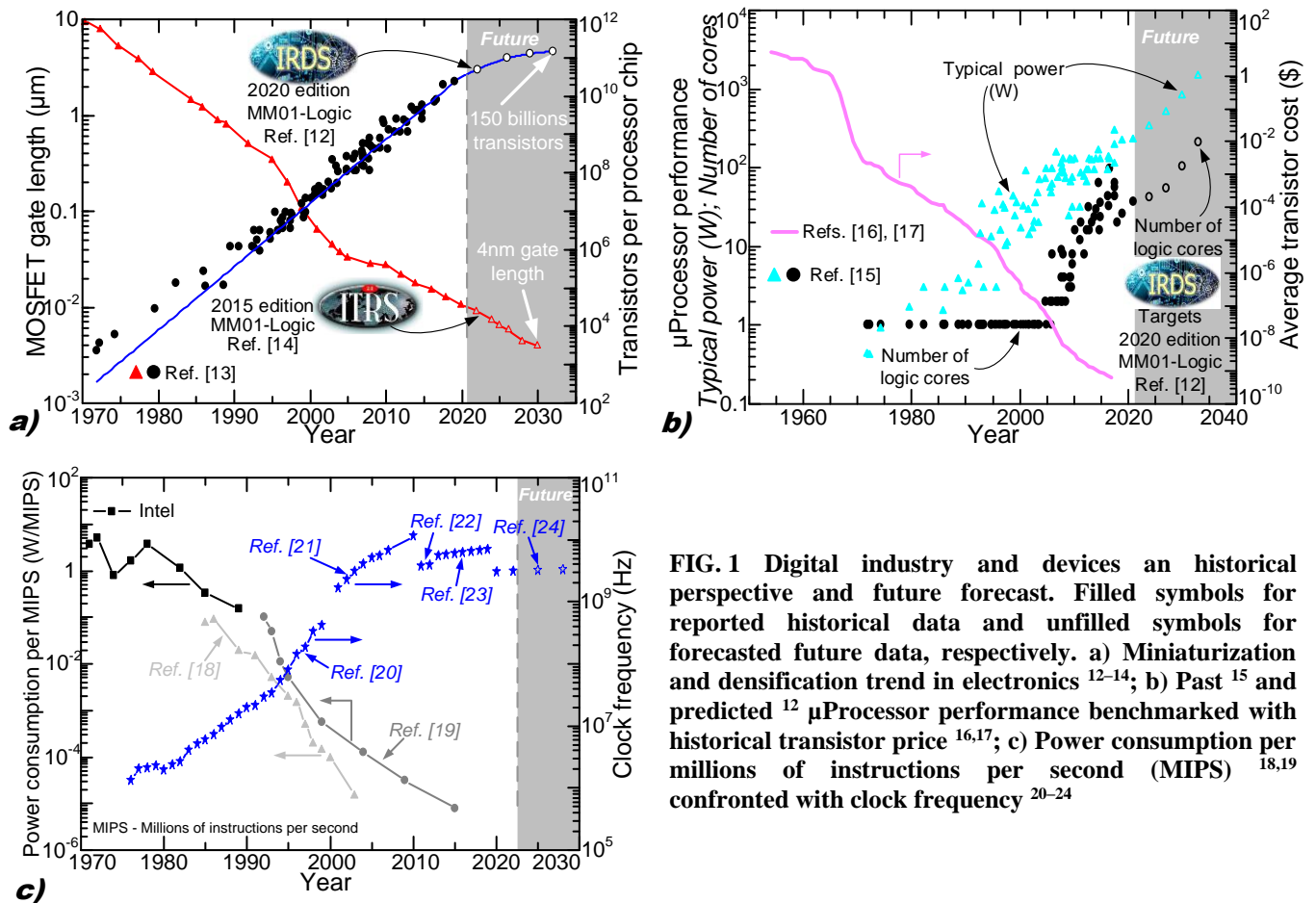


FIG. 1 Digital industry and devices an historical perspective and future forecast. Filled symbols for reported historical data and unfilled symbols for forecasted future data, respectively. a) Miniaturization and densification trend in electronics^{12–14}; b) Past¹⁵ and predicted¹² μ Processor performance benchmarked with historical transistor price^{16,17}; c) Power consumption per millions of instructions per second (MIPS)^{18,19} confronted with clock frequency^{20–24}

Nevertheless, despite years of research and countless experiments, *Si* still conceals properties and physical effects that inspire the scientific community around the world. The level of miniaturization achieved has recently revealed interesting *Si* properties of considerable industrial importance e.g. thickness dependent thermal conductivity reduction,^{25–29} carrier separation,^{30,31} advanced optical properties,^{32–37} increased carrier mobility with mechanical strain,^{38–47} TeraHerz (*THz*) plasma waves,^{48–54} *CMOS* devices performance boost.^{55–59} Moreover, as *THz* devices and market are developing very rapidly in recent times, the fabrication of such devices on *Si* is challenging due to doping-dependent *THz* absorption and low carrier mobilities. Therefore, the application of strain can bring considerable relief to *THz* applications by enabling the fabrication of low cost and industrially compatible devices for *THz* emission and detection. Finally, interesting effects have also been observed in the field of plasmomechanics where mechanical stress is introduced into the *THz* devices.^{60–63}

Even though the miniaturization trend, illustrated in FIG. 1a, cannot be sustained any longer, market still needs performance enhancement beyond improvement delivered by scaling. One opportunity for further improving *Metal Oxide Semiconductor Field Effect Transistors (MOSFETs)* is to increase mobility by introducing mechanical stress into nanometric scale channels^{64–67} or a stress-induced resistance change in *Si NanoWires (NW)*⁶⁸. In this light, research into the mechanical properties of *Si* at nanoscale is of utmost relevance for the development of the latest sub-5nm *CMOS* technology nodes and for future evolution of the *CMOS* industry in general.⁶⁹

The ever-deepening knowledge of *Si* is not only propelled by scientific curiosity, but *Si* still remains at the center of attention owing to: (i) its low cost (~ 0.23 \$/kg for raw material⁷⁰), (ii) unlimited reserves, (iii) simplicity, (iv) harmlessness, (v) availability and (vi) industrial compatibility (all *CMOS* technologies use *Si* wafers produced by millions daily). Spurred on by the evidence that *Si* remains and will remain the cornerstone of future electronics, this paper investigates the outstanding increase in mechanical tensile strength in *Si* nanowires. Last but not least, the use of nanowires is the preferred approach for

preserving electrostatic control in the *MOS* transistor channel and the application of mechanical strain enhances carrier mobility to levels much higher than in any other geometry. In this context, this paper investigates the mechanical properties of *Si* at the nanoscale using a measurement platform specially designed to apply a variable tensile stress to *Si NW* until breakage. The tensile strength was statistically characterized on a large population of nanowires of different lengths and widths but constant *Si* thickness. Finally, the experimental results are compared with the theoretical model.

METHODS

a. PRINCIPLE OF OPERATION

To accurately and efficiently characterize *Si NW* tensile strength, an integrated measurement platform must: (i) focalize the mechanical stress only on the nanowires under tests; (ii) apply only uniaxial stress to the nanowires; (iii) apply known/predefined value of stress to the wires; (iv) provide variation of applied stress in order to determine the *Si NW* mechanical strength; (v) provide a possibility to use a non-invasive (*contactless*) measurement technique in order to eliminate measurement interaction with *NW* under test which can alter the mechanical characterization. Integrating all these requirements in a single device is a real challenge, as is characterizing the mechanical properties of materials with nanometric size. The literature reports a few examples of such measurement platforms coupled to measurement techniques based on Scanning *Electron Microscopy (SEM)*, Raman spectroscopy or Atomic *Force Microscopy (AFM)*.^{71–81}

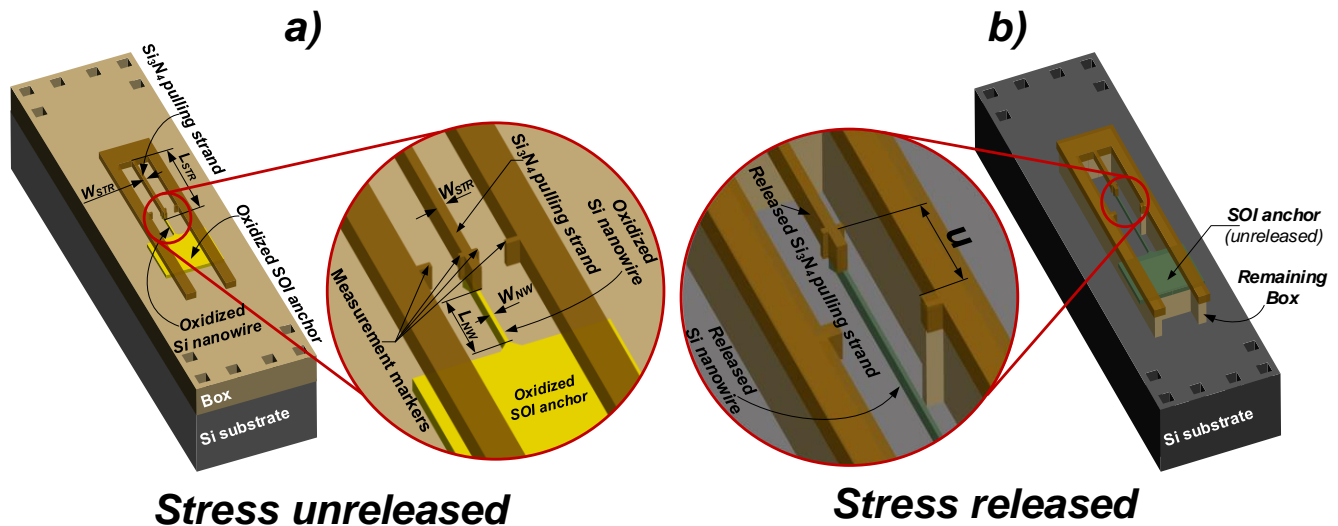


FIG. 2 Principle of operation of measurement platform for *Si* nanowire tensile strength characterization; a) before releasing the Si_3N_4 residual stress; b) after applying Si_3N_4 tensile stress to the *Si* nanowires

The guiding idea is to evaluate the tensile stress that a *Si NW* can withstand through the measurement of its elongation (u) under the application of a uniaxial tensile force. This force is exerted by a *Silicon Nitride (SiN)* strand which acts as an actuator. A distinctive and underlying feature of the associated measurement platform is the suspension of both the *NW* and the *SiN* strand. On one hand, the suspension of the *NW* ensures that it is only subjected to the mechanical load of the *SiN* strand at one side, while the other side is clamped to a heavy anchor. On the other hand, the strand is patterned into a layer of *SiN* whose initial state of tensile stress is released by the suspension process step. This yields a final configuration after suspension where the *SiN* strand pulls on the *NW* in an uniaxial mode. This concept is illustrated in FIG. 2 which also gives a detailed view of the platform construction. This last illustration highlights two key states in the fabrication of the measurement platform, namely, before and after the nanowire and strand suspension. When the suspension is not yet realized (FIG. 2a), all measurement markers are aligned. When uniaxial tensile stress is released after suspension (FIG. 2b), the u of the nanowire is observed which results from the loading of the nanowire by the pulling force of the *SiN* strand.

b. EXPERIMENTAL IMPLEMENTATION

The proposed measurement platform is fabricated using a Silicon *On Insulator* (*SOI*) wafer. This measurement platform uses the high internal tensile stress ($\sim 1\text{GPa}$) of *SiN* in its stoichiometric (Si_3N_4) formula⁸² which is loading the *Si NW*. This stress is originating from the *Si/Si₃N₄* thermal expansion coefficients mismatch which is introduced while performing high-temperature *Low Pressure Chemical Vapor Deposition* (*LPCVD*) of Si_3N_4 .⁸³ The *Si NW* is structured in the top layer of the *SOI* substrate and is connected with a heavy anchor at one end. This anchor features a much larger cross-sectional area than the nanowire. At the other end, the *SiN* pulling strand is connected mechanically to the nanowire (*see FIG. 2a*). In order not to generate stress concentration points, each end of the nanowire accommodates an increase in width towards the anchoring area in the form of dumbbell-shaped connectors as shown in FIG. 3. At this stage, before suspension, the whole structure rests on the buried oxide (*BOX*) so that no stress is yet released. The width of the *SiN* pulling strand (W_{STR}) and that of *Si NW* width (W_{NW}) are much narrower than the dimensions of *SOI* anchor and other parts of the *SiN* layer making it possible to remove the *BOX* layer under the *Si NW* and *SiN* pulling strand without totally under-etching other parts of the platform. The removal of the *BOX* layer under the *SiN* strand and the *Si NW* (*see FIG. 2b*) eliminates the mechanical coupling with the *BOX* layer and loads the *Si NW* with the pulling force of the *SiN* strand. It is worth noting that the top *Si* layer has very low initial residual stress, of the order of 30MPa ,⁸⁴ so that the structural mechanics is dominated by the mismatch stress of the *SiN* layer. Until the tensile strength of the *Si* is exceeded, the strand stress is compensated by the nanowire, which is reflected by an elongation of the *Si NW* length. An accurate measurement of u is possible by means of markers located on the mobile part and on the fixed outer parts of the *SiN* layer. The distance u is characterized using *SEM* which is a contactless method with minimal impact on the characterized nanowires.

The loading force exerted by the released *SiN* strand depends significantly on its length (L_{STR}) thickness (t_{STR}) and W_{STR} . Thus, this opens up interesting possibilities for: (i) performing a statistical analysis of the tensile stress sustained by the wires and (ii) determining the maximum stress before fracture of the nanowires.

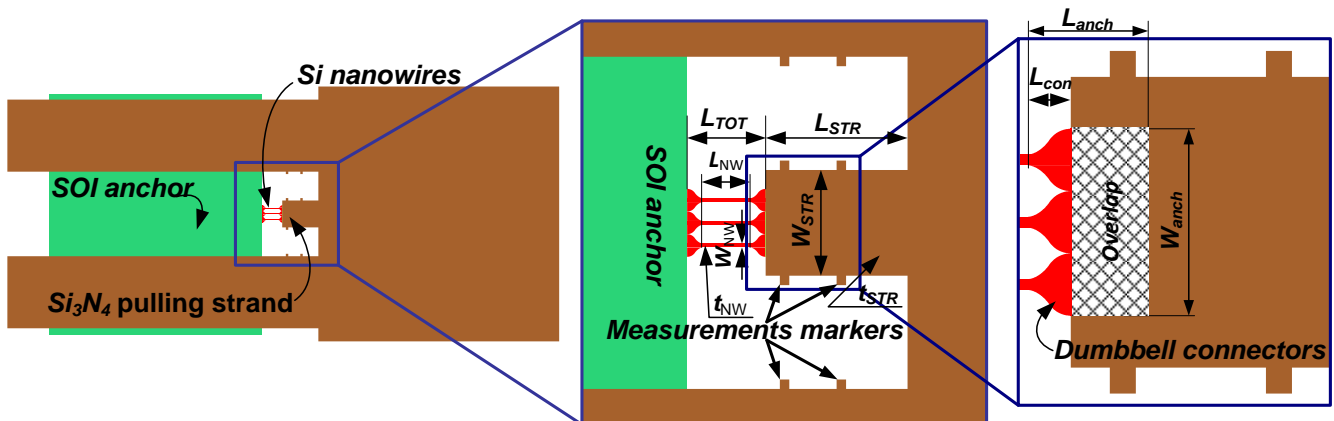


FIG. 3 Detailed layout of a unitary nanometer measurement platform for evaluation of mechanical properties of three nanowires associated in parallel. Successive zooms present the nanowire geometry that accommodates an increase in width towards the anchoring area in the form of a rounded transition referred to as dumbbell connectors.

c. FRAMING OF THE EXPERIMENTAL DESIGN

Characterization of material mechanical properties at the nanoscale requires adapted approach both at topological and technological levels. Modern nanotechnology opens possibilities to expose deep sub- μm patterns using ultra-high-resolution e-beam lithography. Using this method, a topology of nanometer measurement platform for tensile strength investigation in *Si* nanowires was designed (*FIG. 4*). Varying the strand dimensions (t_{STR} , W_{STR} and L_{STR}) changes the pulling force applied to the nanowire and thus allows to modulate its amplitude over a wide range. In order to provide as broad a mechanical

characterization of the nanostructured *Si* as possible, a set of nanowires and *SiN* strands of different dimensions was fabricated. FIG. 4 illustrates the entire chip layout with a set of measurement platforms featuring varying dimensions of *Si* nanowires and *SiN* pulling strands. Nanowires with identical W_{NW} and L_{NW} are grouped as showed in FIG. 4 and for each group L_{STR} is varied so as to gradually increase the applied tensile strain. This approach allows to easily detect the maximal L_{STR} before the nanowire mechanical failure to determine the tensile strength of nanostructured *Si*.

Finally, two configurations of the platforms were designed: (i) single nanowire (*bottom SEM picture in FIG. 5*) and (ii) three identical nanowires in parallel (*top SEM picture in FIG. 5*). Owing to that, an enlargement of the measurement range is achieved because three parallel nanowires will sustain strain from longer (*longer L_{STR}*) strands.

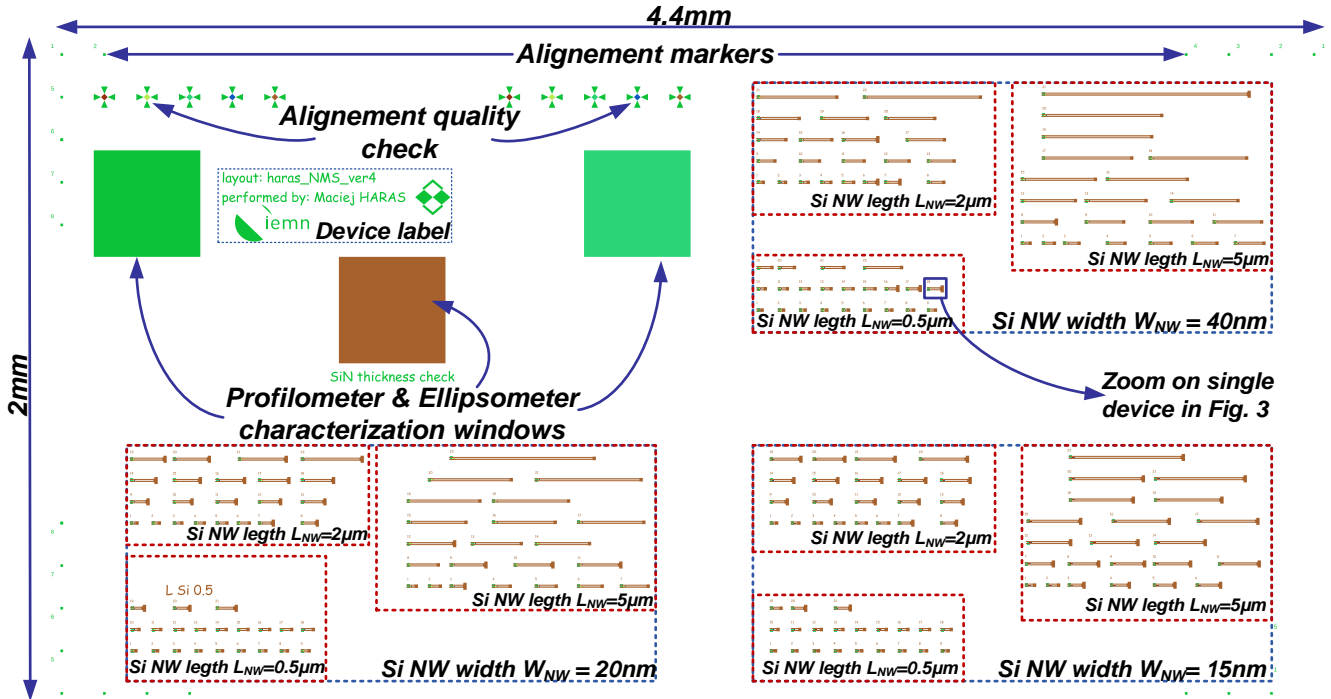


FIG. 4 Layout of the chip comprising 3 subsets of unitary measurement platforms associated with each nanowire width. Each subset is composed of 66 unitary platforms covering 3 nanowire lengths and a range of different lengths of pulling strands. A total of 10 chips was fabricated.

In general, material parameters are given as a range rather than as a fixed value. This is because their measurement is always subject to error, but also because the parameters may vary slightly due to imperfections, defects or non-uniformities in the material. The layout of measurement platforms is therefore also designed to enable statistical processing of the data. Each chip consists in 195 unitary measurement platforms. Such a large number of platforms allows a precise sweep of the applied stress achieved by small variations of L_{STR} , forming in addition a large population for statistical data processing.

d. DEVICE FABRICATION

The fabrication process flow is illustrated in FIG. 5. The starting point is the *SOI* wafer, with $\sim 1.5 \times 10^{15} \text{cm}^{-3}$ acceptor concentration (*resistivity range $\rho_p = 8.5 - 11.5 \Omega \cdot \text{cm}$*). Firstly, *SOI* is cleaned in piranha solution (30ml 96% $\text{H}_2\text{SO}_4 + 10\text{ml}$ 30% H_2O_2) and native oxide is removed using 10% HydroFluoric acid (10% *HF*) dip for 1min (*STEP 1*). Next, 49-points *ELL*ipsometric (*ELL*) mapping was performed in order to determine the *SOI* and *BOX* thicknesses and wafer uniformity (*see Fig. SM1a and Fig. SM1b Supplementary Material for the initial SOI and BOX thicknesses mapping, respectively*). *ELL* characterization determined average thicknesses of $t = 33.546 \pm 0.6 \text{nm}$ and $180.21 \pm 3.61 \text{nm}$ for top *Si* (*SOI*) and *BOX* layers, respectively. *ELL* mapping revealed also that the thicknesses of stack materials are very uniform upon the entire wafer. Information of the initial thicknesses is needed to tune the duration of etching in further fabrications steps. After *ELL*

characterization, the fabrication of etched alignment markers (**STEP 2**) is performed. The alignment markers are transferred into the wafer using electron-beam lithography and subsequently etched in SF_6/Ar and $CF_4/N_2/O_2$ atmosphere by **Reactive Ion Etching (RIE)** yielding markers with a depth of $1.32 \pm 0.017 \mu m$. A high-resolution e-beam lithography using **Hydrogen Silsesquioxane (HSQ)** negative tone resist is subsequently performed in order to structure **Si** nanowires and **SOI** anchors. After **HSQ** development in 25% **TetraMethylAmmonium Hydroxide (TMAH)** for 60 s, **SOI** is selectively etched to reach the **BOX** using **Inductively Coupled Plasma (ICP)** in a chlorine atmosphere (see corresponding **SEM** picture in the **FIG. 5**). Consequently, a thin etch stop layer of dry silicon dioxide (SiO_2) is thermally grown (**STEP 4**) and a 49 points **ELL** mapping returned $9.138 \pm 0.861 nm$ of the SiO_2 thickness. In **STEP 5**, an e-beam lithography is performed to define regions of selective dry SiO_2 removal in 5% **HF** for 5 s. Those regions will improve mechanical junction between remaining **SOI** and Si_3N_4 deposited in the following **STEP 6** (see Fig. **SM1c**, *Supplementary Material for Si_3N_4 thickness mapping*). Deposited $104.108 \pm 0.37 nm$ thick stoichiometric Si_3N_4 possesses residual tensile stress of 622MPa^{82,85} which is applied to **Si NW** via mechanical junction fabricated in **STEP 5**. Subsequently, a Si_3N_4 pulling strand is structured using **RIE** till reaching the dry SiO_2 sacrificial layer (**STEP 7**). The fabrication is completed by releasing the Si_3N_4 residual stress which is done in **STEP 8** where **BOX** is underetched using **HF** in vapor phase.

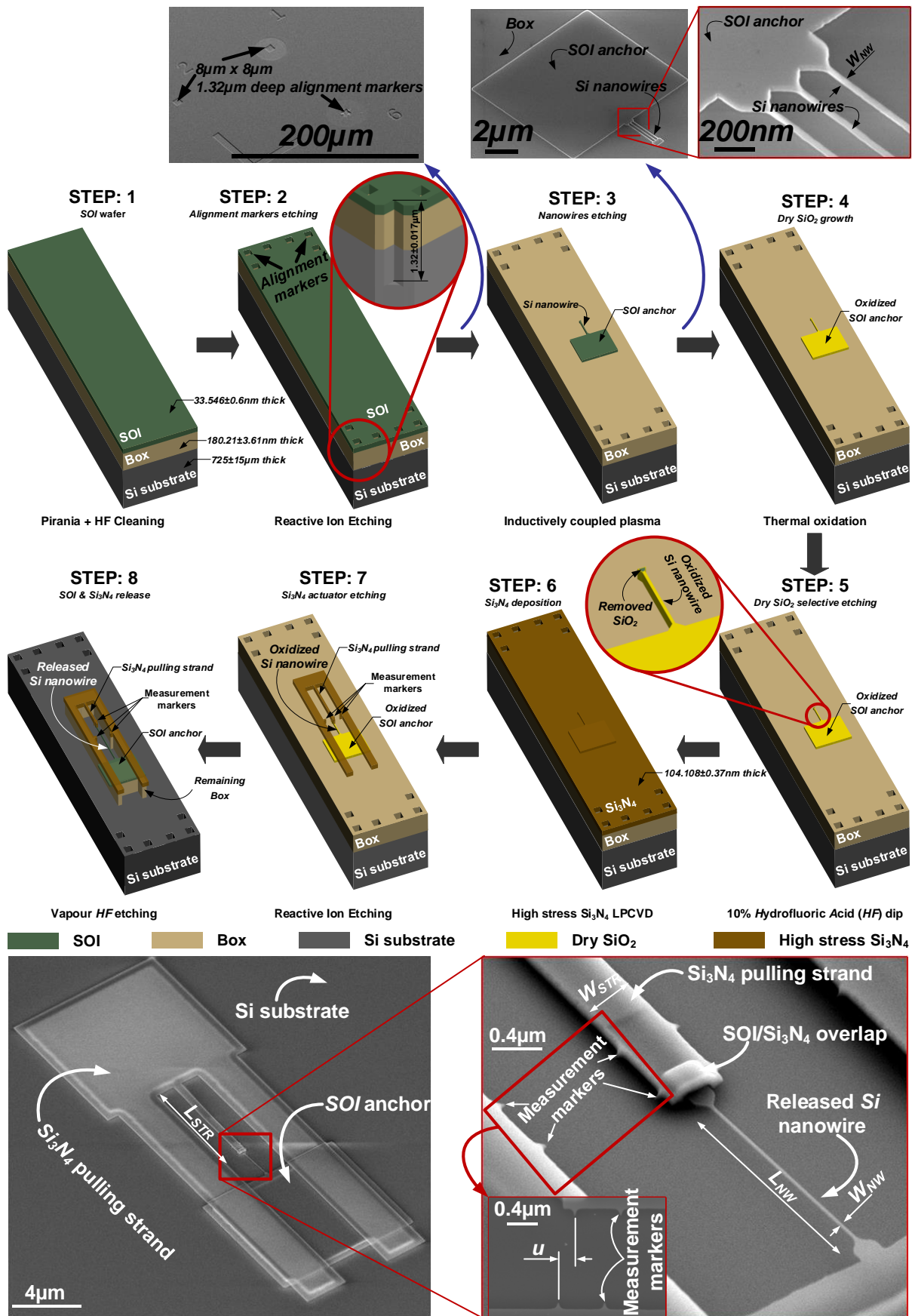


FIG. 5 Fabrication process flow of nanometer measurement platform for characterization of *Si* nanowires mechanical properties. Final device is presented in the SEM micrographs, inset presents the extension u of the nanowire when applied Si₃N₄ residual tensile stress.

RESULTS

Based on the measurement principle and physical implementation of the experimental platform described in the previous sections, the u is determined by evaluating the distance between the moving and fixed markers under **SEM** observation as illustrated in FIG. 5. The breakage mechanism of nanowires under mechanical tension can be induced by very slight process variations or by the presence of extended or point defects. Here, only unbroken nanowires were considered and the measurements are systematically accompanied by the number of nanowires that survived the mechanical stress.

a. ANALYTICAL MODELING

As a first approximation, the strain (ϵ) in the nanowire is given by the Eq. 1⁷² where L_{NW} is the initial length of the nanowire before application of the tensile force, i.e. before suspension.

$$\epsilon = \frac{u}{L_{NW}} \quad \text{Eq. 1}$$

The mechanical coupling between the nanowire and the **SiN** strand can be expressed theoretically by formulating the equilibrium condition of the forces exerted on these two elements.⁷³ The load condition expressed for the actuator is given by Eq. 2:

$$F_{STR} = E_{STR} \times S_{STR} \times \left(\epsilon_{STR}^m - \frac{u}{L_{STR}} \right) \quad \text{Eq. 2}$$

where E_{STR} is the Young modulus of the **Si₃N₄** strand while $S_{STR} = t_{STR} \times W_{STR}$ is the associated cross-sectional area. ϵ_{STR}^m refers to the mismatch strain between the **SiN** layer and the underlying **SOI** layer. This is the strain in the strand resulting from the mismatch stress in the **SiN** layer before its release by suspension. The difference $\left(\epsilon_{STR}^m - \frac{u}{L_{STR}} \right)$ therefore constitutes the residual strain that prevents the **SiN** strand from being totally relaxed because it is loaded by the **Si NW**. As a result, this strain difference is reflected in the load force F_{STR} exerted by the strand on the nanowire after suspension. Complementarily, the load condition expressed for the **Si NW** is given by Eq. 3:

$$F_{NW} = N \times E_{NW} \times S_{NW} \times \left(\frac{u}{L_{NW}} \right) \quad \text{Eq. 3}$$

where E_{NW} is the Young modulus of the **Si NW** oriented along the <110> direction, $S_{NW} = t_{NW} \times W_{NW}$ is the cross-sectional area of a unitary nanowire with t_{NW} and W_{NW} being its thickness and width, respectively. N is the number of nanowires attached to the **SiN** strand. In Eq. 3, we have assumed that no mismatch strain exists between the top **Si** layer and the **BOX** of the used **SOI** wafer, as already mentioned hereinbefore. By applying the equilibrium condition $F_{STR} = F_{NW}$, the u and the uniaxial strain ϵ_{NW} associated to the **Si NW** are expressed by Eq. 4 and Eq. 5, respectively⁷³:

$$u = \frac{\epsilon_{STR}^m}{N \times \frac{E_{NW} \times S_{NW}}{E_{STR} \times S_{STR}} \times \frac{1}{L_{NW}} + \frac{1}{L_{STR}}} \quad \text{Eq. 4}$$

$$\epsilon_{NW} = \frac{u}{L_{NW}} \quad \text{Eq. 5}$$

where L_{STR} is the length of the **SiN** strand before suspension. The above mechanical analysis, however, proves to be

simplistic in that some of the measured elongation takes place in the dumbbell connectors. To a lesser degree, some of this elongation also comes from the undercutting of the **BOX** in the anchor area. In order to better take into account these extrinsic contributions in solving the mechanical problem, the measurement platform is divided into two segments associated with the nanowire and the **SiN** strand respectively, as shown in the FIG. 6.

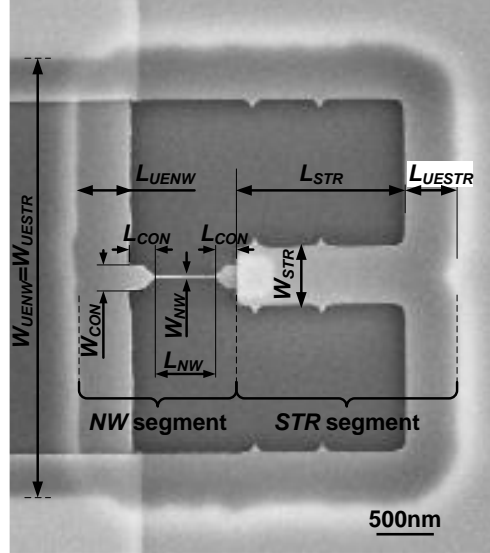


FIG. 6 SEM top view of the strain measurement platform showing the two segments associated to the nanowire (NW) and the SiN strand (STR). Characteristics dimensions used to account for extrinsic contributions due to BOX undercutting (L_{UENW} , W_{UENW} , L_{UESTR} , W_{UESTR}) and the relative impact of the dumbbell-shaped connections to nanowires (L_{CON} , W_{CON}) are detailed.

The nanowire segment can be divided into three parts including respectively (i) the underetched portion of the anchor area (L_{UENW} , W_{UENW} , t_{UENW}) (ii) the intrinsic nanowire (L_{NW} , W_{NW} , t_{NW}) and (iii) the dumbbell-shaped connectors (L_{CON} , W_{CON} , t_{CON}) as shown in FIG. 6. The three variables in parenthesis associated with each part represent the length, width and thickness of that part. It is worth noting here that $t_{NW}=t_{UENW}=t_{CON}=t_{SOI}$ is the thickness of the top layer of the **SOI** wafer. Complementarily, the **SiN** strand segment is composed of two parts, namely, the intrinsic strand (L_{STR} , W_{STR} , t_{STR}) and the under-etched portion of the anchor area (L_{UESTR} , W_{UESTR} , t_{UESTR}). Here, $t_{STR}=t_{UESTR}=t_{SiN}$ is the thickness of the **SiN** strand. Following the basic law of deformation summation in objects composed of parts of varying cross-sectional area, the elongation of the nanowire and strand segments can be expressed by Eq. 6 and Eq. 7, respectively, where $F=F_{NW}=F_{STR}$ represents the axial internal load applied to each segment:

$$u = \frac{F \times L_{NW}}{N \times E_{NW} \times S_{NW}} + \frac{F \times L_{UENW}}{N \times E_{UENW} \times S_{UENW}} + \frac{2 \times F \times L_{CON}}{N \times E_{CON} \times S_{CON}} =$$

$$= \frac{F}{E_{SOI} \times S_{SOI}} \times \left(L_{NW} + L_{UENW} \times \frac{W_{NW}}{W_{UENW}} + 2 \times L_{CON} \times \frac{W_{NW}}{W_{CON}} \right) = \frac{F}{E_{SOI} \times t_{SOI} \times W_{NW}} \times L_{NWEFF} \quad \text{Eq. 6}$$

$$u = \frac{F \times L_{STR}}{E_{STR} \times S_{STR}} + \frac{F \times L_{UESTR}}{E_{UESTR} \times S_{UESTR}} =$$

$$= \frac{F}{E_{SiN} \times S_{SiN}} \times \left(L_{STR} + L_{UESTR} \times \frac{W_{STR}}{W_{UESTR}} \right) = \frac{F}{E_{SiN} \times t_{SiN} \times W_{STR}} \times L_{STREFF} \quad \text{Eq. 7}$$

where $E_{SOI}=E_{NW}=E_{UENW}=E_{CON}$ is the Young modulus of **Si** in the $\langle 110 \rangle$ crystal direction and $E_{SiN}=E_{STR}=E_{UESTR}$ is the Young modulus of stoichiometric **Si₃N₄**. Inspection of the Eq. 6 and Eq. 7 yields the effective lengths L_{NWEFF} and L_{STREFF} for the nanowire and **SiN** strand, respectively. The two effective lengths

$$L_{NWEFF} = L_{NW} + L_{UENW} \times \left(\frac{W_{NW}}{W_{UENW}} \right) + 2 \times L_{CON} \times \left(\frac{W_{NW}}{W_{CON}} \right) \text{ and } L_{STREFF} = L_{STR} + L_{UESTR} \times \left(\frac{W_{STR}}{W_{UESTR}} \right)$$

can be substituted for L_{NW} and L_{STR} in the Eq. 4 and Eq. 5 to properly take into account the extrinsic extensions in the two segments depicted in FIG. 6. Given the position of the measurement markers, it is important to emphasize that the experimental strain, which will be discussed in the following, reflects that of the composite nanowire structure including the dumbbell-shaped connectors and the correction due to the **BOX** undercut. The experimental strain is therefore calculated based on the ratio between the measured elongation and L_{NWEFF} in Eq. 6. Naturally, the contributions from the extrinsic elements are more pronounced as the length of the nanowire is shorter. For the sake of completeness, the set of dimensional parameters used in the model developed hereinbefore is summarized in Table 1 and structural parameters are given in Table 2.

Table 1 Values of parameters used in theoretical modelling for all characterized lengths $L_{NW}=0.5, 2$ and $5\mu\text{m}$, number in brackets in underscore represent measurement population

L_{NW} (μm)	L_{STR} (μm)	Number of nanowires	W_{NW} (nm)	t_{SOI} t_{UENW} t_{CON} (nm)	W_{STR} (nm)	t_{SiN} t_{STR} t_{UESTR} (nm)	L_{CON} (nm)	W_{CON} (nm)	L_{UENW} L_{UESTR} (μm)	W_{UENW} W_{UESTR} (μm)
0.5 2 5	1 to 30 1 to 60 1 to 120	1	14.2±1.1 ₍₉₎	28.1±0.4 ₍₆₎	620	88.8±9.9 ₍₆₎	265	205	0.48	3.53
			18.2±1.0 ₍₁₃₎							
			38.8±1.5 ₍₂₀₎							
	3	15.9±1.6 ₍₇₈₎	25.6±0.6 ₍₁₀₎	1060	73.4±0.6 ₍₁₀₎	265	650			
		20.1±1.3 ₍₇₂₎								
		40.6±1.4 ₍₇₂₎								

Table 2 Mechanical parameters

Structural parameter	Variable name	Value	Unit
Silicon Young modulus <110> [59] [75]–[79]	$E_{SOI}=E_{NW}=E_{UENW}=E_{CON}$	165.8	GPa
Silicon Nitride Young modulus (Si_3N_4) [72] [73]	$E_{SiN}=E_{STR}=E_{UESTR}$	230	GPa
Silicon Nitride mismatch strain (measured)	\mathcal{E}_{STR}^m	0.0033	-

It is worth noting that the thickness of the nitride layer t_{SiN} differs for platforms with one or three nanowires, in triple nanowires platforms the nitride layer is ~21% thinner compared to single nanowire platform, as reported in Table 1. Despite that observation, both devices were fabricated on the same wafer and the thickness difference can be explained by the different etching durations at the end of fabrication process flow in **STEP 8** (see FIG. 5). Triple **Si** nanowires devices have wider Si_3N_4 tensile strands (*bigger* W_{STR}) than in single nanowires, thus the etching time in **STEP 8** is adequately extended for three wires platforms in order to achieve total **BOX** removal under the **SiN** tensile strand. The etch rate of 1-6nm/min of **SiN** in vapor **HF** is reported in the literature depending mainly on the etching temperature.^{91,92}

FIG. 7 and FIG. 8 compare experimental data with the theoretical model for measured **Si** nanowires in single and triple configurations as a function of the length **SiN** pulling strand. Note that L_{STREFF} is also substituted to L_{STR} on the horizontal axis in these figures but this correction only introduces a marginal shift given its magnitude. Markers stand for experimental data while continuous lines correspond to the theoretical model. Note that values of nanowires $W_{NW}=15, 20, 40$ nm are represented by colors: green, red and blue, respectively. In order to reduce the impact of the imprecision of the measurement method, a statistical representation of measured strain was used. Labels close to data points indicate the population of measured platforms.

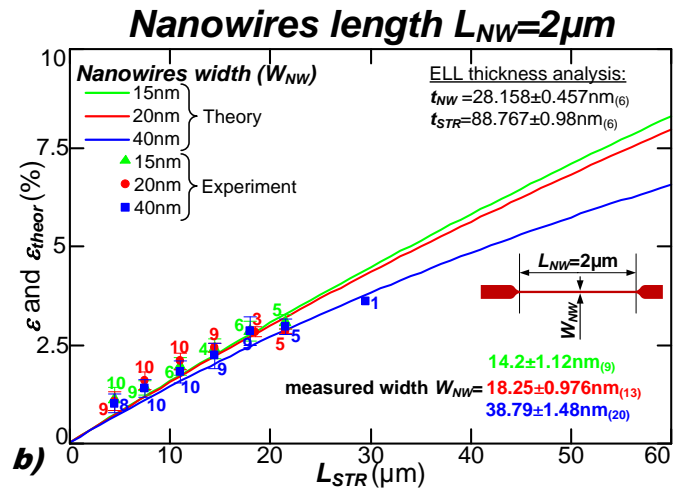
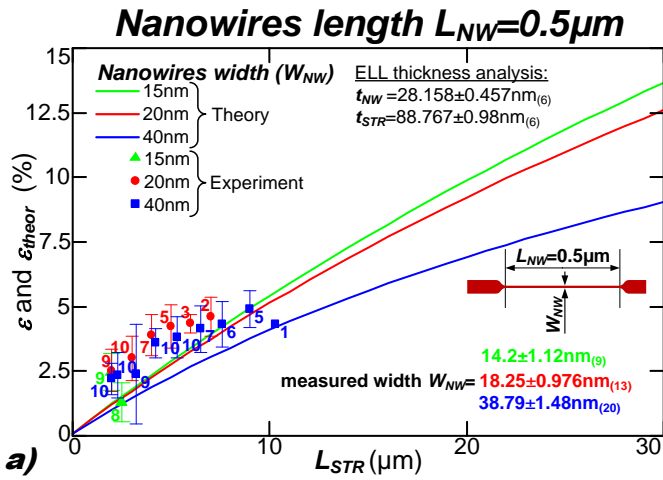
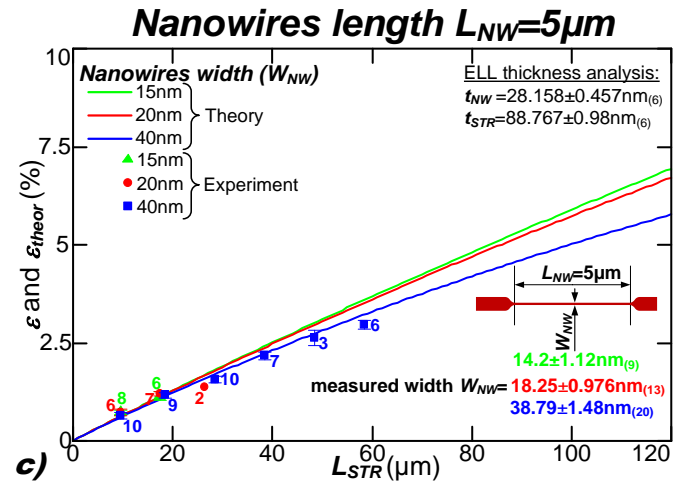


FIG. 7. Strain in single Si nanowire as a function of length of Si_3N_4 pulling strand for a) $L_{NW}=0.5\mu\text{m}$, b) $L_{NW}=2\mu\text{m}$ and c) $L_{NW}=5\mu\text{m}$. Experimental results (points) are taken for all platforms with unbroken wire. Continuous lines correspond to theoretical modelling. Blue, red and green colors are for nominal nanowire widths of $W_{NW}=40, 20, 15\text{nm}$, respectively. Labels close to t_{NW} , t_{STR} and W_{NW} values indicate the limited number of measurements used to calculate the average value of these parameters. Labels near datapoints represent population of successful measurements on unbroken nanowires. The ratio of unbroken to broken nanowires is easy to calculate considering that 10 specimens of each measurement platform were available from the 10 fabricated chips.



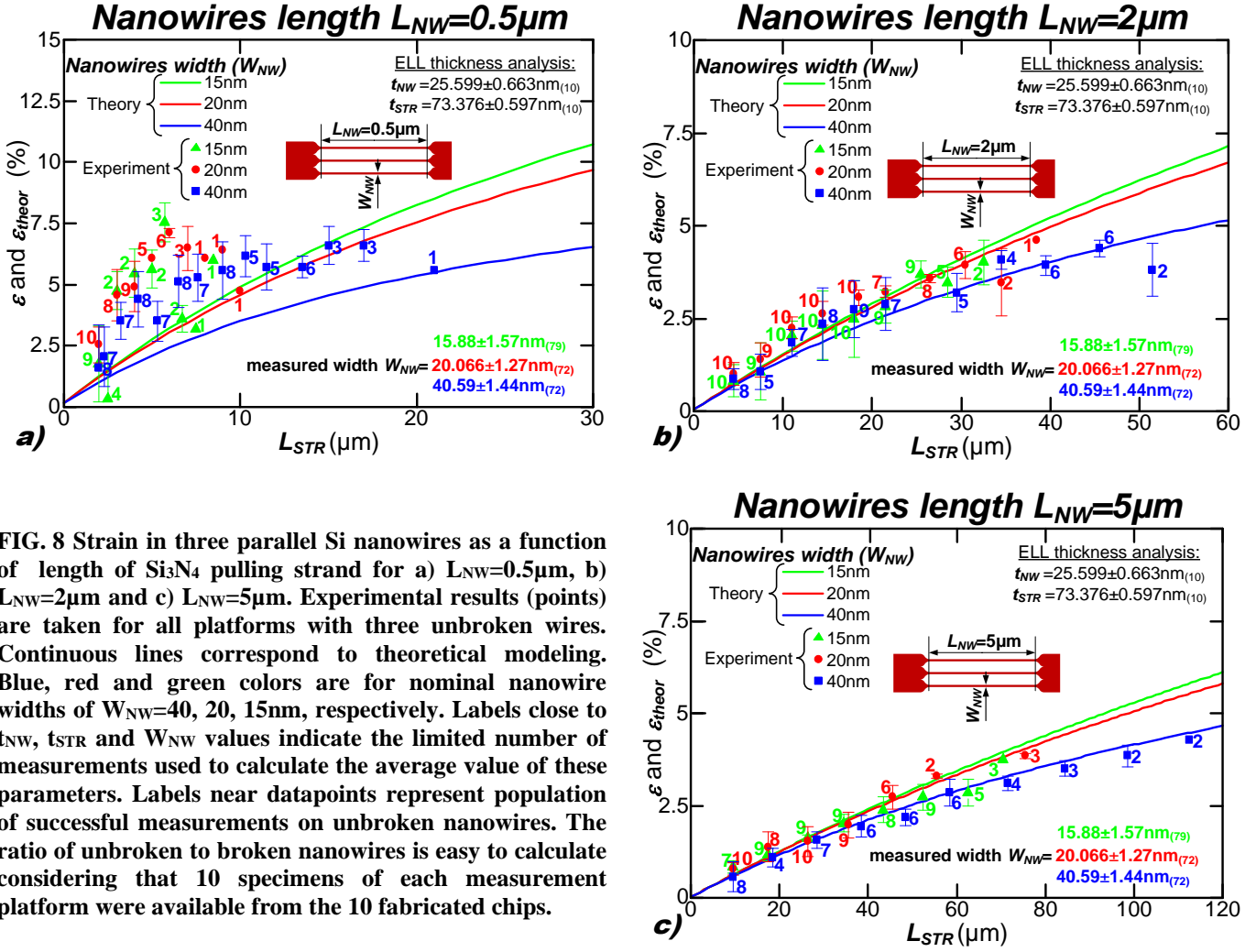


FIG. 8 Strain in three parallel Si nanowires as a function of length of Si_3N_4 pulling strand for a) $L_{NW}=0.5\mu\text{m}$, b) $L_{NW}=2\mu\text{m}$ and c) $L_{NW}=5\mu\text{m}$. Experimental results (points) are taken for all platforms with three unbroken wires. Continuous lines correspond to theoretical modeling. Blue, red and green colors are for nominal nanowire widths of $W_{NW}=40, 20, 15\text{nm}$, respectively. Labels close to t_{NW} , t_{STR} and W_{NW} values indicate the limited number of measurements used to calculate the average value of these parameters. Labels near datapoints represent population of successful measurements on unbroken nanowires. The ratio of unbroken to broken nanowires is easy to calculate considering that 10 specimens of each measurement platform were available from the 10 fabricated chips.

We report a maximum tensile strain of $4.9 \pm 0.7\%$ (*tensile strength* $8.28 \pm 1.18 \text{ GPa}$) for the single nanowire configuration and $7.53 \pm 0.8\%$ (*tensile strength* $12.73 \pm 1.35 \text{ GPa}$) for three nanowires in parallel. These strain values lead to the conclusion that nanowires, owing to their dimensionality, are significantly outperforming mechanical parameters of bulk *Si* (*fracture strain* of $0.18\text{-}0.6\%$ ^{93,94}). Comparing the results between single and three-nanowire configurations, it can be observed that three nanowires in parallel are extending the measurement range enabling characterization for longer L_{STR} . This is explained by the fact that three parallel nanowires are mechanically stronger and the Si_3N_4 pulling strand must be longer for the wires to reach the fracture point. The presented characterization method uses *SEM* measurements of *Si* nanowires elongation (u) probed between the measurement markers (*see FIG. 2a*) for graphical definition). The elongation readout is subjected to the error of the operator and the *SEM* image resolution. After error analysis (*see Supplementary Material for details*) the *SEM*-induced ϵ inaccuracy is between $\pm 0.223\%$ (for the shortest L_{NW}) and $\pm 0.0225\%$ (for the longest L_{NW}), and has minor impact on the characterization results.

To fairly compare the results depicted in FIG. 7 and FIG. 8 with those in the literature, the synthesis technique is an important comparative factor. In the literature, two *Si* nanowires fabrication techniques are the most popular: (i) Vapor-Liquid-Solid (*VLS*) growth or (ii) top-down etching. *VLS* technique produces very small nanowires with very pure and regular crystalline structure.^{75,79} However, *VLS*-grown *Si* *NW* cannot be used on industrial scale due to the fabrication technology and high cost related with it. In order to characterize mechanical properties of *Si* that is widely used in the semiconductor industry, a top-down technique must be used. This approach allows nanowires to be fabricated on the same wafers used industrially.

FIG. 9 benchmarks the ϵ of *Si* NW reported in the literature emphasizing their fabrication technology and width. Its analysis leads to the conclusion that this work presents the narrowest *Si* nanowires withstanding the highest strain among the top-down etched devices reported in the literature.

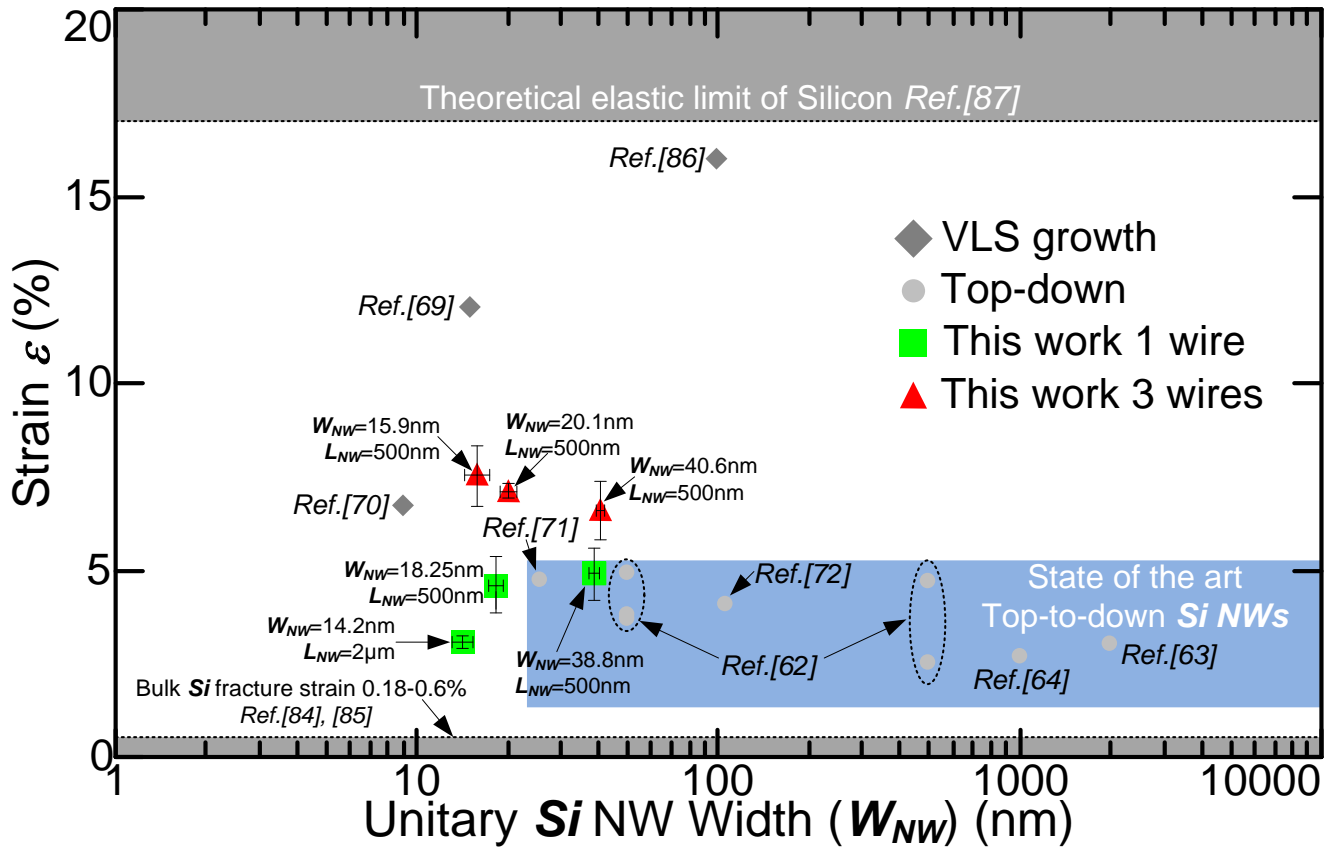


FIG. 9 Maximal supported strain versus width for *Si* nanowires reported in the literature emphasizing their fabrication technique (*VLS growth*^{75,78,79}; *top-down*^{71-73,80,81}) and highlighting theoretical elastic limit⁹⁵ and bulk fracture strain^{93,94}. Error bars are representing standard deviations for mean *Si* nanowires width (for *X-axis bar*) and strain (for *Y-axis bar*) taken from FIG. 7 and FIG. 8, respectively

b. FINITE ELEMENT METHOD MODELLING

The above described analytical model grasps the physics of the nanowire and strand deformation under the law of deformation summation in objects composed of different cross-sectional areas. This model thus describes the dumbbell connectors as parallelepipeds. However, the shape of these connectors is precisely aimed at avoiding abrupt transitions between the highly tensioned, small cross-section nanowire and the lowly tensioned large cross section strand and under etched parts. It could be argued that simplification explains the small remaining discrepancy between the model and the experiments, especially in the case of short nanowires $L_{NW}=0.5 \mu\text{m}$ as seen on Fig. 7a and 8a. More precisely, the dumbbell connector in this case could accommodate a greater fraction of the strain exerted by the *SiN* strand relatively to its actual length. To investigate this hypothesis, a series of *Finite Element Method (FEM)* simulations was performed on a selected subset of parameters. The measurement platform has been modelled using the material parameters, lengths, widths, thicknesses in accordance with the analytical model and using under etchings lengths (L_{UENW} and L_{UESTR}) and widths (W_{UENW} and W_{UESTR}) (see FIG. 6 for graphical definition) measured after fabrication. While *SEM* analysis allows for u measurements of entire the *Si NW* segment, thus integrating the displacement of dumbbell connectors, *FEM* modeling allows for a separate evaluation of the stress and deformation of all components of the *Si NW* and the *SiN* strand segments. FIG. 10a shows the u while FIG. 10b corresponds to the local deformation in the vicinity of the nanowire ($L_{NW}=0.5 \mu\text{m}$). The color maps reflect the local values of displacement

and deformation, respectively. As expected, the connection between the *Si NW* and *SiN* strand corresponds to the largest displacement. It is worth noting that the highest deformation occurs within the *Si NW* segment and that extrinsic contributions (*dumbbell connectors*, *SiN strand deformation*, etc.) are minor compared to the deformation occurring in the nanowire. The connectors shape plays its assigned role to ensure continuous transition of the deformation between the nanowire and external parts. FIG. 10c compares the results from the analytical model (*dark blue lines*) and *FEM* simulations. The strain evaluated by *FEM* has been split to show the total strain of the *NW* segment as measured in the experiment (*light blue lines*) and the sole contribution of the nanowire (*magenta lines*). It can be underlined that analytical and *FEM* modeling agree with good accuracy especially in the short *SiN* strand limit. The discrepancy in the long strand limit is attributed to an increasing out-of-plane deformation of the strand (*not depicted here*) which is neglected in the analytical model. We now compare the cases of short ($L_{NW}=0.5\ \mu\text{m}$) and longer ($L_{NW}=2\ \mu\text{m}$) nanowires on FIG. 10c. In the case of longer nanowires, the role of extrinsic parts is quite negligible as the strain in the nanowire is almost equal to the strain within the full *Si NW* segment. However, for the short ($L_{NW}=0.5\ \mu\text{m}$) wires, the fraction of strain supported by the dumbbell connectors is less negligible, especially for long strand sizes. The impossibility to separate those contributions during measurements can explain the better agreement of the analytical model with measurements in the $L_{NW}=2, 5\ \mu\text{m}$ cases.

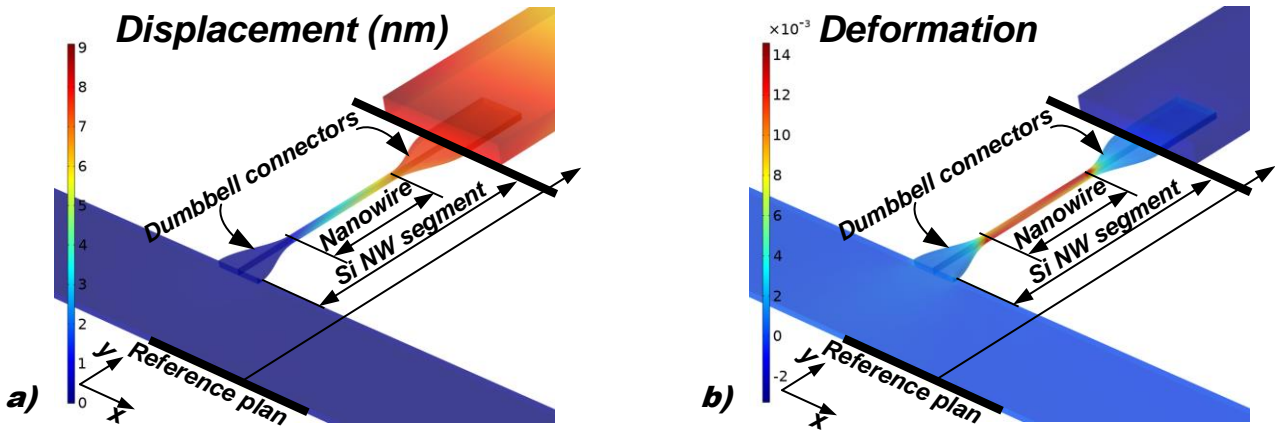
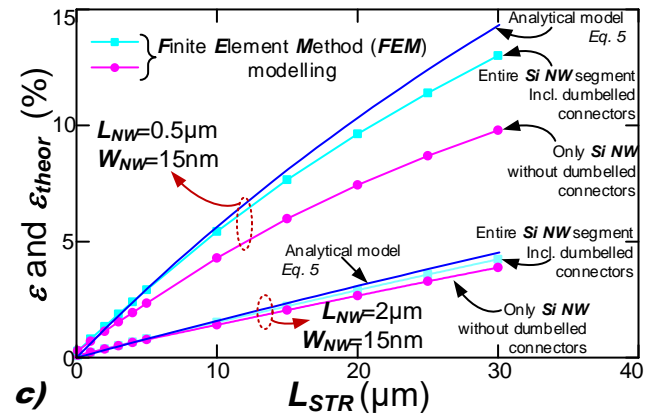


FIG. 10 Finite Element Method (FEM) modelling of uniaxially loaded *Si* nanowires: a) displacement (u) in nm the color map depicts the local displacement with respect to the reference plan, b) deformation results are revealing that the highest deformation occurs within the nanowire region and c) comparison of strain values obtained from analytical model (blue continuous line) and FEM simulations (• and •) for nanowires width $W_{NW}=15\text{nm}$ and two different lengths $L_{NW}=0.5\ \mu\text{m}$ and $2\ \mu\text{m}$, the strain of the sole nanowire segment is extracted (•).



CONCLUSIONS

In this paper, we have demonstrated the design, fabrication process, characterization and modeling of an integrated platform for measuring tensile strength in nanoscale *Si* nanowires. The novelty of our approach lies in the fact that a *Si₃N₄* residual tensile strain is applied to *Si* nanowires in a very wide range using strands of different lengths L_{STR} . The result is precise control of applied tensile stress which can be achieved by appropriate design. The fabrication process is fully *CMOS* compatible, with platforms processed in a top-down configuration which allows characterization of material identical to that in

industry. The tensile stress is released by dry etching with **HF** vapor, a technique that requires no mask while SiO_2/Si selectivity is naturally assured. The presented process approach enables the fabrication of nanowires with widths (W_{NW}) as small as $14.2 \pm 1.27 \text{ nm}$ and as short as 500 nm , which is comparable to the channel size of **MOSFETs** in the most advanced technology nodes.

Characterization of these devices is non-contact and non-invasive, based on u elongation measurements using a **SEM**. As a result, characterization is easy to perform and has minimal impact on the nanowires integrity. In addition, **SEM** characterization makes it easier to build up a statistical representation of the measured nanowire population.

At first glance FIG. 7 and FIG. 8 demonstrate the same trend for single and triple nanowire configurations. It can be observed that the agreement between theory and experiment is better for longer nanowires (higher L_{NW}), as explained in the FEM analysis. Moreover, the calculation of the strain associated with long nanowires is less prone to error due to smaller and therefore more sensitive displacement measurements. The second observation is that, while increasing L_{STR} , the population of measured nanowires is becoming smaller. This is obviously the result of an increase in the stress applied to the nanowires which increases the fracture probability. The third observation concerns the fact that, with increasing applied tensile strain using a longer strand (L_{STR}), nanowires begin to fail more rapidly when they have a smaller W_{NW} . A plausible hypothesis to explain the more fragile nature of narrow nanowires is that the volume/surface ratio is lower, resulting in a higher density of point defects which are at the origin of mechanical failure. At low dimensionality, Si increases dramatically its tensile strength. A strain of $\sim 4.5\%$ was reported in ⁸⁰ for 30 nm wide nanowires, 5% for 100 nm wide nanowires, ⁹⁶ 3.6% in $1 \mu\text{m}$ Si nanowires. ⁷² For the narrowest and the shortest nanowires, we report a strain of $7.53 \pm 0.8\%$ (*tensile strength* $12.73 \pm 1.35 \text{ GPa}$) for the triple-nanowire configuration and $4.9 \pm 0.7\%$ (*tensile strength* $8.28 \pm 1.18 \text{ GPa}$) for the single nanowire configuration, to date the highest figures achieved in a top-down fabrication approach. The presented topology and fabrication sequence enables, after optimization, to reach $W_{\text{NW}} \approx 10 \text{ nm}$ allowing strain characterization in the range of the theoretical elastic limit of Si , estimated at $17\text{-}20\%$. ⁹⁵

SUPPLEMENTARY MATERIAL

See supplementary material for more details on: (i) the characterization of the **SOI** wafer material stack thickness and uniformity at the initial stage of the device fabrication and (ii) the measurement error analysis.

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LICENSING

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REFERENCES

- ¹ J.N. Burghartz, editor, *Guide to State-of-the-Art Electron Devices* (John Wiley & Sons Inc, Chichester, West Sussex, United Kingdom, 2013).
- ² M. Segal, "Material history: Learning from silicon," *Nature* **483**(7389), S43–S44 (2012).
- ³ B. Lojek, *History of Semiconductor Engineering* (Springer-Verlag, Berlin Heidelberg, 2007).
- ⁴ F. Seitz, and N.G. Einspruch, *Electronic Genie: The Tangled History of Silicon* (University of Illinois Press, Urbana, 1998).
- ⁵ F. Seitz, and N.G. Einspruch, in *Encycl. Condens. Matter Phys.*, edited by F. Bassani, G.L. Liedl, and P. Wyder (Elsevier, Oxford, 2005), pp. 368–378.
- ⁶ D.H. Bailey, and J. Borwein, "Moore's Law is 50 years old but will it continue?," *The Conversation*, (2015).
- ⁷ C.A. Mack, "Fifty Years of Moore's Law," *IEEE Trans. Semicond. Manuf.* **24**(2), 202–207 (2011).
- ⁸ G.E. Moore, "Cramming more components onto integrated circuits," *Electronics* **38**(8), 114–117 (1965).
- ⁹ T. Skotnicki, C. Fenouillet-Beranger, C. Gallon, F. Boeuf, S. Monfray, F. Payet, A. Pouydebasque, M. Szczap, A. Farcy, F. Arnaud, S. Clerc, M. Sellier, A. Cathignol, J.-P. Schoellkopf, E. Perea, R. Ferrant, and H. Mingam, "Innovative Materials, Devices, and CMOS Technologies for Low-Power Mobile Multimedia," *IEEE Trans. Electron Devices* **55**(1), 96–130 (2008).
- ¹⁰ G.Q. Zhang, and A.J. van Roosmalen, editors, *More than Moore: Creating High Value Micro/Nanoelectronics Systems* (Springer, Dordrecht ; New York, 2009).
- ¹¹ G.Q. Zhang, F. van Roosmalen, and M. Graef, in *6supthsup Int. Conf. Electron. Packag. Technol. ICEPT* (IEEE, Shenzhen, China, 2005), pp. 17–24.
- ¹² International Roadmap for Devices and Systems (IRDS™), *More Moore - Table MM01 Logic Core Device Technology Roadmap* (2020).
- ¹³ F. Schwierz, "Graphene transistors," *Nat. Nanotechnol.* **5**(7), 487–496 (2010).
- ¹⁴ International Technology Roadmap for Semiconductors (ITRS™), *More Moore - Table MM01 Logic Core Device Technology Roadmap* (2015).
- ¹⁵ K. Rupp, "42 Years of Microprocessor Trend Data," (2018).
- ¹⁶ VLSI research, "Is it time for a revolution?," *VLSI Res.*, (n.d.).
- ¹⁷ R.K. Cavin, P. Lugli, and V.V. Zhimov, "Science and Engineering Beyond Moore's Law," *Proc. IEEE* **100**(Special Centennial Issue), 1720–1749 (2012).
- ¹⁸ G. Frantz, "Digital signal processor trends," *IEEE Micro* **20**(6), 52–59 (2000).
- ¹⁹ M.A. Richards, and G.A. Shaw, "Chips, Architectures and Algorithms: Reflections on the Exponential Growth of Digital Signal Processing Capability," (2004).
- ²⁰ E.R. Berndt, and N.J. Rappaport, "Price and Quality of Desktop and Mobile Personal Computers: A Quarter-Century Historical Overview," *Am. Econ. Rev.* **91**(2), 268–273 (2001).
- ²¹ International Technology Roadmap for Semiconductors (ITRS™), *On-Chip Local Clock in Table 4c: Performance and Package Chips: Frequency On-Chip Wiring Levels—Near-Term Years* (2002), p. 12.
- ²² International Technology Roadmap for Semiconductors (ITRS™), *Table ORTC-4 Performance and Packaged Chips Trends* (2013), p. 12.
- ²³ International Technology Roadmap for Semiconductors (ITRS™), *Table ORTC-1 ITRS Technology Trend Targets 2013-2028* (2014), p. 12.
- ²⁴ International Roadmap for Devices and Systems (IRDS™), *More Moore - Table MM01 Logic Core Device Technology Roadmap* (2022).
- ²⁵ J.-K. Yu, S. Mitrovic, D. Tham, J. Varghese, and J.R. Heath, "Reduction of thermal conductivity in phononic nanomesh structures," *Nat. Nanotechnol.* **5**(10), 718–721 (2010).
- ²⁶ M. Haras, V. Lacatena, F. Morini, J.-F. Robillard, S. Monfray, T. Skotnicki, and E. Dubois, in *Tech. Dig. - Int. Electron Devices Meet. IEDM* (IEEE, San Francisco, California, 2014), p. 8.5.212-8.5.215.
- ²⁷ A.I. Hochbaum, R. Chen, R.D. Delgado, W. Liang, E.C. Garnett, M. Najarian, A. Majumdar, and P. Yang, "Enhanced thermoelectric performance of rough silicon nanowires," *Nature* **451**(7175), 163–167 (2008).
- ²⁸ K.F. Murphy, B. Piccione, M.B. Zanjani, J.R. Lukes, and D.S. Gianola, "Strain- and Defect-Mediated Thermal Conductivity in Silicon Nanowires," *Nano Lett.* **14**(7), 3785–3792 (2014).
- ²⁹ A.M. Massoud, V. Lacatena, M. Haras, E. Dubois, S. Monfray, J.-M. Bluet, P.-O. Chapuis, and J.-F. Robillard, "Heat dissipation in partially perforated phononic nano-membranes with periodicities below 100 nm," *APL Mater.* **10**(5), 051113 (2022).
- ³⁰ Z. Wu, J.B. Neaton, and J.C. Grossman, "Charge Separation via Strain in Silicon Nanowires," *Nano Lett.* **9**(6), 2418–2422 (2009).
- ³¹ R. Sen, N. Vast, and J. Sjakste, "Hot electron relaxation and energy loss rate in silicon: Temperature dependence and main scattering channels," *Appl. Phys. Lett.* **120**(8), 082101 (2022).
- ³² M. Cazzanelli, F. Bianco, E. Borga, G. Pucker, M. Ghulinyan, E. Degoli, E. Luppi, V. Véniard, S. Ossicini, D. Modotto, S. Wabnitz, R. Pierobon, and L. Pavesi, "Second-harmonic generation in silicon waveguides strained by silicon nitride," *Nat. Mater.* **11**(2), 148–154 (2012).
- ³³ R.S. Jacobsen, K.N. Andersen, P.I. Borel, J. Fage-Pedersen, L.H. Frandsen, O. Hansen, M. Kristensen, A.V. Lavrinenko, G. Moulin, H. Ou, C. Peucheret, B. Zsigri, and A. Bjarklev, "Strained silicon as a new electro-optic material," *Nature* **441**(7090), 199–202 (2006).
- ³⁴ N. Healy, S. Mailis, N.M. Bulgakova, P.J.A. Sazio, T.D. Day, J.R. Sparks, H.Y. Cheng, J.V. Badding, and A.C. Peacock, "Extreme electronic bandgap modification in laser-crystallized silicon optical fibres," *Nat. Mater.* **13**(12), 1122–1127 (2014).

- ³⁵ H. Wang, J. Guo, J. Miao, W. Luo, Y. Gu, R. Xie, F. Wang, L. Zhang, P. Wang, and W. Hu, "Emerging Single-Photon Detectors Based on Low-Dimensional Materials," *Small* **18**(5), 2103963 (2022).
- ³⁶ A. Tarun, N. Hayazawa, H. Ishitobi, S. Kawata, M. Reiche, and O. Moutanabbir, "Mapping the 'Forbidden' Transverse-Optical Phonon in Single Strained Silicon (100) Nanowire," *Nano Lett.* **11**(11), 4780–4788 (2011).
- ³⁷ D. Heydari, M. Cătuneanu, E. Ng, D.J. Gray, R. Hamerly, J. Mishra, M. Jankowski, M.M. Fejer, K. Jamshidi, and H. Mabuchi, "Degenerate optical parametric amplification in CMOS silicon," *Optica* **10**(4), 430–437 (2023).
- ³⁸ K. Uchida, A. Kinoshita, and M. Saitoh, in *Tech. Dig. - Int. Electron Devices Meet. IEDM* (IEEE, San Francisco, California, 2006), pp. 1–3.
- ³⁹ K. Uchida, and M. Saitoh, in *Dig. Tech. Pap. Symp. VLSI Technol.* (IEEE, 2009), pp. 6–7.
- ⁴⁰ F. Gamiz, A. Godoy, and C. Sampedro, in *Proc. SPIE 6591 Nanotechnol. III* (Society of Photo-Optical Instrumentation Engineers (SPIE), Maspalomas, Gran Canaria, Spain, 2007), pp. 65910C-65910C–9.
- ⁴¹ D. Shiri, Y. Kong, A. Buin, and M.P. Anantram, "Strain induced change of bandgap and effective mass in silicon nanowires," *Appl. Phys. Lett.* **93**(7), 073114 (2008).
- ⁴² Y.-M. Niquet, C. Delerue, and C. Krzeminski, "Effects of Strain on the Carrier Mobility in Silicon Nanowires," *Nano Lett.* **12**(7), 3545–3550 (2012).
- ⁴³ V.-H. Nguyen, F. Triozon, F.D.R. Bonnet, and Y.-M. Niquet, "Performances of Strained Nanowire Devices: Ballistic Versus Scattering-Limited Currents," *IEEE Trans. Electron Devices* **60**(5), 1506–1513 (2013).
- ⁴⁴ R.A. Minamisawa, S. Habicht, D. Buca, R. Carius, S. Trellenkamp, K.K. Bourdelle, and S. Mantl, "Elastic strain and dopant activation in ion implanted strained Si nanowires," *J. Appl. Phys.* **108**(12), 124908 (2010).
- ⁴⁵ M. Jeong, B. Doris, J. Kedzierski, K. Rim, and M. Yang, "Silicon Device Scaling to the Sub-10-nm Regime," *Science* **306**(5704), 2057–2060 (2004).
- ⁴⁶ S. Takagi, T. Iisawa, T. Tezuka, T. Numata, S. Nakaharai, N. Hirashita, Y. Moriyama, K. Usuda, E. Toyoda, S. Dissanayake, M. Shichijo, R. Nakane, S. Sugahara, M. Takenaka, and N. Sugiyama, "Carrier-Transport-Enhanced Channel CMOS for Improved Power Consumption and Performance," *IEEE Trans. Electron Devices* **55**(1), 21–39 (2008).
- ⁴⁷ M.V. Fischetti, and S.E. Laux, "Band structure, deformation potentials, and carrier mobility in strained Si, Ge, and SiGe alloys," *J. Appl. Phys.* **80**(4), 2234–2252 (1996).
- ⁴⁸ A. Lisauskas, K. Ikamas, S. Massabeau, M. Bauer, D. Čibiraitė, J. Matukas, J. Mangeney, M. Mittendorff, S. Winnerl, V. Krozer, and H.G. Roskos, "Field-effect transistors as electrically controllable nonlinear rectifiers for the characterization of terahertz pulses," *APL Photonics* **3**(5), 051705 (2018).
- ⁴⁹ K. Ikamas, D. Čibiraitė, A. Lisauskas, M. Bauer, V. Krozer, and H.G. Roskos, "Broadband Terahertz Power Detectors Based on 90-nm Silicon CMOS Transistors With Flat Responsivity Up to 2.2 THz," *IEEE Electron Device Lett.* **39**(9), 1413–1416 (2018).
- ⁵⁰ W. Knap, F. Teppe, Y. Meziani, N. Dyakonova, J. Lusakowski, F. Boeuf, T. Skotnicki, D. Maude, S. Romyantsev, and M.S. Shur, "Plasma wave detection of sub-terahertz and terahertz radiation by silicon field-effect transistors," *Appl. Phys. Lett.* **85**(4), 675–677 (2004).
- ⁵¹ R. Tauk, F. Teppe, S. Boubanga, D. Coquillat, W. Knap, Y.M. Meziani, C. Gallon, F. Boeuf, T. Skotnicki, C. Fenouillet-Beranger, D.K. Maude, S. Romyantsev, and M.S. Shur, "Plasma wave detection of terahertz radiation by silicon field effects transistors: Responsivity and noise equivalent power," *Appl. Phys. Lett.* **89**(25), 253511 (2006).
- ⁵² A. Varpula, K. Grigoros, K. Tappura, A.V. Timofeev, A. Shchepetov, J. Hassel, J. Ahopelto, and M. Prunnila, "Silicon Based Nano-Thermoelectric Bolometers for Infrared Detection," *Proceedings* **2**(13), 894 (2018).
- ⁵³ A. Varpula, A.V. Timofeev, A. Shchepetov, K. Grigoros, J. Ahopelto, and M. Prunnila, in edited by L. Fonseca, M. Prunnila, and E. Peiner (SPIE Press, Barcelona, Spain, 2017), p. 102460L.
- ⁵⁴ K. Tani, K. Oda, M. Deura, and T. Ido, "Enhanced room-temperature electroluminescence from a germanium waveguide on a silicon-on-insulator diode with a silicon nitride stressor," *Opt. Express* **29**(3), 3584–3595 (2021).
- ⁵⁵ S.W. Bedell, A. Khakifirooz, and D.K. Sadana, "Strain scaling for CMOS," *MRS Bull.* **39**(2), 131–137 (2014).
- ⁵⁶ H.M. Manasevit, I.S. Gergis, and A.B. Jones, "Electron mobility enhancement in epitaxial multilayer Si-Si_{1-x}Ge_x alloy films on (100) Si," *Appl. Phys. Lett.* **41**(5), 464–466 (1982).
- ⁵⁷ T. Ghani, M. Armstrong, C. Auth, M. Bost, P. Charvat, G. Glass, T. Hoffmann, K. Johnson, C. Kenyon, J. Klaus, B. McIntyre, K. Mistry, A. Murthy, J. Sandford, M. Silberstein, S. Sivakumar, P. Smith, K. Zawadzki, S. Thompson, and M. Bohr, in *Tech. Dig. - Int. Electron Devices Meet. IEDM* (IEEE, Washington DC, United States, 2003), p. 11.6.1-11.6.3.
- ⁵⁸ X. Yu, Y. Wang, H. Zhou, Y. Liu, Y. Wang, T. Li, and Y. Wang, "Top-Down Fabricated Silicon-Nanowire-Based Field-Effect Transistor Device on a (111) Silicon Wafer," *Small* **9**(4), 525–530 (2013).
- ⁵⁹ K.-N. Lee, S.-W. Jung, K.-S. Shin, W.-H. Kim, M.-H. Lee, and W.-K. Seong, "Fabrication of Suspended Silicon Nanowire Arrays," *Small* **4**(5), 642–648 (2008).
- ⁶⁰ T. Maurer, J. Marae-Djouda, U. Cataldi, A. Gontier, G. Montay, Y. Madi, B. Panicaut, D. Macias, P.-M. Adam, G. Lévêque, T. Bürgi, and R. Caputo, "The beginnings of plasmomechanics: towards plasmonic strain sensors," *Front. Mater. Sci.* **9**(2), 170–177 (2015).
- ⁶¹ U. Celano, and N. Maccaferri, "Chasing Plasmons in Flatland," *Nano Lett.* **19**(11), 7549–7552 (2019).
- ⁶² D. Dahal, G. Gumbs, and D. Huang, "Effect of strain on plasmons, screening, and energy loss in graphene/substrate contacts," *Phys. Rev. B* **98**(4), 045427 (2018).
- ⁶³ Z. Ma, Z. Chen, J. Xu, W. Li, L. Zhang, and L. Wang, "Investigation of a new graphene strain sensor based on surface plasmon resonance," *Sci. Rep.* **10**(1), 16870 (2020).
- ⁶⁴ M. Chu, Y. Sun, U. Aghoram, and S.E. Thompson, "Strain: A Solution for Higher Carrier Mobility in Nanoscale MOSFETs," *Annu. Rev. Mater. Res.* **39**(1), 203–229 (2009).

- ⁶⁵ W. Wu, G. Yang, Y. Wang, L. Zhang, S. Liu, J. Zhu, and W. Sun, "Experimental Investigation on the Electrical Properties of Lateral IGBT Under Mechanical Strain," *IEEE Electron Device Lett.* **40**(6), 937–940 (2019).
- ⁶⁶ S.E. Thompson, M. Armstrong, C. Auth, S. Cea, R. Chau, G. Glass, T. Hoffman, J. Klaus, Z. Ma, B. McIntyre, A. Murthy, B. Obradovic, L. Shifren, S. Sivakumar, S. Tyagi, T. Ghani, K. Mistry, M. Bohr, and Y. El-Mansy, "A logic nanotechnology featuring strained-silicon," *IEEE Electron Device Lett.* **25**(4), 191–193 (2004).
- ⁶⁷ H. Wen, D. Borlaug, H. Wang, Y. Ji, and B. Jalali, "Engineering Strain in Silicon Using SIMOX 3-D Sculpting," *IEEE Photonics J.* **8**(2), 1–9 (2016).
- ⁶⁸ R.A. Bernal, T. Filleter, J.G. Connell, K. Sohn, J. Huang, L.J. Lauhon, and H.D. Espinosa, "In Situ Electron Microscopy Four-Point Electromechanical Characterization of Freestanding Metallic and Semiconducting Nanowires," *Small* **10**(4), 725–733 (2014).
- ⁶⁹ C. Auth, C. Allen, A. Blattner, D. Bergstrom, M. Brazier, M. Bost, M. Buehler, V. Chikarmane, T. Ghani, T. Glassman, R. Grover, W. Han, D. Hanken, M. Hattendorf, P. Hentges, R. Heussner, J. Hicks, D. Ingerly, P. Jain, S. Jaloviar, R. James, D. Jones, J. Jopling, S. Joshi, C. Kenyon, H. Liu, R. McFadden, B. McIntyre, J. Neiryneck, C. Parker, L. Pipes, I. Post, S. Pradhan, M. Prince, S. Ramey, T. Reynolds, J. Roesler, J. Sandford, J. Seiple, P. Smith, C. Thomas, D. Towner, T. Troeger, C. Weber, P. Yashar, K. Zawadzki, and K. Mistry, in *2012 Symp. VLSI Technol. VLSIT* (IEEE, Honolulu, HI, USA, 2012), pp. 131–132.
- ⁷⁰ U.S. Geological Survey, *Mineral Commodities Summary 2021* (U.S. Government printing office, Reston, Virginia, 2021).
- ⁷¹ V. Passi, U. Bhaskar, T. Pardoen, U. Sodervall, B. Nilsson, G. Petersson, M. Hagberg, and J.P. Raskin, "High-throughput on-chip large deformation of silicon nanoribbons and nanowires," *J. Microelectromechanical Syst.* **21**(4), 822–829 (2012).
- ⁷² F. Ureña, S.H. Olsen, L. Šiller, U. Bhaskar, T. Pardoen, and J.-P. Raskin, "Strain in silicon nanowire beams," *J. Appl. Phys.* **112**(11), 114506 (2012).
- ⁷³ F. Ureña, S.H. Olsen, and J.-P. Raskin, "Raman measurements of uniaxial strain in silicon nanostructures," *J. Appl. Phys.* **114**(14), 144507 (2013).
- ⁷⁴ A. Tarun, N. Hayazawa, M.V. Balois, S. Kawata, M. Reiche, and O. Moutanabbir, "Stress redistribution in individual ultrathin strained silicon nanowires: a high-resolution polarized Raman study," *New J. Phys.* **15**(5), 053042 (2013).
- ⁷⁵ H. Zhang, J. Tersoff, S. Xu, H. Chen, Q. Zhang, K. Zhang, Y. Yang, C.-S. Lee, K.-N. Tu, J. Li, and Y. Lu, "Approaching the ideal elastic strain limit in silicon nanowires," *Sci. Adv.* **2**(8), e1501382 (2016).
- ⁷⁶ C.Y. Tang, L.C. Zhang, and K. Mylvaganam, "Mechanical Properties of a Silicon Nano-Wire Under Uni-Axial Tension and Compression," *J. Comput. Theor. Nanosci.* **7**(10), 2135–2143 (2010).
- ⁷⁷ M.N. Esfahani, and B.E. Alaca, "A Review on Size-Dependent Mechanical Properties of Nanowires," *Adv. Eng. Mater.* **21**(8), 1900192 (2019).
- ⁷⁸ Y. Zhu, F. Xu, Q. Qin, W.Y. Fung, and W. Lu, "Mechanical Properties of Vapor-Liquid-Solid Synthesized Silicon Nanowires," *Nano Lett.* **9**(11), 3934–3939 (2009).
- ⁷⁹ D.-M. Tang, C.-L. Ren, M.-S. Wang, X. Wei, N. Kawamoto, C. Liu, Y. Bando, M. Mitome, N. Fukata, and D. Golberg, "Mechanical Properties of Si Nanowires as Revealed by in Situ Transmission Electron Microscopy and Molecular Dynamics Simulations," *Nano Lett.* **12**(4), 1898–1904 (2012).
- ⁸⁰ R.A. Minamisawa, M.J. Süess, R. Spolenak, J. Faist, C. David, J. Gobrecht, K.K. Bourdelle, and H. Sigg, "Top-down fabricated silicon nanowires under tensile elastic strain up to 4.5%," *Nat. Commun.* **3**, 1096 (2012).
- ⁸¹ T. Tsuchiya, T. Hemmi, J. Suzuki, Y. Hirai, and O. Tabata, "Tensile Strength of Silicon Nanowires Batch-Fabricated into Electrostatic MEMS Testing Device," *Appl. Sci.* **8**(6), 880 (2018).
- ⁸² H. Ftouni, C. Blanc, D. Tainoff, A.D. Fefferman, M. Defoort, K.J. Lulla, J. Richard, E. Collin, and O. Bourgeois, "Thermal conductivity of silicon nitride membranes is not sensitive to stress," *Phys. Rev. B* **92**(12), 125439 (2015).
- ⁸³ E.A. Irene, "Residual stress in silicon nitride films," *J. Electron. Mater.* **5**(3), 287–298 (1976).
- ⁸⁴ V. Passi, E. Dubois, A. Lecestre, A.S. Linde, B.D. Bois, and J.-P. Raskin, "Design guidelines for releasing silicon nanowire arrays by liquid and vapor phase hydrofluoric acid," *Microelectron. Eng.* **103**, 57–65 (2013).
- ⁸⁵ O. Tabata, K. Kawahata, S. Sugiyama, and I. Igarashi, "Mechanical property measurements of thin films using load-deflection of composite rectangular membranes," *Sens. Actuators* **20**(1), 135–141 (1989).
- ⁸⁶ M.A. Hopcroft, W.D. Nix, and T.W. Kenny, "What is the Young's Modulus of Silicon?," *J. Microelectromechanical Syst.* **19**(2), 229–238 (2010).
- ⁸⁷ T. Yi, L. Li, and C.-J. Kim, "Microscale material testing of single crystalline silicon: process effects on surface morphology and tensile strength," *Sens. Actuators Phys.* **83**(1), 172–178 (2000).
- ⁸⁸ Y.-S. Sohn, J. Park, G. Yoon, J. Song, S.-W. Jee, J.-H. Lee, S. Na, T. Kwon, and K. Eom, "Mechanical Properties of Silicon Nanowires," *Nanoscale Res. Lett.* **5**(1), 211–216 (2010).
- ⁸⁹ W.A. Brantley, "Calculated elastic constants for stress problems associated with semiconductor devices," *J. Appl. Phys.* **44**(1), 534–535 (1973).
- ⁹⁰ C.J. Wilson, and P.A. Beck, "Fracture testing of bulk silicon microcantilever beams subjected to a side load," *J. Microelectromechanical Syst.* **5**(3), 142–150 (1996).
- ⁹¹ K.R. Williams, K. Gupta, and M. Wasilik, "Etch rates for micromachining processing-Part II," *J. Microelectromechanical Syst.* **12**(6), 761–778 (2003).
- ⁹² S. Guillemin, P. Mumbauer, H. Radtke, M. Fimberger, S. Fink, J. Kraxner, A. Faes, and J. Siegert, "Etching Mechanisms of SiO₂ and SiN_x:H Thin Films in HF/Ethanol Vapor Phase: Toward High Selectivity Batch Release Processes," *J. Microelectromechanical Syst.* **28**(4), 717–723 (2019).
- ⁹³ D.Y.R. Chong, W.E. Lee, B.K. Lim, J.H.L. Pang, and T.H. Low, in *Ninth Intersoc. Conf. Therm. Thermomechanical Phenom. Electron. Syst.* (IEEE, Las Vegas, NV, USA, 2004), pp. 203-210 Vol.2.
- ⁹⁴ Y. Chen, and X. Liao, in *Semicond. Semimet.*, edited by S.A. Dayeh, A. Fontcuberta i Morral, and C. Jagadish (Elsevier, 2016), pp. 109–158.
- ⁹⁵ D. Roundy, and M.L. Cohen, "Ideal strength of diamond, Si, and Ge," *Phys. Rev. B* **64**(21), 212103 (2001).

⁹⁶ E.M. Grumstrup, M.M. Gabriel, C.W. Pinion, J.K. Parker, J.F. Cahoon, and J.M. Papanikolas, "Reversible Strain-Induced Electron–Hole Recombination in Silicon Nanowires Observed with Femtosecond Pump–Probe Microscopy," *Nano Lett.* **14**(11), 6287–6292 (2014).