Towards Low-Power and Low Data-Rate Software-Defined Radio Baseband with RISC-V Processor for Flexibility and Security

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Abstract

This work discusses opportunities and challenges of using Software Defined Radio (SDR) in baseband processor architectures dedicated to IoT end-devices.
It highlights some important features that are still missing to build flexible, secure and low-power SDR processors for IoT end-devices using Sub-GHz low data rate protocols.

SDR baseband architectures related work

This table presents a comparison of IoT SDR baseband processor architectures and their features:

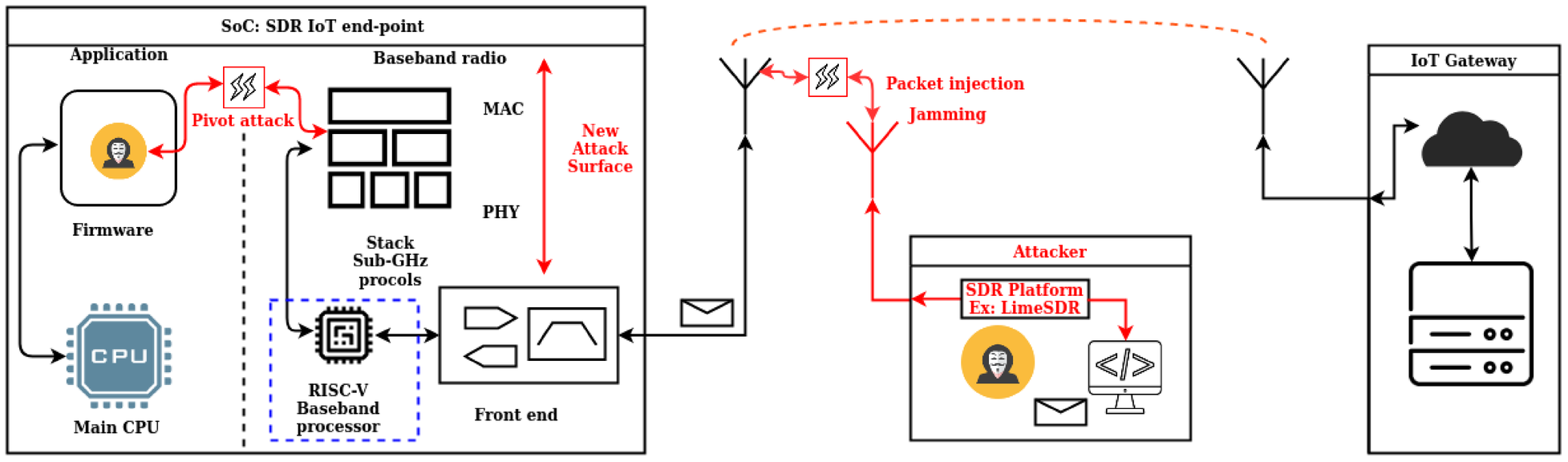
Architecture	Hybrid FPGA [1]	CPU (dedicated) [2]	CPU (Generic) [3]	ARM cortex M0+
Multi-Protocol operation	✗	✗	✗	✗
Programmability	+	+	+++	+++
Security	✗	✗	✗	✓
Flexibility	+++	+	++	++
Dynamic power	$\sim 100mW$	$\sim 10mW$	$\sim 10\mu W$	$\sim 10\mu W$

State of the art regarding security

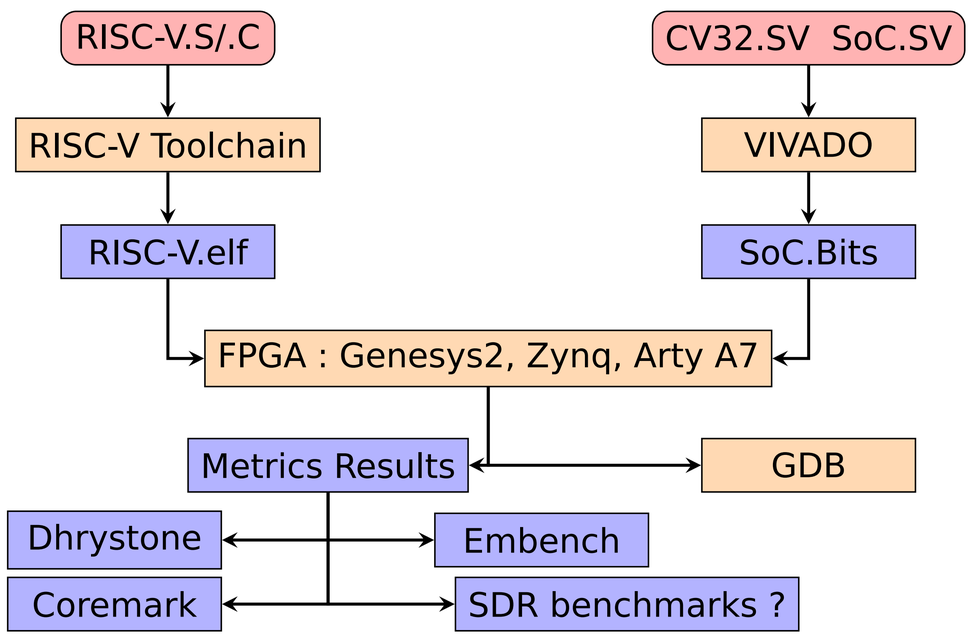
- The emergence of low-cost high-performance platforms and associated software allows attackers to access lower layers of networks [4]
- 33 vulnerabilities in TCP/IP stacks which allows to perform code execution, DoS, and data ex-filtration [5]
- Exploitation of buffer overflow vulnerabilities to perform DoS attacks and remote execution of malware on the target [6]
- Wazabee: Transmitting and receiving 802.15.4 frames, including Zigbee, from a chip supporting only Bluetooth Low Energy (BLE) [7]

Potential threat models

- Jamming Attack ✓
- Logical Attacks: Packet Injection, . . . ✓
- Physical Attacks ✗



Workflow of performance evaluation



Security Mechanisms

- Compilation & run-time levels
- Memory protection and isolation
- Intrusion detection
- Over the air (OTA) programming

Conclusion and perspective work

- CV32E40P RISC-V Processor instruction set extension
- Support DSP performance and Security mechanisms for sub-GHz Protocols
- Reproduction of the authors' work of DSP instructions [3]
- Performance rating (SDR and security benchmarks)

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