Towards Low-Power and Low Data-Rate Software-Defined Radio Baseband with RISC-V Processor for Flexibility and Security

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Internet of Things (IoT) implementations span all sectors around the world and there is an exponential increase in the number of IoT devices. Moreover, attacks against these devices represent a significant threat and one of the potential entry points relies on their communication capabilities where many vulnerabilities and attacks are found. We argue that flexibility and security are essential features under power consumption constraints. In that context, instruction set extension of the open source RISC-V ISA is a promising and interesting solution to build new capabilities [1]. Hence we present a new architecture for flexible, secure and low-power network based RISC-V processors for IoT end-devices. Our solution targets a multi-layer (network, execution and hardware) data tracing approach to detect ongoing logical attacks such as network availability (e.g. DoS, jamming) and data integrity (i.e. packet injection) in the network and in the baseband RISC-V processor from the network entry point.

In this talk, we first discuss the network processor requirements and challenges for resource-constrained IoT end-devices using low-data-rate Sub-Ghz protocols [2]. Then we present our testbed as shown in Figure 1 to evaluate the proposed solution. The testbed is composed of three sections: hardware, software and post-processing part. In the hardware part, we connect our CV32E41P RISC-V Processor and the HPMtracer (hardware block) in our SoC built with LiteX. Currently the execution of the whole architecture is done using the Verilator SystemVerilog simulator. In the software part, we have designed a packet parser and modules to manage the HPMtracer hardware block. A packet generator is also created to produce packets. We use a post-processing part which consists of handling the data recorded by the HPMtracer from the hardware performance counters (HPC).

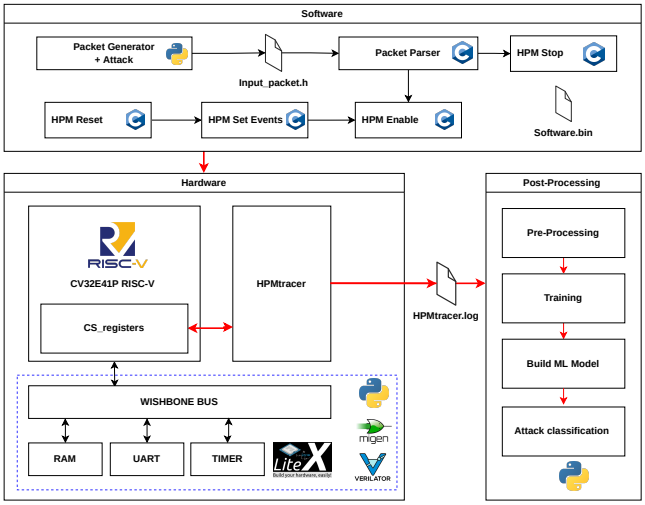

Figure 1: Testbed with tracing metrics from RISC-V CV32E41P

References

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