

# **Graphite heat spreader for power component embedded in printed circuit boards (PCB)**

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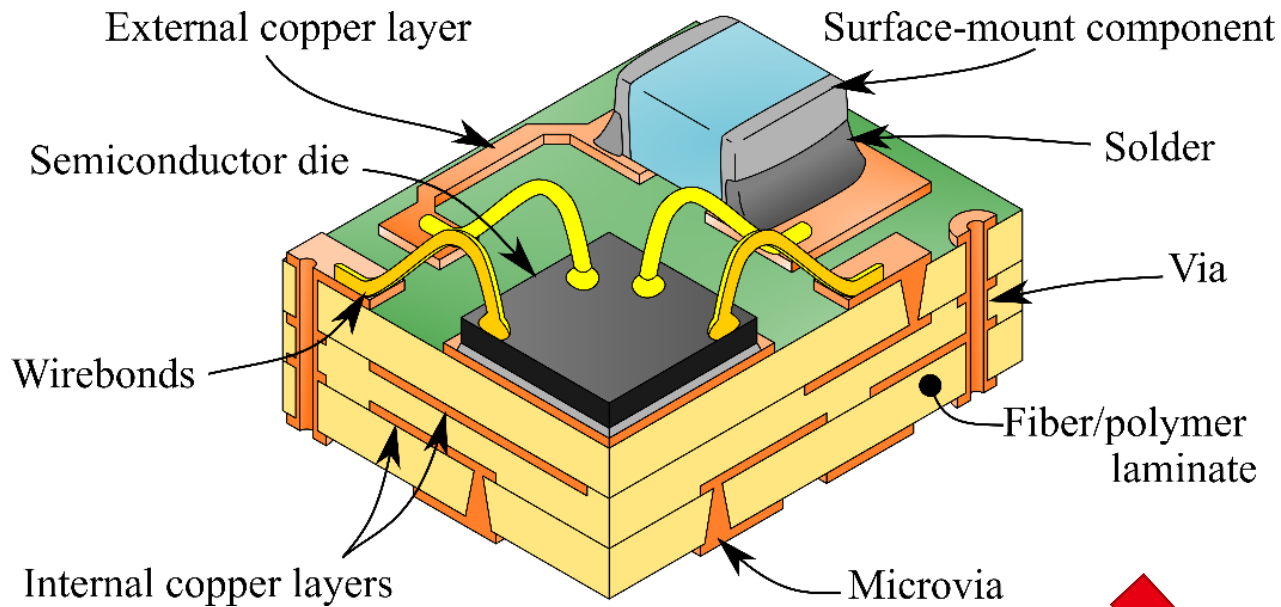
**MITSUBISHI ELECTRIC R&D CENTRE EUROPE**

- Introduction to PCB embedding technology.
- Optimization of a graphite heat spreader for PCB.
- Experimental validation
- Conclusion

# 1

## Introduction to PCB embedding technology

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❖ Printed Circuit Board (PCB) provides

→ electrical connections

→ mechanical support

for electrical components of an electrical circuit to achieve certain function.

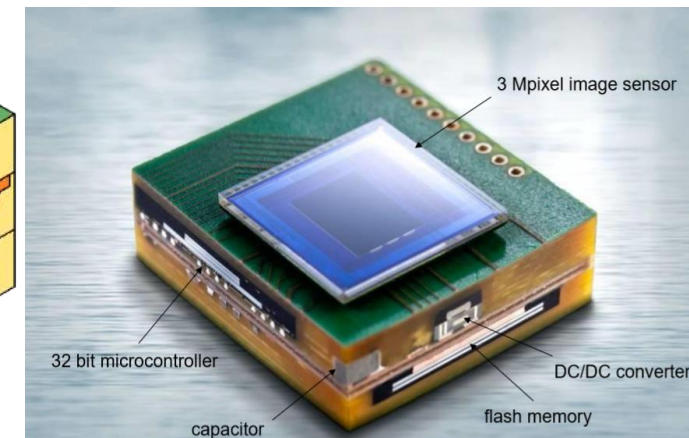
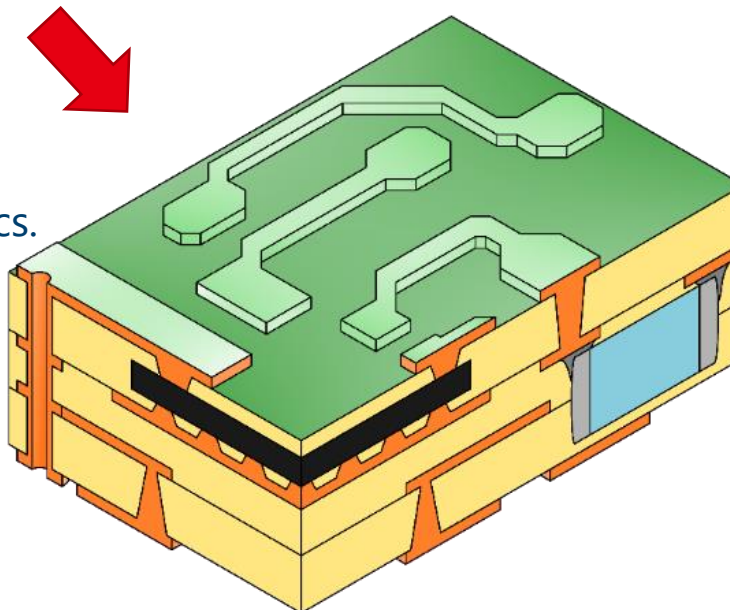
❖ PCB embedding :

→ Electrical benefits since it reduces circuit parasitics.

→ Simplifying device packaging.

→ Producing more compact systems.

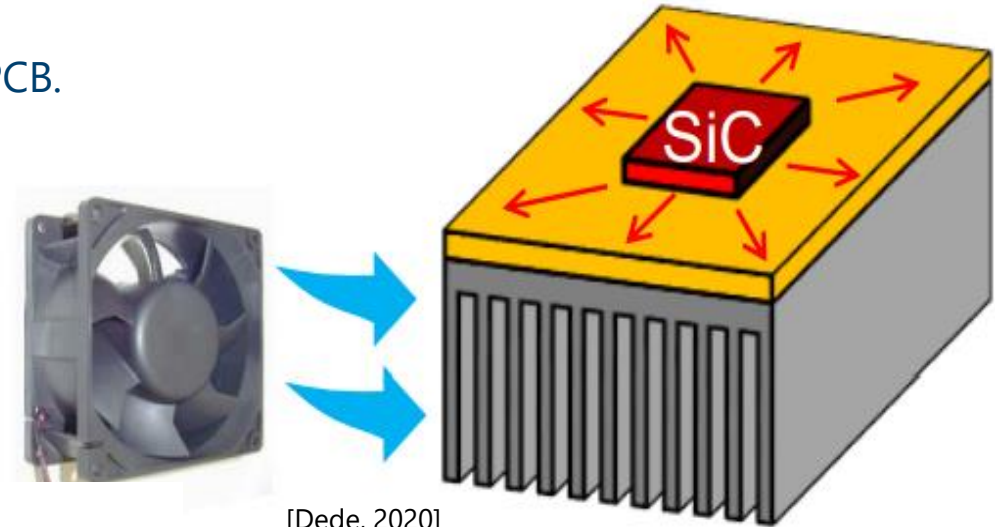
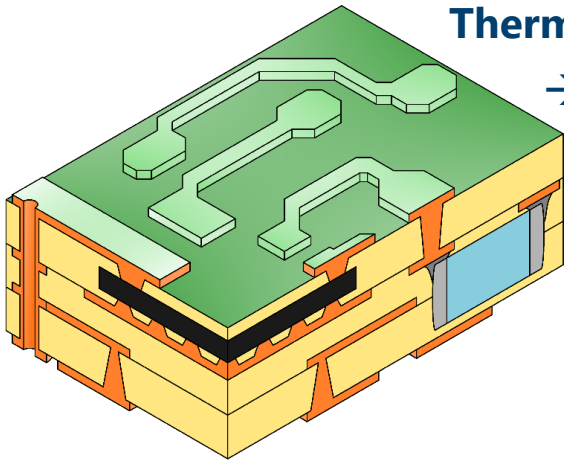
→ Thermal challenges.



[A. Ostmann, 2016]

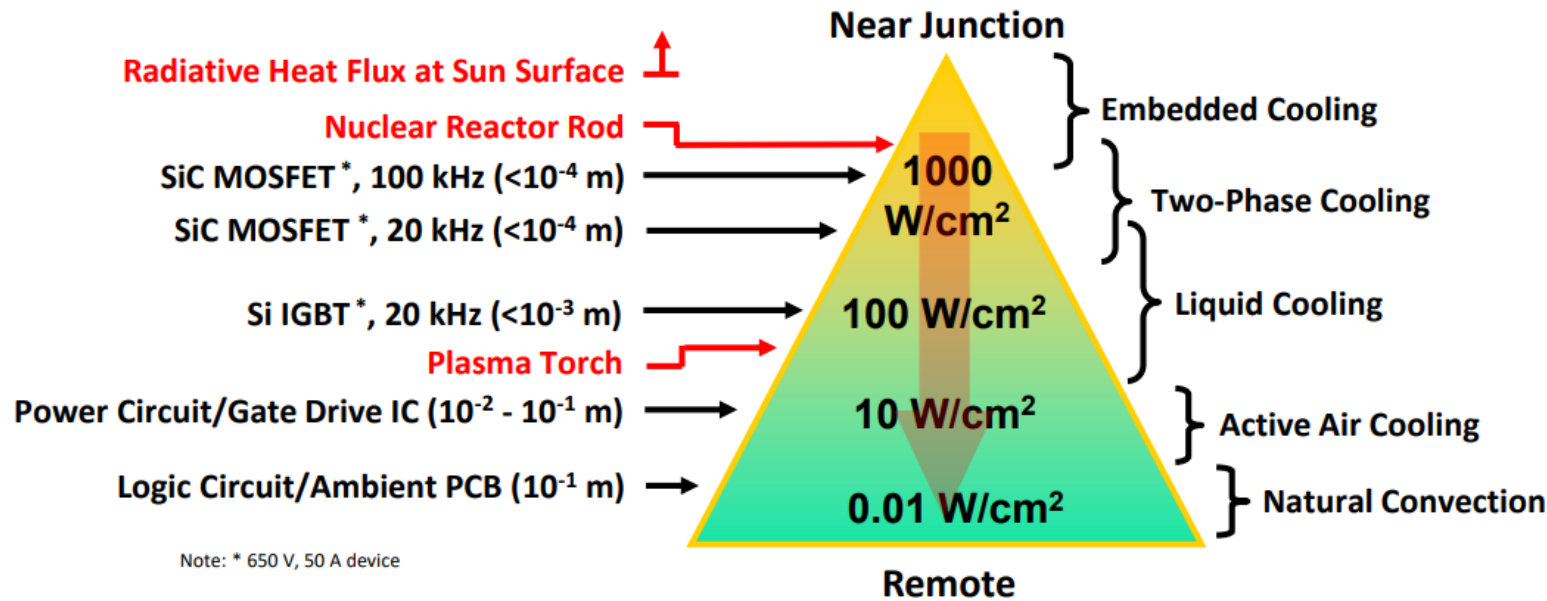
### Thermal challenges of PCB embedding

- Increasing density of electronic chips in a PCB.
- High power loss density.
- High junction temperature.
- High thermal resistance.



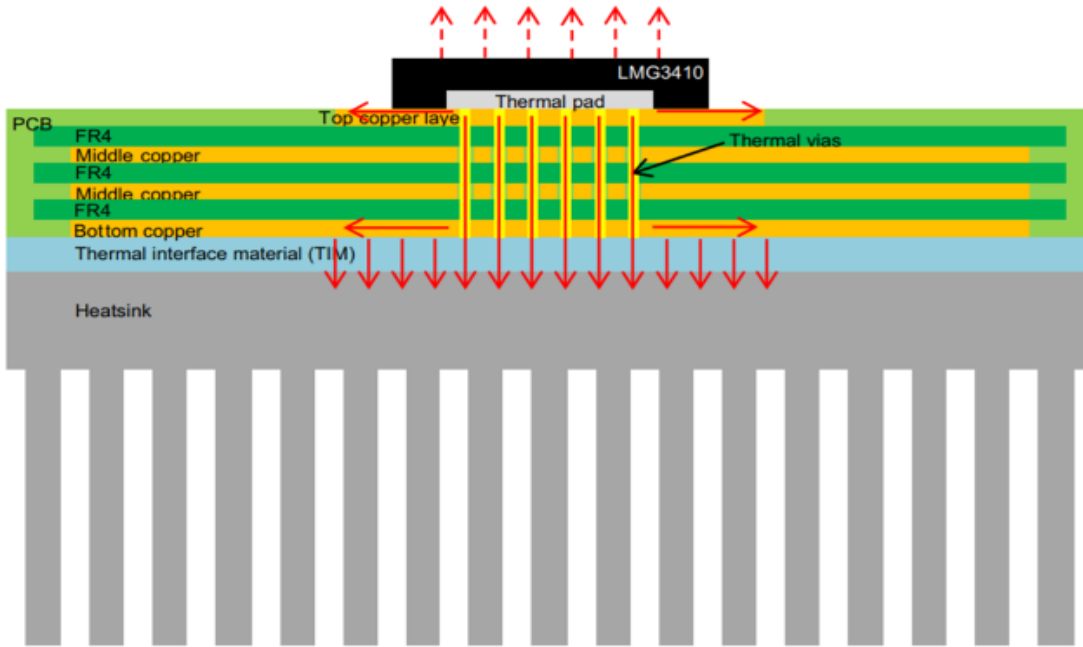
[Dede, 2020]

→ need for **an efficient heat spreader** closer to the chip.

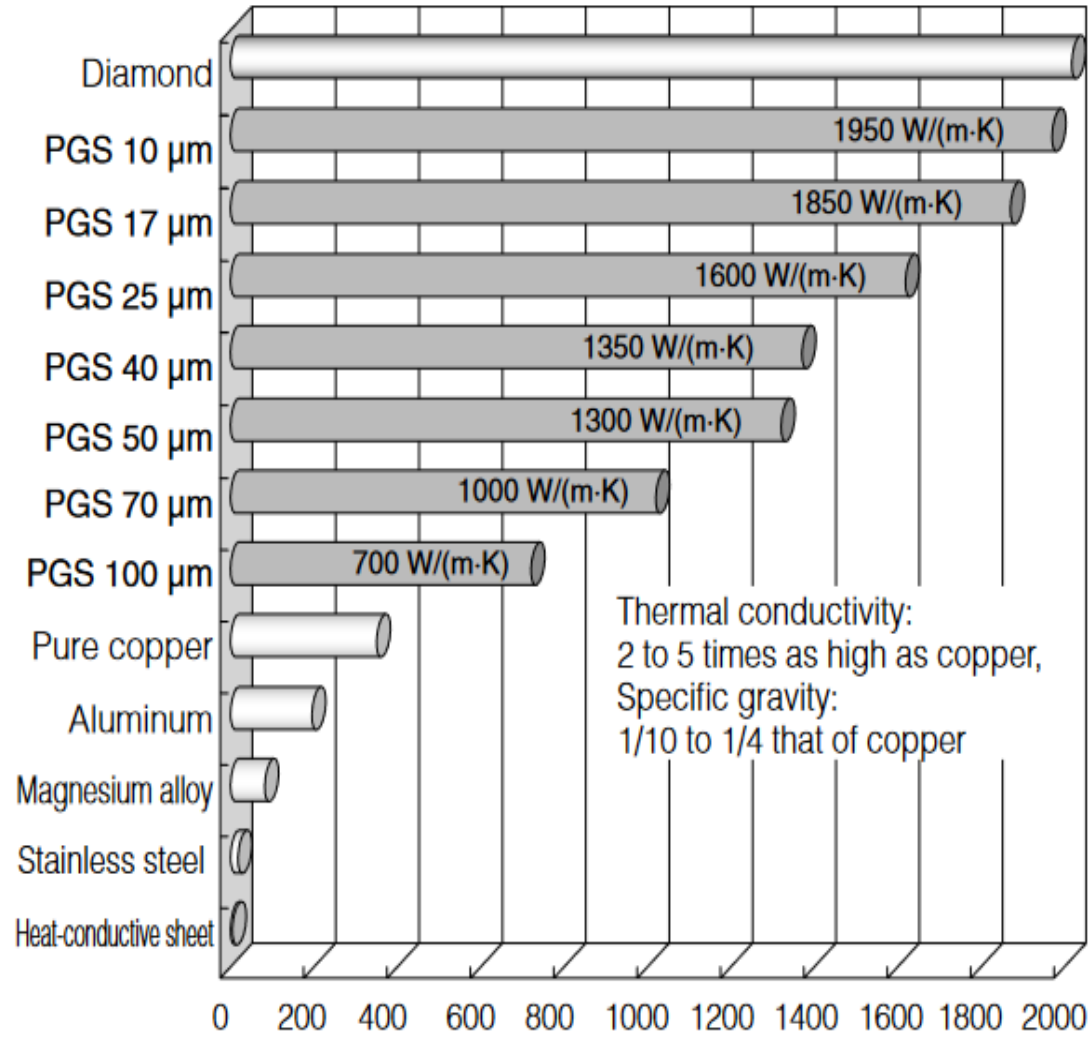


Note: \* 650 V, 50 A device

[Dede, 2020]



[www.ti.com]



Thermal conductivity:  
2 to 5 times as high as copper,  
Specific gravity:  
1/10 to 1/4 that of copper

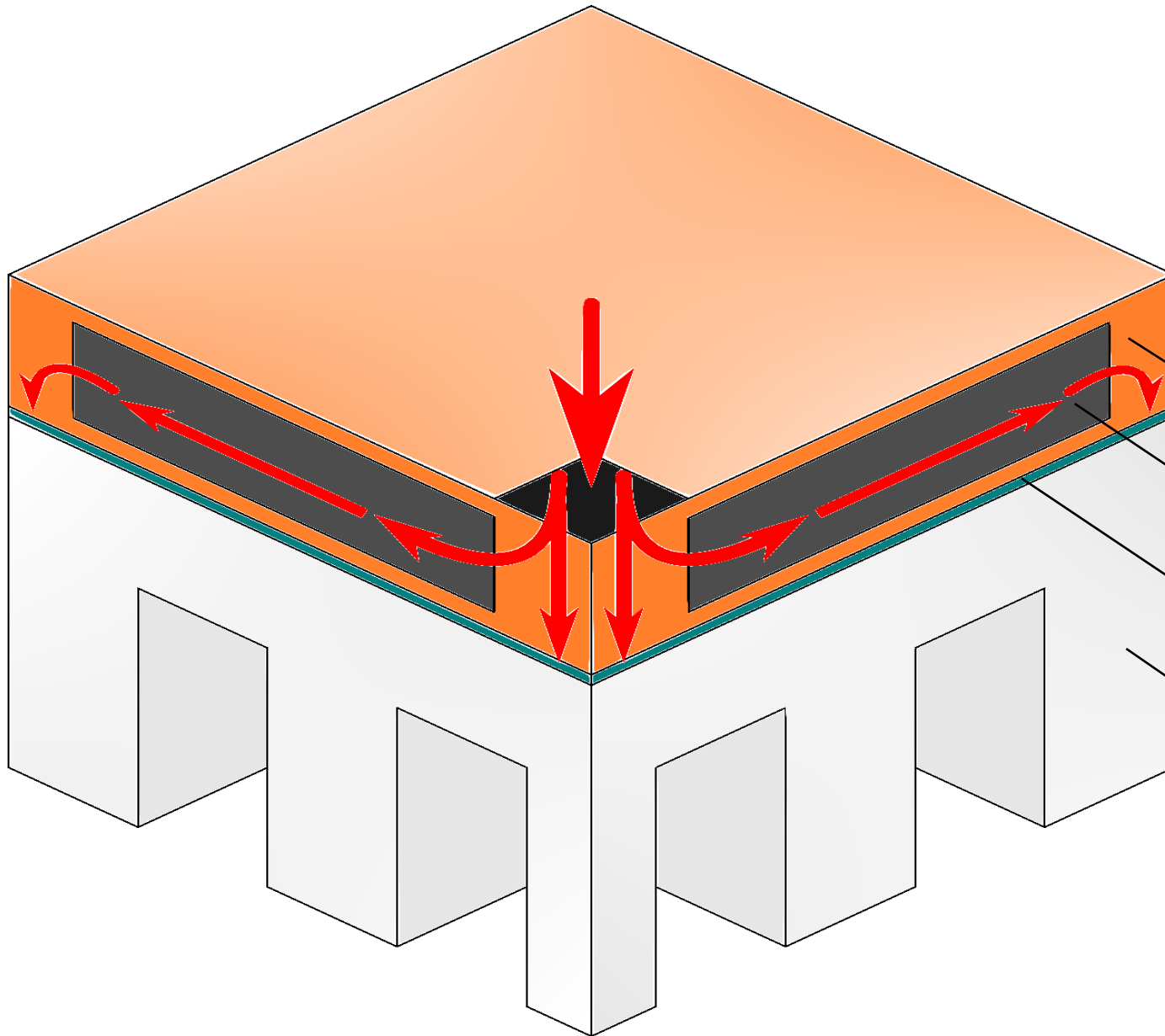
[www.industrial.panasonic.com]

- ❖ **Copper** → Conventional heat spreader → Good thermal conductivity
- ❖ **Diamond** → 2000 W/(m K) isotropic thermal conductivity.  
→ **Very expensive.**
- ❖ **Graphite** → Orthotropic → 2000 W/(m K) (in-plane).  
→ 15 W/(m K) (cross-plane).  
→ **Not expensive.**

# 2

## Optimization of a graphite heat spreader for PCB

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❖ **Graphite are embedded** in a PCB stack.

❖ **Lower thermal resistance** path for the heat,

→ Horizontally through graphite.

→ Vertically through copper.

Copper (Cu)

Graphite (Gr)

TIM

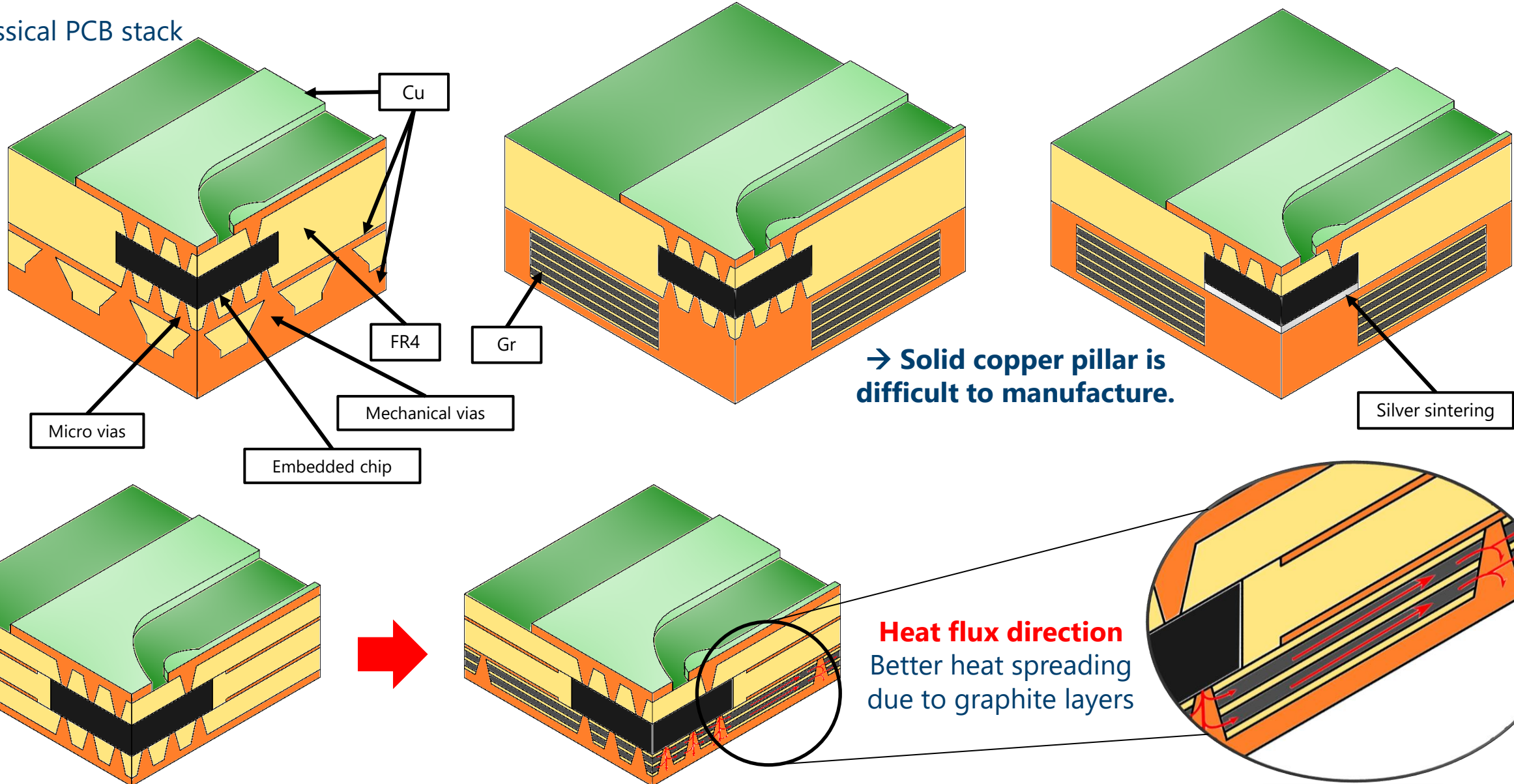
Heat sink



# 2.1

## Graphite heat spreader for PCB: the concept

Classical PCB stack



# 2.2 Graphite heat spreader for PCB : simulation results



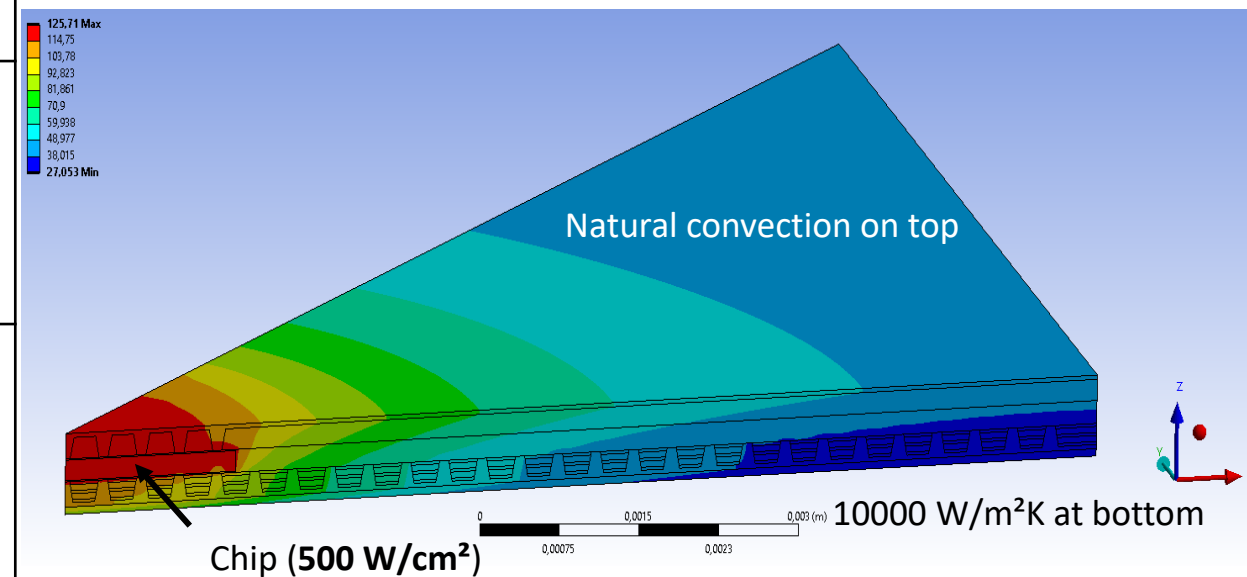
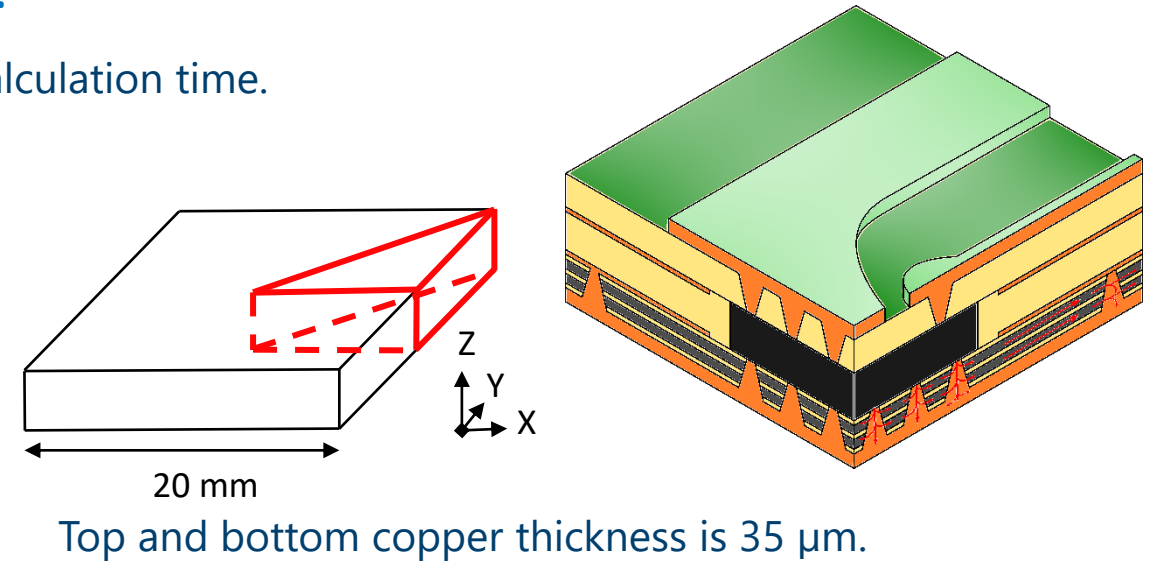
## ➤ Simulations results of and comparison of micro vias patterns:

❖ Only an eighth was considered due to symmetry to reduce calculation time.

❖  $R_{th} = \frac{T_{av} - 22^{\circ}C}{Power}$

❖ Several vias patterns on drain side were compared.

Reference sample without graphite → Rth = 4.31 K/W			
	Rth = 1.77 K/W → Rth reduction of 59.03 %		Rth = 1.93 K/W → Rth reduction of 55.34 %
	Rth = 1.79 K/W → Rth reduction of 58.48 %		Rth = 1.94 K/W → Rth reduction of 54.9 %
	Rth = 1.84 K/W → Rth reduction of 57.37 %		Rth = 2 K/W → Rth reduction of 53.71 %



# 3

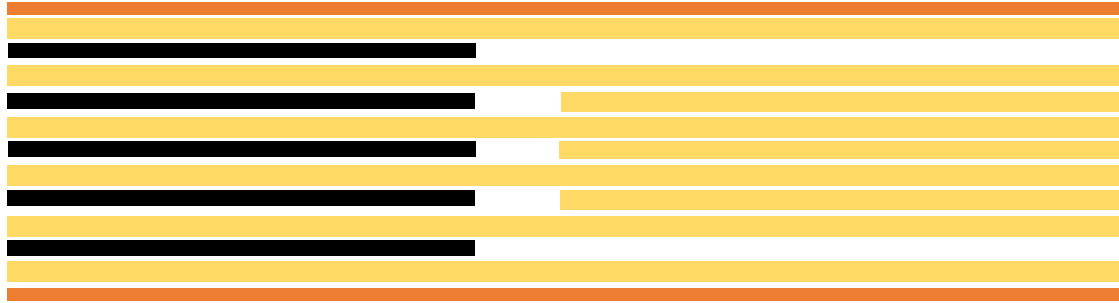
## Experimental validation

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# 3.1

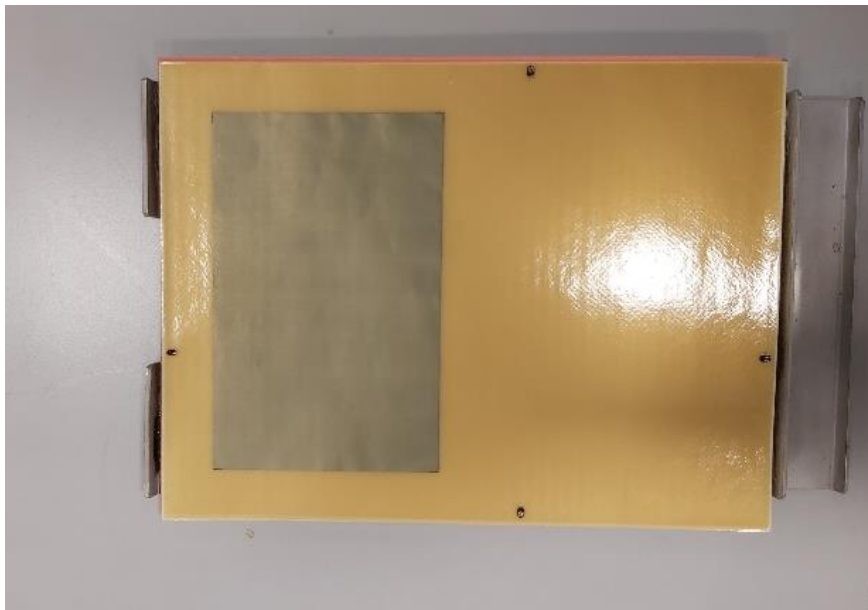
## Experimental validation : fabrication

### ➤ PCB stack :

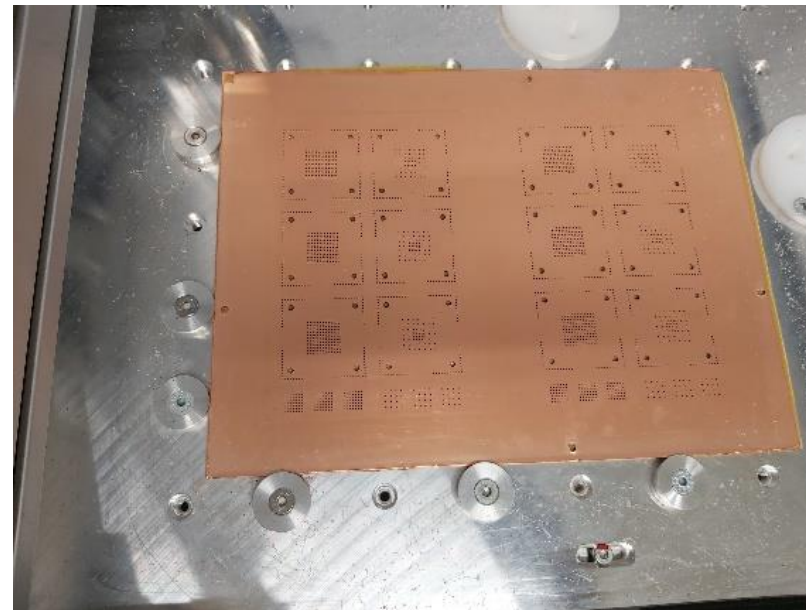


- Copper (35  $\mu\text{m}$ )  $\rightarrow$  400 W/(mK)
- FR4 (80  $\mu\text{m}$  \_Isola-PCL-FRP-370HR-106)  $\rightarrow$  0.4 W/(mK)
- Graphite (50  $\mu\text{m}$  Panasonic-PGS EYGS12181205)  $\rightarrow$  1300 W/(mK) (XY)

- ❖ The PCB is 45x45mm<sup>2</sup>.
- ❖ The active part is 20x20 mm<sup>2</sup>.

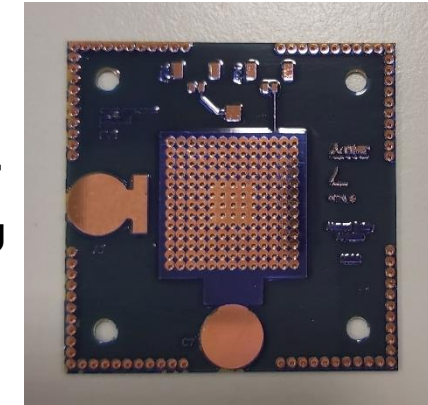


PCB stack-up

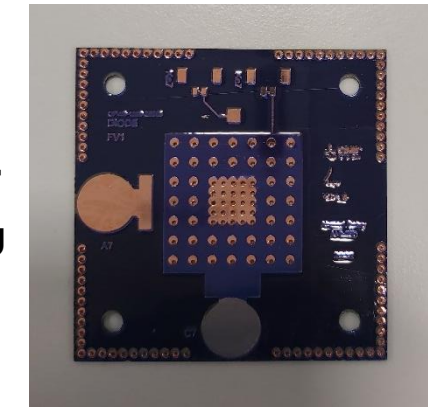


Drilling of mechanical vias

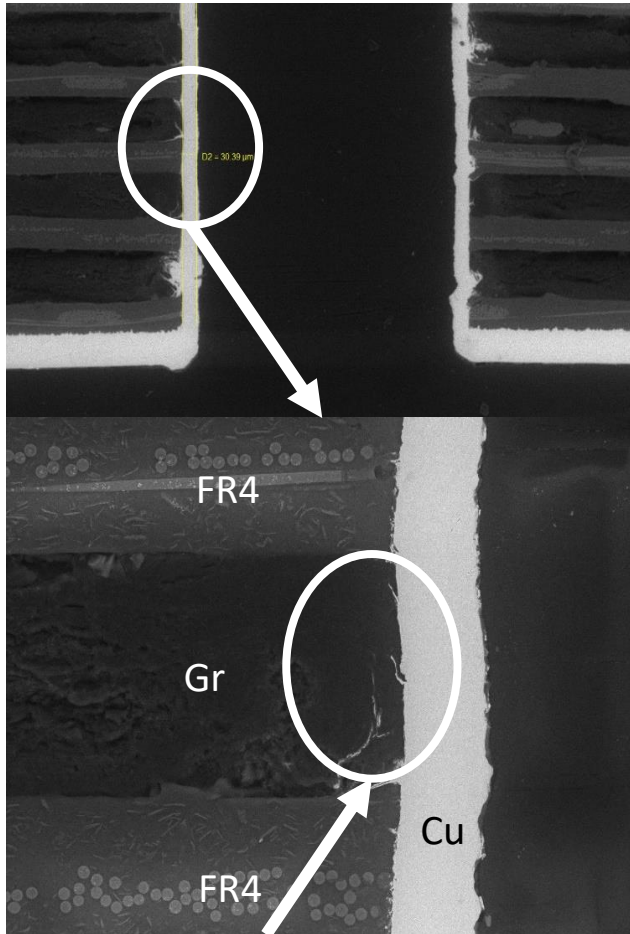
**1st vias pattern**  
 $\rightarrow$  0.7 mm diameter  
and 1.4 mm spacing



**2nd vias pattern**  
 $\rightarrow$  0.7 mm diameter  
and 2.8 mm spacing

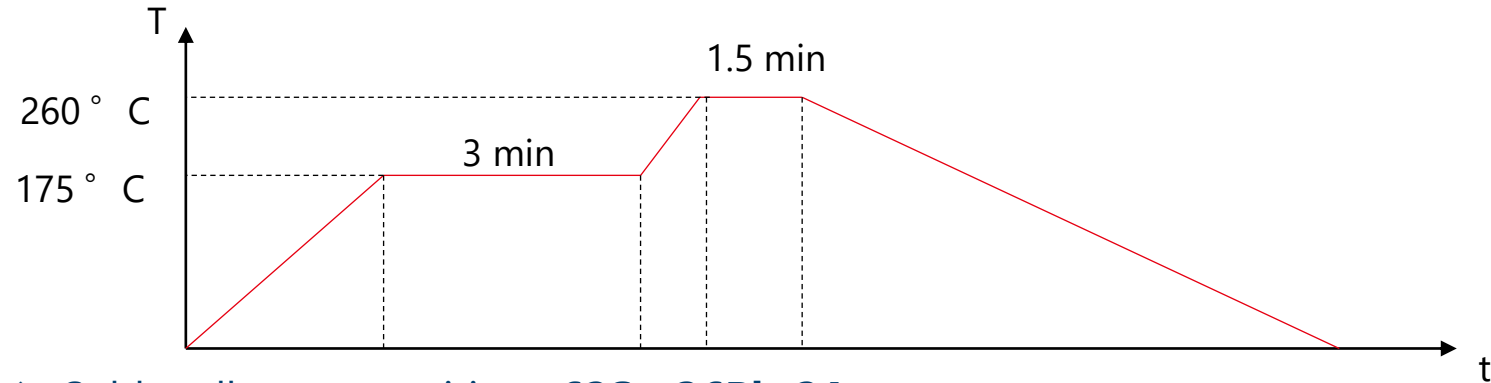


### ➤ Cross section microscopic images :



Microscopic cross-section pictures: **electro-deposited copper** of micro-vias in **good contact with graphite layers**, which is a **key point** for the proposed stack.

### ➤ Diode and connectors soldering :



❖ Solder alloy composition : **62Sn-36Pb-2Ag**

➔ thermal conductivity = 50 W/mK

➔ melting temperature = 179 ° C

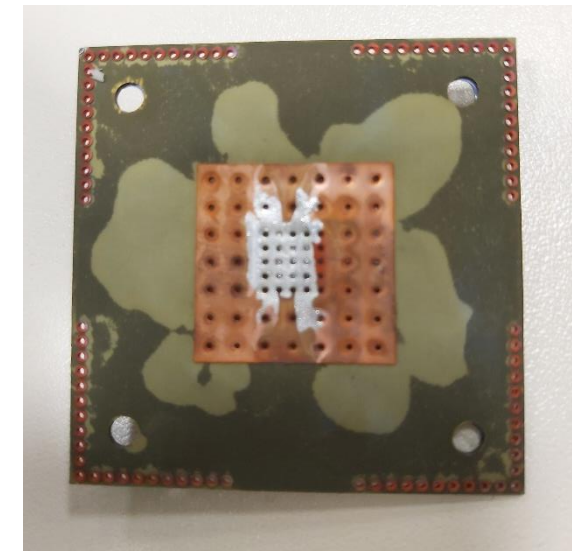
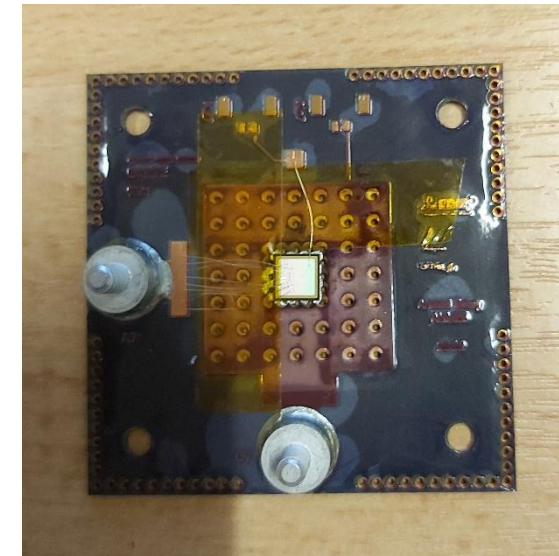
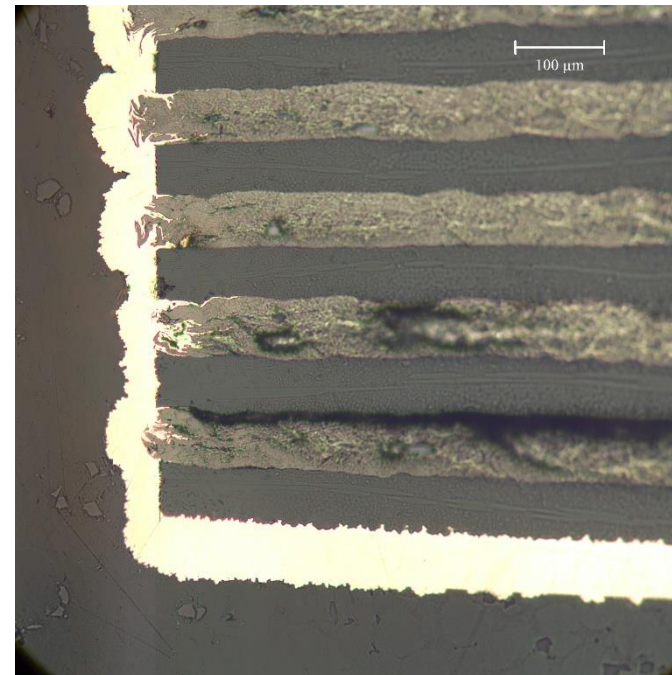
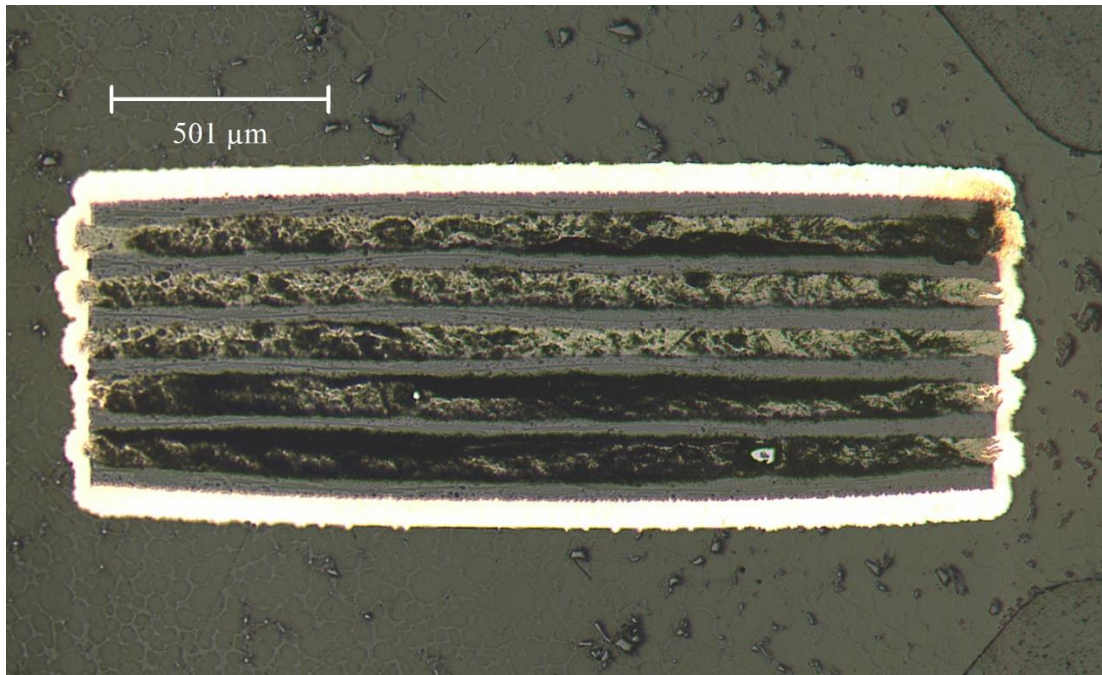
❖ Soldering temperature for reflow should be at or above 235°C for a minimal time of 20 seconds.

❖ SiC diode chip (CPW5-1200-Z050B ) is used (4.9x4.9 mm<sup>2</sup>)

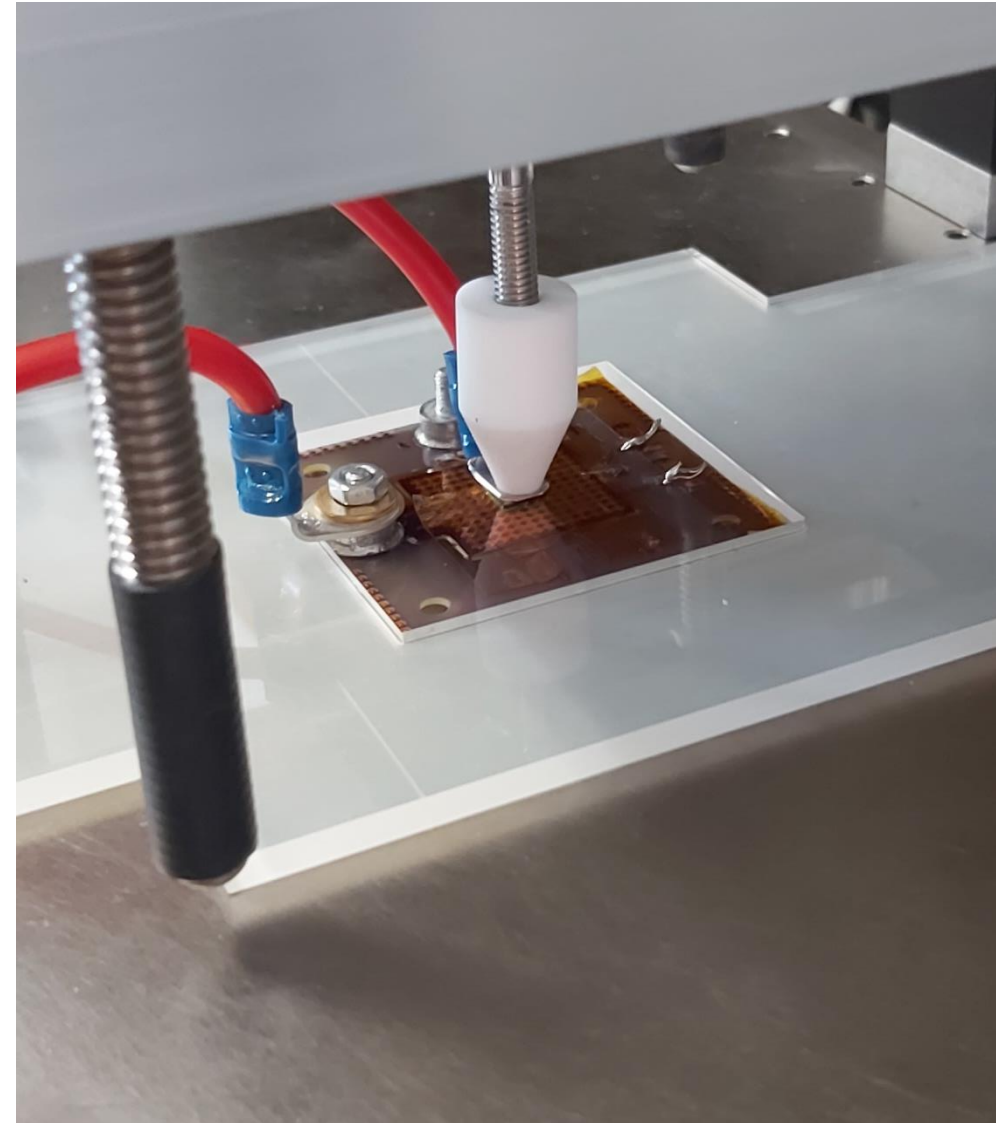
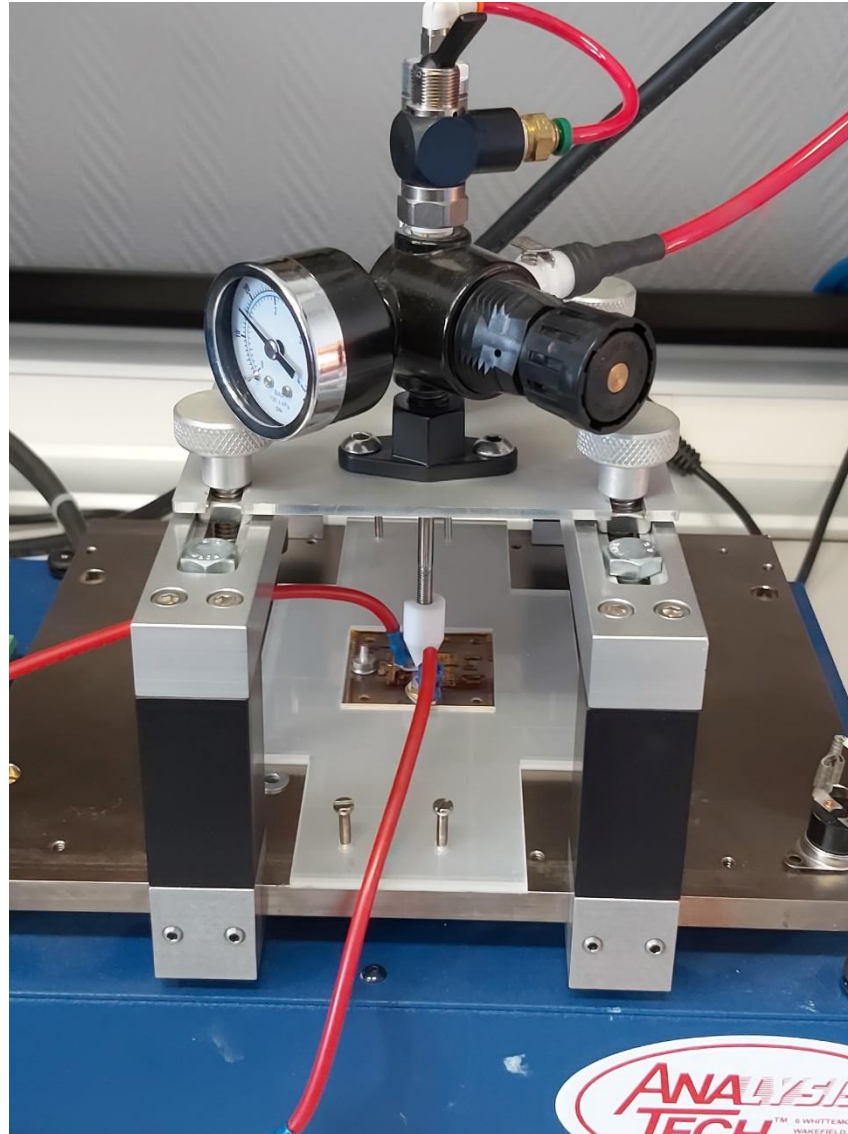
Material	CTE-XY (ppm)	CTE-Z (ppm)	Young's Modulus (Gpa)
Isola-PCL-FRP-370HR-106 (FR4)	Pre Tg: 13/14 Post Tg: 14/17	Pre Tg: 45 Post Tg: 230	Grain direction: 25.8 Fill direction: 21.9
Copper (Cu)	16/17	16/17	130
Graphite (Gr) (Panasonic PGS EYGS121805)	0.93	32	~ 2

➤ **Delamination :**

- ❖ A delamination took place in graphite samples at places without distributed vias.
- ❖ The delamination started at 200-220 °C.
- ❖ The active part of the sample is still functional because of distributed mechanical vias.

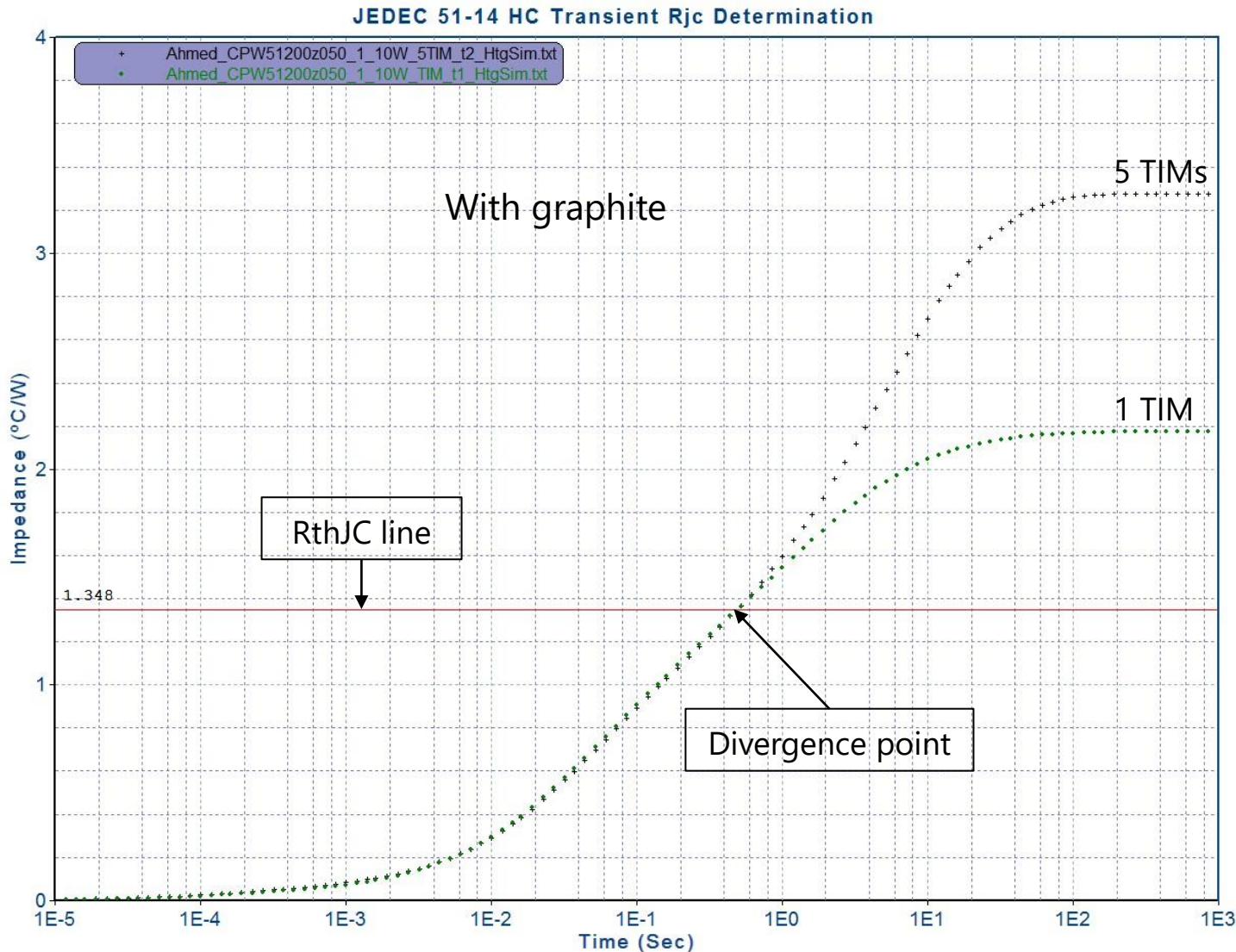


- ❖ The sample is calibrated in calibration oven to obtain a relationship between junction temperature and diode voltage.
- ❖ The test setup **measures junction-to-case thermal resistance ( $R_{thJC}$ ) using the transient dual interface method (TDIM).**
- ❖ All test were performed at **heating power of 10 W.**



# 3.3

## Experimental validation : experimental results

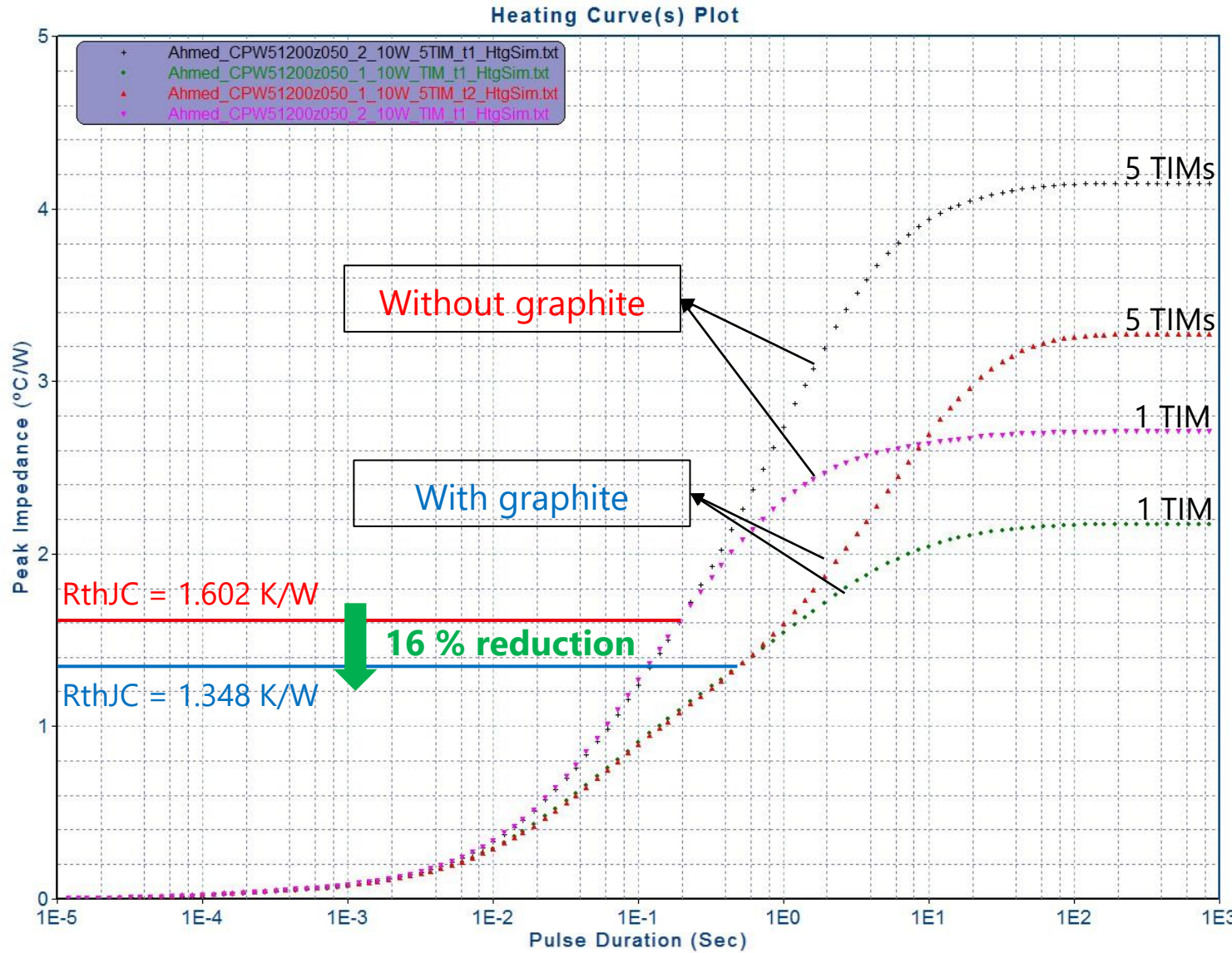


- ❖ Two heating curves are obtained by **using a thermal interface material (TIM) of two different thermal resistances.**
- ❖ **The divergence point** between the two curves indicates the thermal impedance at **which RthJC of the package** is considered.
- ❖ In this work, **one type of TIM is used** but with **different number of layers to have two different thermal resistances.**



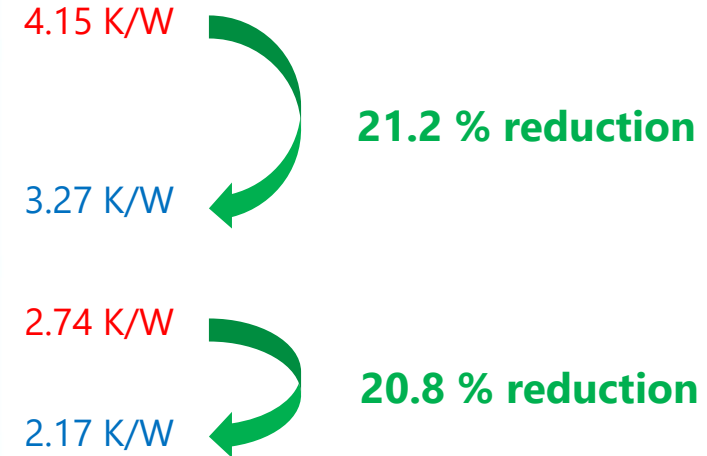
# 3.3

## Experimental validation : experimental results



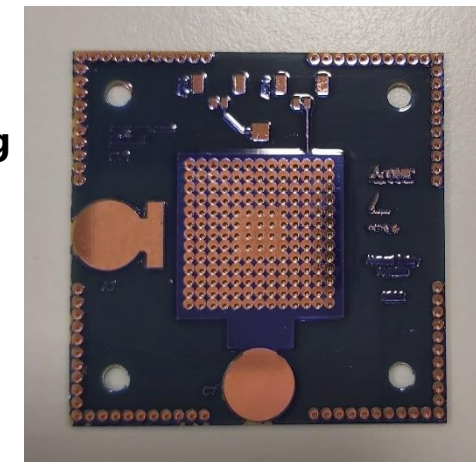
### 1st vias pattern

→ 0.7 mm diameter and 1.4 mm spacing



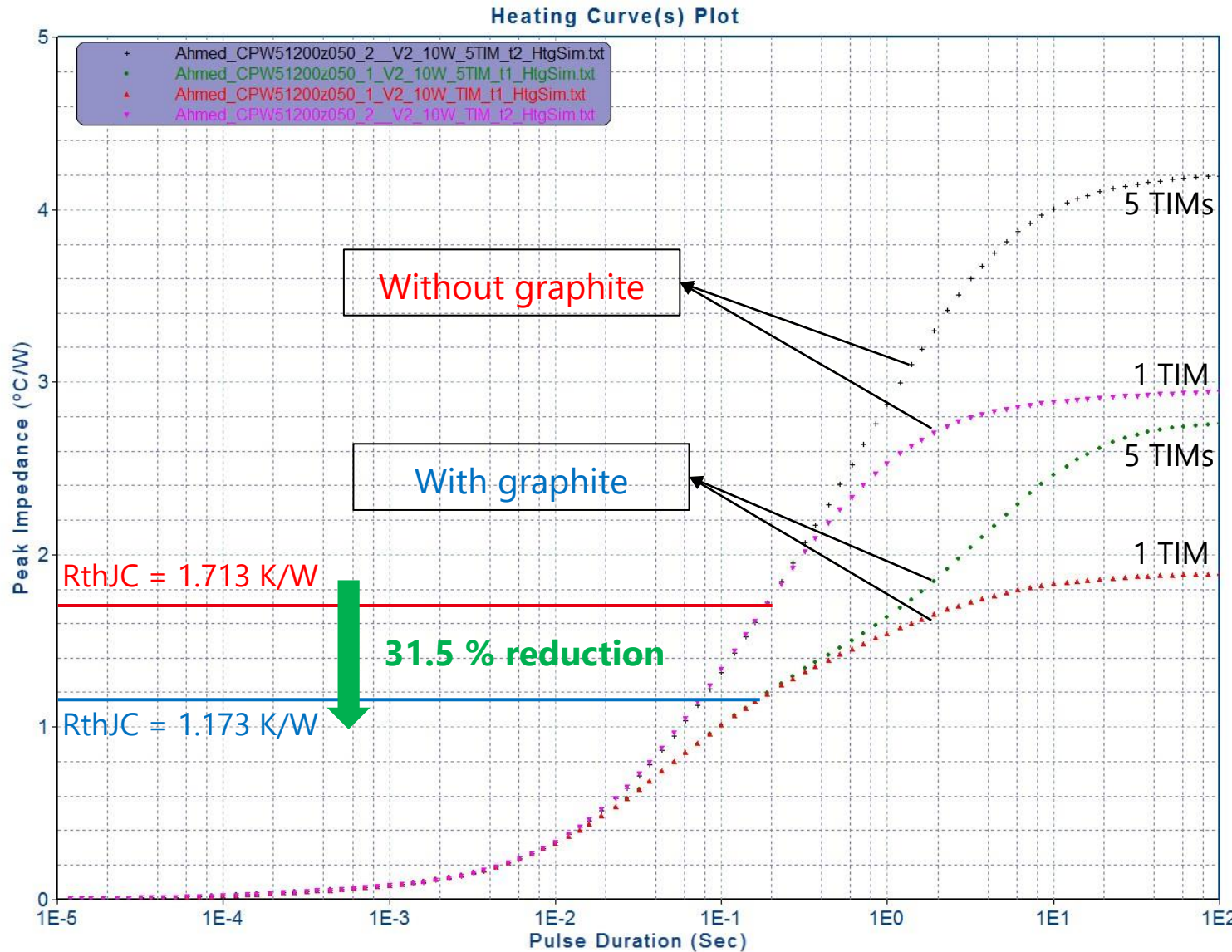
Since vias are hollow with only 35  $\mu\text{m}$  plated copper, **increasing** density of distributed vias :

- **reduces** the heat spreading impact of graphite.
- **reduces**  $R_{th}$  in samples without Gr.



# 3.3

## Experimental validation : experimental results



2<sup>nd</sup> vias pattern

→ 0.7 mm diameter and 2.8 mm spacing

4.2 K/W

34.3 % reduction

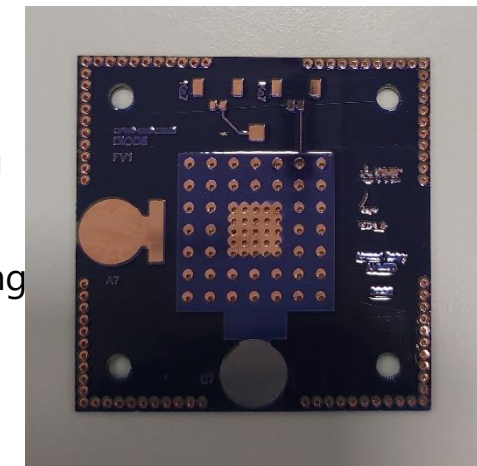
2.94 K/W

2.76 K/W

35.4 % reduction

1.9 K/W

Since vias are hollow with only 35 µm plated copper, **reducing** density of distributed vias :  
 → **Increases** the heat spreading impact of graphite.  
 → **Increases** Rth in samples without Gr.

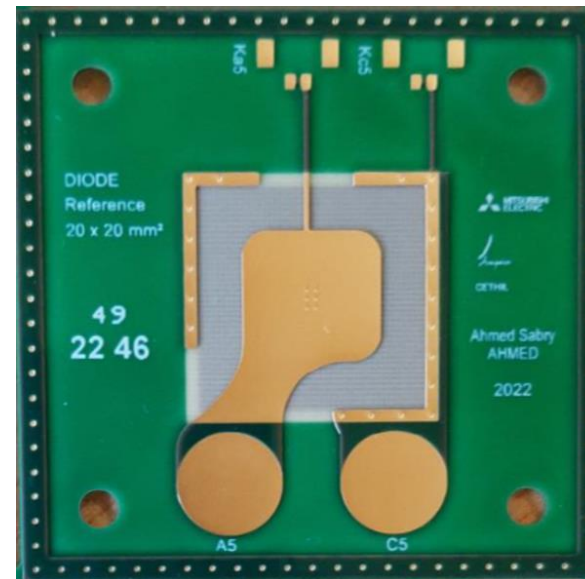


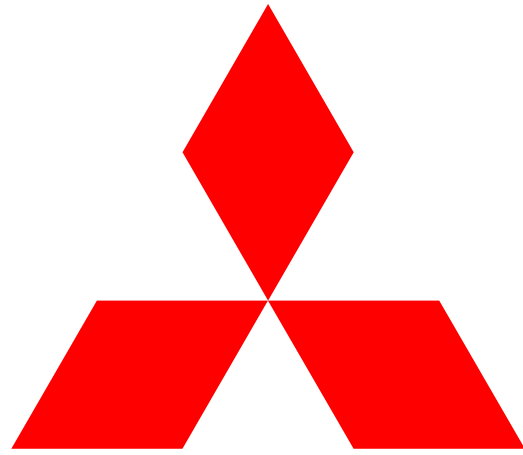
# 4

## Conclusion

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- ❖ A heat spreading solution compatible with PCB manufacturing process was proposed by embedding graphite layers in PCB.
- ❖ **Numerical simulations** predict junction to ambient thermal resistance **RthJA reduction of more than 50 %**.
- ❖ **An initial prototype with was fabricated.**  
→ A delamination took place in samples with graphite following reflow. → need for further investigations.
- ❖ **Thermal experimental results** showed a junction to case thermal resistance **RthJC reduction of 16-31 %** depending on distributed vias pattern.
- ❖ **Next step** → Tests on a **new prototype** with **embedded chip**.





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