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Planar Integrated Multilayer Capacitive Substrate For DC-DC Converter Applications

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Abstract- This exploratory work aims to develop and validate a technology of plane substrates close to "Busbar" but directly integrating capacitive layers. These capacitive layers may be used to realize the decoupling capacitor required by any switching cells on its DC bus and/or to realize the capacitors of a common filter placed on the same DC bus. As an additional property, this approach allows matching the shape and the arrangement of the capacitive layers with the building requirements of the full converter. The technological process to achieve that aim is the screen- printing technique. The process was optimized in order to manufacture high electrical performance multilayer ferroelectric ceramic capacitors. High capacitance values density ($2,2\pm 2,7\text{nF/mm}^2$), low parasitic losses ($\text{ESR} < 11\text{m}\Omega$; $\text{ESL} < 3\text{nH}$), low leakage currents, high dielectric withstand voltage ($> 300\text{V}$) are obtained. These new integrated passive components are then used for the realization of planar integrated multilayer capacitive substrate in a practical DC-DC converter.

I. INTRODUCTION

Classically, a power electronic circuit is composed of active components as discrete semiconductor devices connected to passive components as transformers, conductors, and capacitors into distinctive functional converters. In the last years, power electronics has been relentlessly driven by the progress of active device integration, the improvements of circuit topologies, the augmentation of switching frequency and the amelioration of packaging. Although the advancement of semiconductor devices integration allows reducing active component part, power passive components still occupy the major volume of the converter. Therefore, in order to improve performance, increase manufacturability and reduce costs in power electronics, the trend has placed great burden on the demand to integrated passive components [1-2]. Furthermore, it is necessary to find technologies suitable for three-dimensional integration of both active and passive components in a standardized approach. One of the simplest ways is to allow one, or more, capacitance layers to be embedded in the multilayer printed circuit board in addition to components placed on the surface of the substrate to form

a 3D compact system [3-4]. The integrated passive component technologies that are available nowadays consist of thin/thick-film technology, low-temperature co-fired ceramic (LTCC) technology, and technologies based on extensions of high-density interconnection (HDI) and other printed circuit board (PCB) technologies. Of the technologies suited for capacitive substrate integration, the thick-film technology generally provides advantages of versatility, range of component values, and functional density to allow a more integrated, more shrinkable, lighter and more cost-effective execution. Among various thick-film technologies, screen-printing technique is an attractive choice because of its ability of mass production thanks to using roll-to-roll (R2R) printing [5]. Moreover, the screen-printing technique is uncomplicated, economical, and highly feasible in a laboratory environment and it can be performed under normal conditions (atmospheric pressure and room temperature). Consequently, screen printing technique is emerging as a promising technology that permits new generation of converters to become to be nearer to 3D construction and especially more competitive in a relentless descending cost market.

The first section of this paper presents the power electronics context in which the proposed technology is positioned. The second section describes the step-by-step approach used to obtain multilayer capacitive substrates devoted to realize a capacitive substrate. Last, the third section presents a more elaborated substrate designed to integrate two semi-conductor dies in order to constitute a dc-to-dc elementary switching cell. The final aim of this work is not to realize a competitive integrated converter but to test and to validate the technology on a very simplified power stage.

II. CONTEXT OF WORK

All power electronic converter topologies are based on the association of switching cells using from 2 to $2n$ power switches (two-levels to $n+1$ levels). In most of the cases, the switching cells are connected to a dc-to-dc bus. As an example, the figure 1 shows the well-known and basic two-levels switching cell that can be realized with any kind of

power devices (here only MOSFET or IGBT+diode are considered). In all the cases, the switching cell requires adding decoupling capacitors on the dc bus, as close as possible to the power switches, in order to minimize the leakage inductance of the physical switching loop and therefore to minimize the turn-off overvoltage.

The present work is mainly focused on this decoupling capacitive function. Additional capacitors can be introduced on the dc bus as a part of a common mode filter, if necessary. Both capacitive functions, decoupling and common mode filtering, will be considered in the final demonstrator.

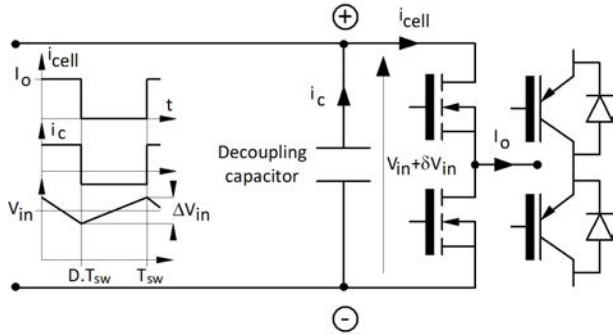


Figure 1: Operation of a decoupling capacitor

The capacitor value needed to correctly achieve the decoupling function can be estimated by using the following equation (1).

$$C_{in} = \frac{P}{4F_{sw} \frac{\Delta V_{in}}{V_{in}} V_{in}^2} \quad (1)$$

With:

- $P = V_{in} \cdot I_{on}$ nominal output power of the cell in DC conversion mode
- F_{sw} , switching frequency
- $\Delta V_{in}/V_{in}$ relative voltage ripple across the decoupling capacitor, maximal value obtained for a duty-cycle $D = 0.5$ and $I_o = I_{on}$.

For the common mode filtering, the capacitor values are approximately five to ten times lower than the decoupling capacitor values.

The proposed approach consists on one hand, in the integration of the plane capacitive zones in areas available in the considered devices, and, on the other hand, to take benefits of the plane configuration to realize three-dimensional devices by stacking plane elementary switching cells. In both cases, the vicinity between decoupling capacitors and power switches is a critical feature. The figure 3 illustrates these two ways of possible application

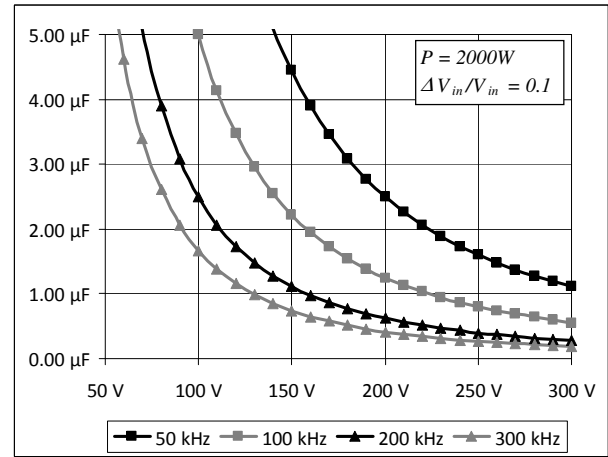
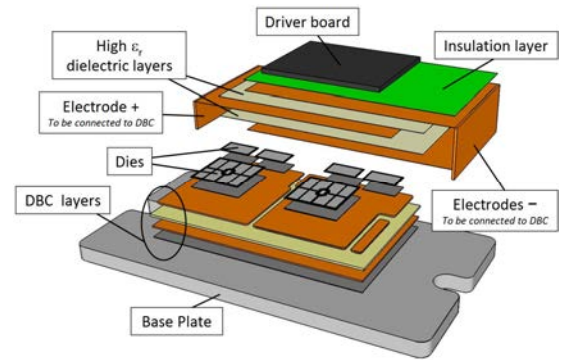
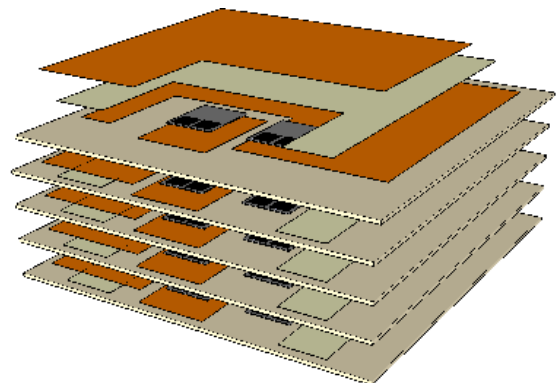


Figure 2: Values of decoupling capacitor



3-a – Decoupling in power modules



3-b – Decoupling in multicell converters

Figure 3: Projection of capacitor integration

The figure 3-a presents an example of the first option. The area available inside a power module could be used to integrate a decoupling capacitor directly in this module, above the semiconductor devices. The gate drivers can be possibly reported on the top face. If the capacitor is thin enough, the height of the module can be unchanged and therefore an improved technological cell, including the decoupling and the gate drivers, is obtained. The expected thickness of the capacitive layers being around few hundred μm , this aim can be reached.

On the schematic representation of figure 3-a, the electrodes are not representative, due to the exploded view of the capacitive zone, and the connection parts are not represented. If the proposed concept allows constituting a complete integrated switching cell, many critical issues have to be solved:

- The interconnection of the upper face of the die,
- The interconnection of the plane capacitor with the previous part,
- The realization of conductive vias through the capacitive zone to connect the gate driver to the dies.

The second option concerns multicell converter topologies. The elementary cell should be implemented on a plane capacitive substrate and n samples of this elementary block should be stacked to constitute a n -cell converter. As in the previous case, critical issues have to be solved in the same way, i.e. the interconnections between the stacked cells and the thermal management of the dies.

Therefore, the aim of the present work is to carry out capacitive substrates on significant areas (few cm^2) and to obtain high specific capacitance values with a low number of layers by using high-permittivity materials. The issues concerning interconnection and thermal management will not be considered here. Nevertheless, it was necessary to validate the proposed technology in a configuration including semiconductor power devices: therefore, a simplified switching cell has been chosen and will be presented in the third section. This cell has been defined to operate with the following characteristics:

$$P = 2000W, V_{in} = 200V, I_{on} = 10A, F_{sw} = 100kHz$$

This choice induces significant values of the decoupling capacitor, around one to two μF for a relative voltage ripple of 10% (see Figure 2). It seems appropriate to evaluate the concept limitations if current dielectric materials are used.

The next section presents the technological process and its optimization to realize the capacitive layers.

III. REALIZATION AND CHARACTERIZATION OF INTEGRATED CAPACITORS

A. Process Flow and Discussion

Multilayer ferroelectric (FE) ceramic capacitors were fabricated using screen-printing technique. The advantage of screen-printing over other print processes is that the press

can print on substrates of any shape, thickness and size. A significant characteristic of screen-printing is that a greater thickness of the ink can be applied to the substrate than is possible with other printing techniques. Thanks to the simplicity of the application process, a wide range of conductive and dielectric inks is available for use in screen-printing than for use in any other printing process. In this research, the 96% alumina, 2 inches squared and 635 μm thickness substrates were used to be suitable for thick film processing. The ceramic substrates are quite uniform and have very good ability for facing high temperature during sintering progress. For the purpose of fabricating multilayer ceramic capacitors MLCCs, Barium titanate based ferroelectrics are usually used as dielectric layers because of their high and stable dielectric properties. Due to the HK (high dielectric constant) inorganic capacitive substrate could be used to manufacture embedded capacitors between conductive layers and could be designed to form a sandwich structure between two silver layers. Nevertheless, it is also important to note that screen printing also has disadvantages such as the screen frames are durable, they can eventually become warped and uneven after reused many times in roll-to-roll process. Such problems influence on the quality of the dielectric layers, they can be less uniform and have more defects. The optimized process, presented in figure 4 mainly focused on removing defects in the ceramic to increase the dielectric breakdown strength and to reduce the dielectric loss of the capacitor.

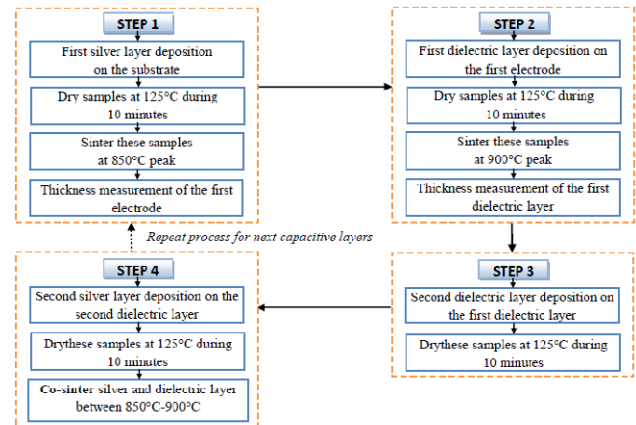


Figure 4. Summary of the process flow used to fabricate integrated capacitors

B. Characterization of the Capacitors

In the first step, classic metal-insulator-metal (MIM) capacitors (figure 5) were successfully realized according to the proposed process flow. The measured thicknesses range from 18 to 25 μm and from 30 to 40 μm for the silver electrodes and the two dielectric layers, respectively.

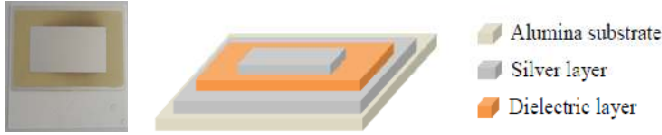


Figure 5. 3D construction of a simple MIM capacitor

In figure 6 the impedance characteristics of the sample are plotted which proves to be capacitive from 100Hz to 900 kHz. Around 1 MHz, the ESR (equivalent series resistance) may be determined whereas for higher frequency the inductance behavior becomes predominant. The ceramic capacitors realized have large capacitance values and exhibit low ESR and low ESL (equivalent series inductance) making them suitable for high power and high frequency applications. The measured leakage current (not presented here for the sake of clarity) of MIM capacitors ranges in the order of nano-amps (nA). The resistance - generally referred as the "insulation resistance" (R_p) is around 1G Ω at 100V.

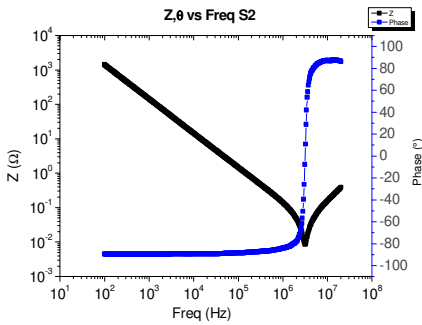


Figure 6. Impedance and phase behavior of MIM capacitors

Last, Table 1 shows that the withstand voltage of the FE capacitors at room temperature can reach a value of 300V under DC stress. On the other hand, thermal stability is one of the important factors limiting capacitor applications. The dielectric properties of MIM capacitors were therefore also measured as a function of temperature as shown in Figure 7. Due to the nature of the dielectric used and not surprisingly, the capacitance value changes with the temperature, the maximum value being reached at 25°C. These changes with the temperature imply that this material composition is probably not a good candidate for severe environment applications [6].

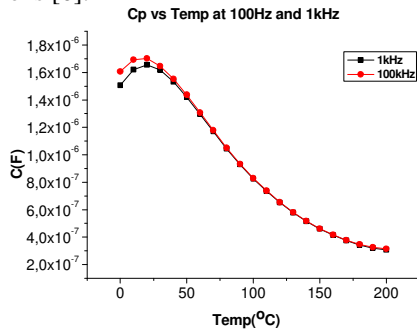


Figure 7. Capacitance behavior versus temperature

Name	U (V)	I (μ A)	Result	C (μ F)
S1	1	Low	Ok	
	10	Low	Ok	
	20	Low	Ok	
	50	Low	Ok	
	100	0.2	Ok	
	200		Ok	
	300		Flashover	
	400	>I _{limit}	Flashover	1.9
S2	1	Low	Ok	
	10	Low	Ok	
	20	Low	Ok	
	50	Low	Ok	
	100	Low	Ok	
	200	Low	Ok	
	300	0.7	Ok	
	400	>I _{limit}	Flashover	1.26
	450	>I _{limit}	Flashover	1.22

Table 1. Determination of the withstand voltage of the samples under study

In a second step, multilayer FE capacitors were developed from MIM capacitors with simple construction in figure 8. The main goal of this work is to determine the ability to realize multilayer samples using the same process but with different superimposed frames.

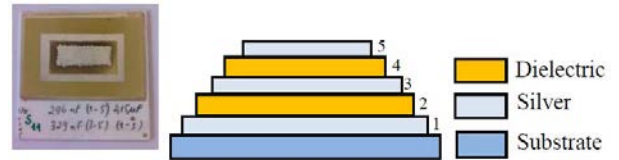


Figure 8. Photo, construction of multilayer capacitor in series

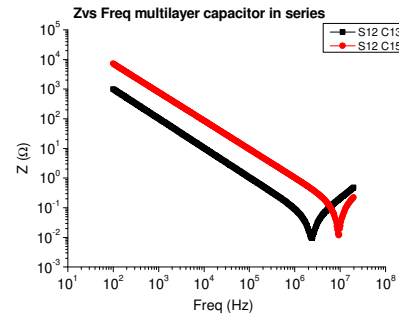


Figure 9. Impedance characterization of multilayer capacitor in series

The sample presented in figure 9 includes capacitor C_{13} and C_{35} in series, thus the equivalent multilayer capacitor is $C_{15} = C_{13}C_{35}/(C_{13}+C_{35})$. The parameters of the capacitor C_{13} and C_{15} are compared in figure 8. It is obvious that there is a decrease in the capacitance value, a shift in the resonant frequency (the ESR being nearly the same) from 3MHz to 5MHz. However, such a design is limited in shape and configuration to build up capacitive substrate.

In a third step, the layers are stacked to create the multilayer structure depicted in figure 10. The comparison between impedances of a simple MIM capacitor S14 and a multilayer capacitor S25 (figure 11) proves that the quality of the interconnections between electrodes allows establish multilayer capacitor.

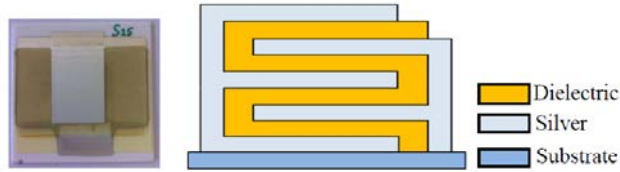


Figure 10. Photo, construction of interdigitated multilayer

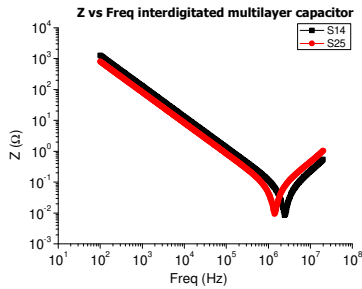


Figure 11. Impedance characterization of interdigitated multilayer

In summary, the capacitors made from ferroelectric ceramics realized by screen-printing technique present good values of their main characteristics together with a reduction in their volume. The demonstration of the possibility to realize a stacked structure to make a capacitive substrate thanks to screen-printing is achieved. It also proves that changing the pattern of the screen mask may allow realizing different capacitive areas on the same substrate for filtering or decoupling functions in a power electronic converter.

IV. INTEGRATION OF MULTILAYER CAPACITORS FOR APPLICATION TO FILTERING AND DECOUPLING FUNCTIONS IN THE CONVERTER

Therefore, the aim of the next step of this technological approach is the integration of capacitive functions very close to semiconductor power devices, as described in section II. This proximity is mainly required to minimize the parasitic inductance of the switching cell. To emphasize the interest of the process regarding to the integration possibilities, a common mode of filtering part directly connected to this switching cell has been added on the proposed capacitive substrate (figure 12). This substrate constitutes the base of a 200V-10A switching cell that should be able to operate in a few ten to few hundred kHz frequency range. The value of the decoupling capacitor has to be around few μF while the values of both common mode

capacitors, using the same dielectric layers, can be limited to few ten nF. This option of common mode capacitors directly associated to the switching cell can lead to a very efficient common mode filtering. To obtain the complete filtering function, a common mode choke must be added, that will be achieved in a next step of the work, the final aim being here to test a complete cell including the semiconductor power devices. Therefore, the substrate is divided in three capacitive zones; two smaller zones for two filtering capacitors and one larger zone for decoupling capacitor.

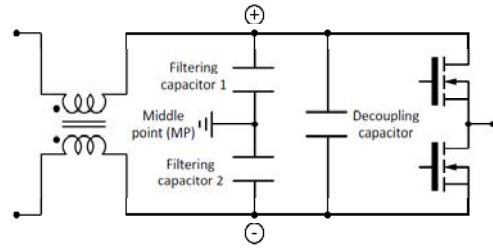


Figure 12. Proposed topology using integrated capacitive

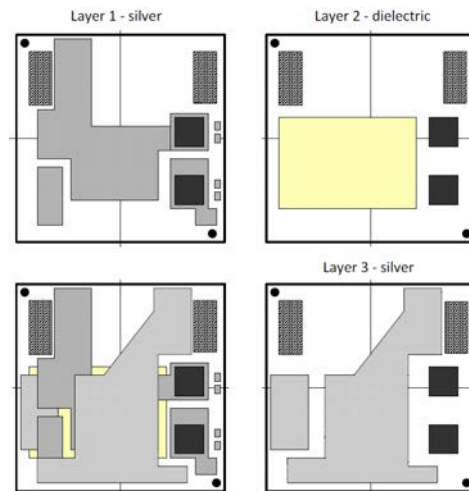


Figure 13. Drawing of specific screen masks

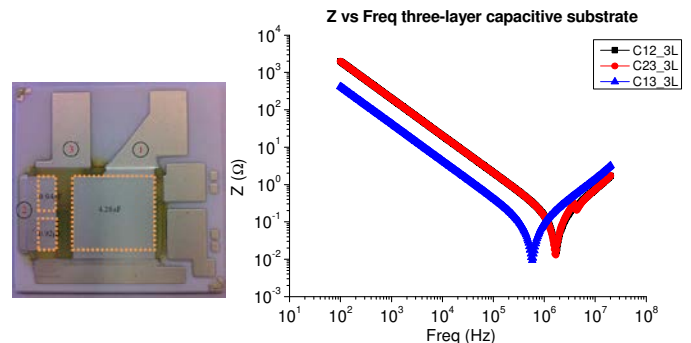


Figure 14. Photo and impedance characterization of the multilayer capacitive substrate

Specific screen masks have been realized (figure 13). Using the same process that the one described in the first stage, the three first capacitor layers were successfully fabricated and their capacitance values increase gradually with the number of layers (1st capacitor layer $C_{12_1L}=C_{23_1L}=0.26\mu\text{F}$, $C_{13_1L} = 1.42\mu\text{F}$; 2nd capacitor layer $C_{12_2L}=C_{23_2L}=0.59\mu\text{F}$, $C_{13_2L} = 2.78\mu\text{F}$; 3rd capacitor layer $C_{13_3L}=C_{23_3L}=0.9\mu\text{F}$, $C_{13_3L} = 4.28\mu\text{F}$). The characterizations of the new passive component are shown in figure 14 and prove to be compatible with the objective.

V. CONCLUSION AND FUTURE WORK

In the first step, an important work to optimize the process to realize multilayer capacitors thanks to screen-printing technique has been achieved and step-by-step samples- ranging from a very simple planar capacitor to more complicated ones- have been realized and tested. High electrical properties were obtained. In the second and third steps, specific masks allowed to realize a multilayer functional capacitive substrate. The ability of screen-printing to be a useful technological tool for power integration has been demonstrated. In a next step, the semiconductor dies will be connected to the capacitive substrate and the complete circuit will be tested.

ACKNOWLEDGMENT

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