Thermal Stress Analysis Comparison in IGBT Power Modules between DC and switching Power Cycling

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***Abstract*—The purpose of this paper is to show and highlight the observed differences in power cycling test results between DC and switching modes. The focus is done in the generated thermal stresses in IGBT power modules where degradations concern the bond-wire contacts and interconnections. It has been found that for the same ΔT_J test conditions, the necessarily higher load current in DC mode leads to a higher thermal stress in the bond wires than in switching mode. Consequently, the bond-wire contacts experience locally a slightly higher ΔT than compared to the switching mode and to a slightly lower lifetime. The results of the experimental tests were corroborated by electro-thermo-mechanical simulations with which the difference in lifetime between the two modes was evaluated.**

***Index Terms*—Power cycling tests, IGBT power modules, DC and switching tests, thermal stresses, lifetime.**

I. Introduction

Power semiconductor devices play a major role in power electronic systems. They are also the most critical part in terms of reliability and the most fragile components [1,2]. The main failures in such devices are caused by thermomechanical fatigue of the material assembly and interconnects [3-5]. Aging reliability tests are thus necessary to estimate the lifetime of such devices. These ones are usually done by Power Cycling Tests (PCTs) as they reproduce thermomechanical stresses seen in applications. The test principle is based on thermal fatigue of the devices due to periodic succession of self-heating and cooling phases [6-8].

Since many decades, the PCTs are performed essentially in DC mode where the self-heating of the power chips is obtained by the conduction losses only (Joule effect). Nowadays, such reliability tests are also performed in switching mode under high voltage where the heating is obtained by a combination of conduction and switching losses [3,9,10,11]. Over the past decade, comparatively only few tests have been performed in switching mode. Since the stress conditions in this last mode are more representative of those applied in operation, the stresses and degradations undergone should be better correlated with the operating conditions. Whatever the test mode, the objective is to evaluate the behavior and the lifetime of the assembly, the packaging and the interconnections. Nevertheless, the thermal stress distributions on the chip can be modified according to the relative weight between conduction and switching losses. Thus, it is necessary not only to compare the effects of the PCTs in DC and switching modes but also to evaluate the impacts of the different parameters of PCTs in switching mode (switching frequency, duty cycle,…) for a same junction temperature swing (ΔT_J) or same total dissipated power. Until now, very few papers have reported some technical and general comparisons between power cycling tests in DC and switching modes [3, 10], but not an in-depth analysis of stress distribution and their consequences in lifetime.

In this paper we try to fill this gap using experimental and numerical results. First, it is reported a comparison in experimental results of power cycling test done in IGBT power modules done in DC and switching mode for a same ΔT_J. Then, an electro-thermo-mechanical finite element model has been built in order to highlight the thermal and mechanical stress distributions in both test types and provide explanations for the observed differences in behavior.

II. Power cycling test setup and principles

A. DC Power cycling test bench

Usually, PCTs are performed at low voltage DC current conditions [12-14]. A typical test bench scheme for this purpose is shown in Figure 1a. The dies of the power modules are always in on-state and the DC current is alternatively and periodically driven in each tested power modules by auxiliary switches. Each module is cooled by heat-sink system such as a fluid-cooled plate. It is important to note that power cycling generates strong temperature gradients and inhomogeneous temperature distribution within the power modules.

As visible in Figure 1b, during the heating period, the power dies heat up the whole device. Depending on the power pulse duration, the heat flow will concern only dies vicinity with upper contact technology (bondings, ribbons…) for short pulses or deeper layers (such as solders between chip and DBC substrates, DBC substrates and solders between DBC substrate and base plate) for longer pulse durations [15]. A permanent low current (I_{sense}) is flowing through the devices under test (DUTs) in order to get the junction temperature (T_J) by a thermo-sensitive electrical parameter (TSEP) [16-19]. For this purpose, the forward voltage drop such V_{CE} for IGBTs is generally used during the cooling phase. Dies maximum temperature (T_{Jmax}) can be evaluated by extrapolation at the end of the power pulse and the minimum temperature (T_{Jmin}) at the end of the cooling phase. Case temperatures are measured by thermocouples in the base plate or the ceramic substrates underneath the power dies. A temperature and fluid flow

regulator sets the temperature reference. The DC current pulse duration and level set the temperature variations and thus the maximum temperatures for junction (T_{Jmax}) and case (T_{Cmax}).

As output, some reliable ageing indicators must be monitored along the test. In practice, the most common monitored parameters are the maximum junction and case temperatures (T_{Jmax}, T_{Cmax}), temperature swings (ΔT_J, ΔT_C), thermal resistances such as junction-to-case (R_{thJC}) or junction-to-ambient (R_{thJA}) and forward voltage drop (V_{CESAT}) [20].

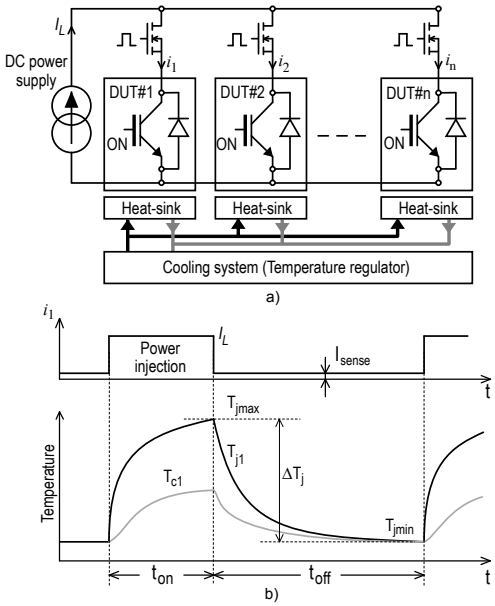

Fig. 1. Principle of power cycling test in DC mode: a) bench schematic b) power cycles and junction (Tj) and case (Tc) temperature swings.

B. Switching power cycling test bench

The test bench schematic, shown in fig.2, is made up of two independent parts: a "*Load part*" and a test part called "*Device under test (DUTs) part*". The two parts are only connected by the load inductances and the same DC bus. It can be tested until 3 DUTs, each DUT is connected by a load inductance to an inverter in the load part. Each inverter/DUT pair can be controlled independently and constitutes a test channel.

The role of the load part is only to supply the desired shape current to the DUTs through the load inductors. For this purpose, a control system is used to regulate the shape and level of the current in each channel. The test bench is capable to deliver square current waveforms (from few amps until ±500A), sinusoidal currents (until 500A peak current and from DC to 500Hz) and more complex currents as a combination of a square and sinusoidal waveforms.

Independently, in the "DUT part", the devices can be tested with any desired gate control strategy with switching frequency until 500 kHz (depending on the gate drivers) and with duty cycles from 1 to 99%.

The sequence instructions can be modified every millisecond allowing to change the type of cycle at this frequency and to play very complex cycles. The two parts are controlled by a compactRio system from National Instruments. The overall system is managed and monitored through a LabView interface. All parameters are monitored through the high-speed data acquisition system SIRIUS-HS from Dewesoft.

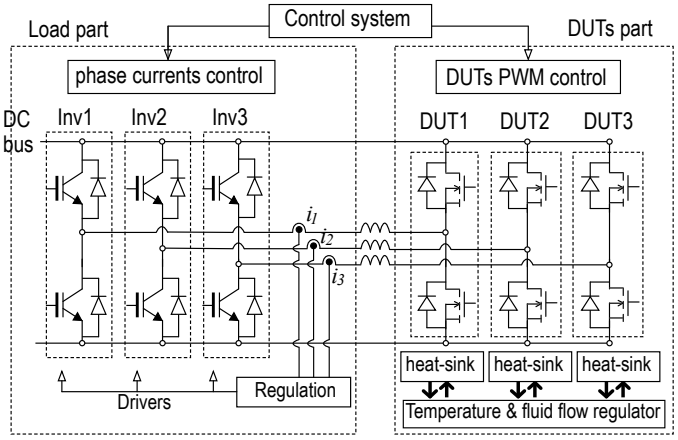

Fig. 2. Switching mode power cycling scheme.

The devices used in the "Load part" have a higher nominal power than the DUTs in order to greatly reduce their own stresses and that they remain reliable. The tested devices are cooled through heat-sinks using a thermoregulator with cooling fluid.

C. Devices under test

The devices under test are six-pack (3 phase inverter) 150A-1.2kV IGBT modules, not fully described here for confidentiality reason. Only one leg (the central one) in each module has been tested. The figure 3 shows a photo of the tested leg layout.

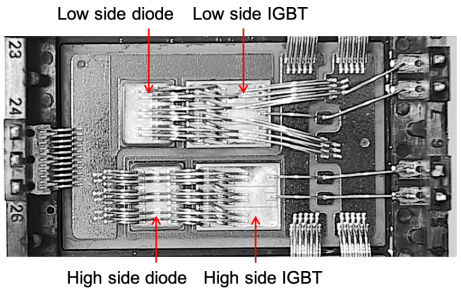

Fig. 3. Tested leg layout of the DUTs.

D. Experimental test conditions and results

Power cycling were performed in both modes DC and switching in comparable thermal stress conditions (ΔT_J).

As already said, in DC mode the junction temperature swing (ΔT_J) is controlled by the load current (I_L) and by the heating time (t_{on}). In DC mode, the test conditions where ΔT_J = 110°C with T_{Jmin} = 30°C and ON/OFF durations: t_{on}/t_{off} = 3s/6s. In order to reach this temperature swing with this pulse durations, the load current has been set to I_L = 150A.

In switching mode, the same ΔT_J can be obtained by practically the same total losses. But these total losses can be obtained by different contributions between conduction and switching losses. For the tests in switching mode, we have chosen to keep the same rectangular waveform of the load current (phase current) as in DC with the same t_{on} and t_{off} parameters (t_{on} = 3s, t_{off} = 6s). As there is a contribution in switching losses, the RMS load current is necessarily smaller than in DC mode during the heating time (t_{on}) and will depend on the switching frequency (f_{sw}) and duty cycle (η). These two last parameters have been set to f_{sw} = 15kHz and η = 90%. The

choice of the frequency is linked to a compromise so that the weight of the switching and conduction losses remains approximately balanced in the IGBTs. Concerning the duty cycle value, it has been chosen in order to favor aging of IGBTs rather than diodes (90% conduction time in IGBTs, 10% in diodes). Thus, the power cycling undergone by the diodes remains negligible comparatively to IGBTs. The choice of duty cycle depends on the accelerated aging objectives. In our case, the aging of the IGBTs has been favored rather than that of the diodes, but it is also possible to do the opposite or, for example, to choose duty cycles which make it possible to homogenize the thermal stresses between the switches and the diodes.

The common test conditions for both DC and switching modes as well as the control parameters used to reach these conditions are given in table I.

TABLE I: POWER CYCLING TEST CONDITIONS

Common test conditions	Control parameters to reach the same stress test conditions	
	DC mode	switching mode
t_{ON} = 3s t_{OFF} = 6s ΔTj = 110°C T_{jmin} = 35°C	I_L = 150A	$I_{L\,(phase)}$ = 100 A f_{sw} = 15kHz η = 90%

During the aging test, the main degradations and failures occur at the bondwire contacts on the high-side IGBT for both tests. The collector-emitter voltage (V_{CE}) is used as aging indicator and the aging criterion is when the relative change in V_{CE} reaches 5% increase. As results, it can be seen in figure 4 the relative variation of V_{CE} for the 4 IGBT samples tested in DC mode in the top graph and for the 3 samples tested in switching mode in the bottom graph.

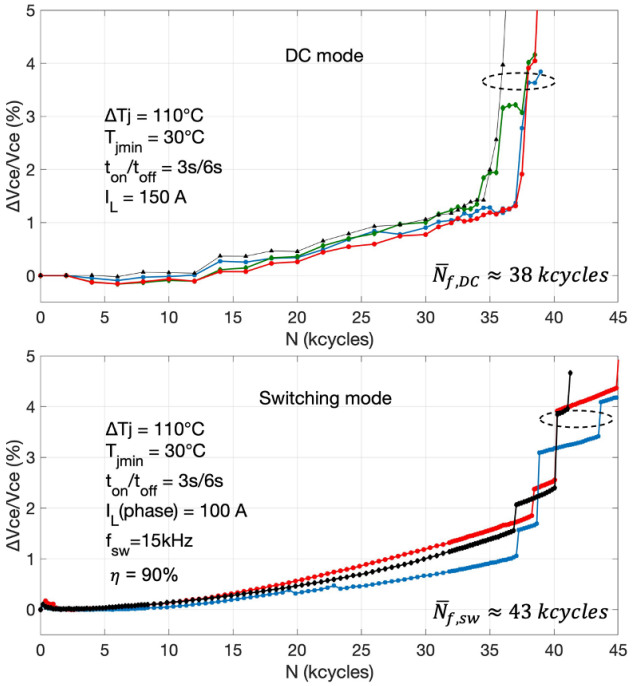

Fig. 4. Power cycling test results.

It can be observed similar trends for both tests. A gradual increase to about 1% to 1.5% due to a process of progressive cracking of the wire contacts, followed by a sudden increase which reflects bond-wires lift-off. The number of cycles to failure (N_f) reached at 5% increase in V_{CE} is between 35 and 40 kcycles in DC-mode (mean value $\bar{N}_{f,DC} \approx 38$ kcycles) and between 40 and 45 kcycles in switching mode (mean value at $\bar{N}_{f,sw} \approx 43$ kcycles).

In order to understand what should be the cause of the difference in lifetime, we performed a numerical comparison in thermal and mechanical stresses between the DC and the switching mode using a strong coupled electrical-thermal-mechanical analysis.

It should be noted that only cracks of the bonding wire contacts and bond-wires lift-off was observed during these tests. In particular, no solder delamination occurred in the tested samples. The degraded bonds being those numbered in figure 5, and particularly the center contacts (#3 and #4).

III. MODELLING THE DC AND SWITCHING AGING MODES

A. Description of the FE model

Only the central leg has been tested and only bond-wire lift-off occurred in experimental tests. Consequently, the zones of interest are at the level of metallization and contacts with the bonding wires of the corresponding substrate. The lateral substrates therefore have no significant thermomechanical influence and can be avoided in the numerical model for simplification reasons. The model is shown in fig.5.

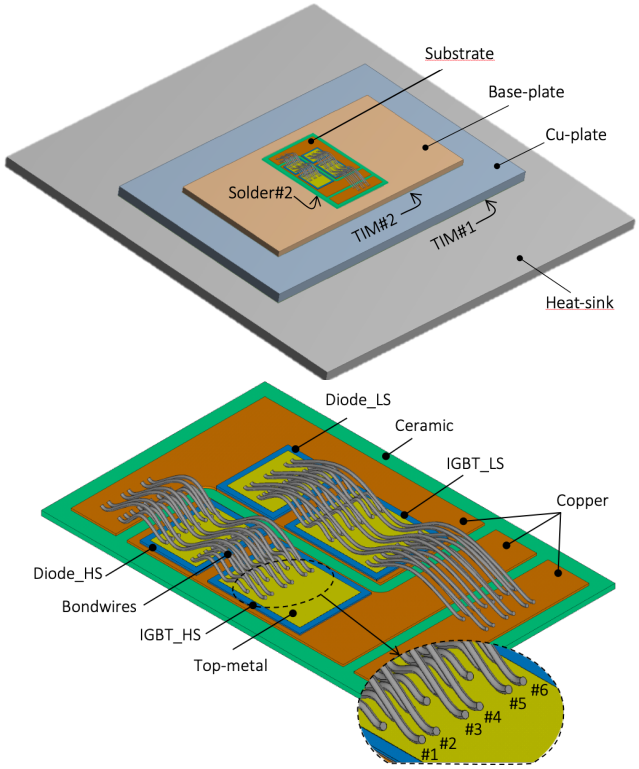

Fig. 5. Geometry of the FE model.

The power module is made-up of the central substrate which is attached by a solder layer (solder#2) on a copper base plate. This latter is mounted on an aluminum heat-sink. A copper plate is inserted between the heat-sink and the power module as for experimental tests to reach high temperature variations. Two

thermal interface materials (TIM) layers are used, as shown in fig.5, to ensure the thermal contact between the base plate and copper plate and between the copper plate and the heat-sink.

The geometrical model of the substrate is detailed in the bottom part of fig.5. Both the high side and low side IGBTs and diodes are taken into account with their thin top-metal layers covering the active areas of the chips. A direct copper bond (DCB), with an aluminum nitride (AlN) ceramic, is used as substrate where the four chips are attached on copper patterns. Since the main degradations are observed at the contacts of the long bondwires at the center of the HS-IGBT, these contacts are numbered from #1 to #6. All materials, with their dimensions, are given in table II and the material properties in table III.

TABLE II: DIMENSIONS AND NATURE OF MATERIALS

Parameter	Material	Thickness (µm)	Dimensions (mm x mm)
Bondwires	Aluminum	∅ 390µm	-
Top-metal (IGBT)	Aluminum	10	11 x 8.2
Top-metal (diode)	Aluminum	10	6.2 x 8.2
IGBTs	Silicon	130	12.4 x 9.6
Diodes	Silicon	250	7.6 x 9.6
Solder1	$Sn_{96.5}Ag_{3.5}$	100	see diode/IGBT
Patern	Copper	250	-
Ceramic	AlN	635	46 x 30
Pattern	Copper	250	45 x 28
Solder2	$Sn_{96.5}Ag_{3.5}$	300	45 x 28
Base plate	Copper	3000	120 x 60
TIM2	Thermal grease	50	120 x 60
Plate	Copper	5000	160 x 100
TIM1	Thermal grease	50	160 x 100
Heat-sink	Aluminum	5000	200 x 200

TABLE III: MATERIAL PROPERTIES

	Al	Si	Cu	AlN	SnAg	Thermal grease
Density	2700	2330	8930	3300	7360	-
Thermal cond. ($W.m^{-1}.K^{-1}$)	237	150	400	170	55	1.5
Specif. Heat ($J.Kg^{-1}.K^{-1}$)	900	710	390	720	240	-
Electrical Resistivity (Ω.m)	28.10^{-9}	Anisotrop	17.10^{-9}	1.10^{11}	12.10^{-9}	1.10^{5}

Concerning the electrical behaviors of IGBTs and diodes:

- *In DC mode:*

During the heating phase, only conduction losses in IGBTs are considered by Joule effect. If we consider the IGBT chips, the power losses are calculated as following:

$$P_{cond}(T_j) = V_{CE}(T_j)\, I_c \tag{1}$$

In this relation, the temperature dependance of V_{CE} is obtained from the data-sheet:

$$V_{CE}(T_j) = k_1(T_j)\, I_c^{k_2(T_j)} + k_3(T_j) \tag{2}$$

with:

$$\begin{cases} k_1(T_j) = 3.52 \times 10^{-5}\ T_j + 0.02182 \\ k_2(T_j) = 2.64 \times 10^{-4}\ T_j + 0.7394 \\ k_3(T_j) = -1.13 \times 10^{-3}\ T_j + 0.7796 \end{cases} \tag{3}$$

In these relations, T_j is in °C, V_{CE} in Volts, and I_C in Amps. As these relations come from the manufacturer's data-sheet, they are a first approximation.

In the FEM tool used (ANSYS Multiphysics), it is not possible to simulate the physics of operation of semiconductor devices. These ones are considered as conductive layers with anisotropic resistivities. Since IGBT chips can be considered as multiple elementary IGBT cells in parallel, the current flows only in the vertical axis (i.e. through the thickness of the dies). So, in order to simulate such "vertical" conduction, the in-plane resistivities data input for IGBT layers are supposed infinite, whereas the vertical resistivity is fitted in order to have the same on-state voltage and thus the same dissipated power in the heating phase than in experiments:

$$\rho_z(T_j) = \frac{V_{CE}(T_j)}{I_{RMS}} \frac{S_a}{L_z} \tag{4}$$

Where L_z is the thickness of the IGBT chip, S_a is its active area and I_{RMS} is the RMS current flowing through the device. This is to have the same dissipated power in the heating phase than in experiments.

- *In switching mode:*

The approach consists in calculating the conduction losses in IGBTs and in generating switching losses within all chips (diodes and IGBTs). The conduction losses are calculated by Joule effect by using RMS current (like a DC current) through the electrical path. Switching losses are generated in a volume that represents the space charge region within the power dies, where electric field will develop during transient process. In practice, the heat generation volume is considered as a slab within the chips having the same active area and with a thickness corresponding to 80% of the chip thicknesses (see fig.11).

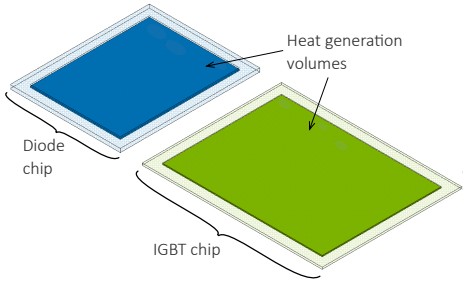

Fig.6: Heat generation volumes within the chips for switching power dissipation

If the measured current in a phase leg is $I_{L(phase)}$ and considering the 90% duty cycle for IGBTs, we can assume that the RMS currents through the chips can be written as :

$$\begin{cases} I_{RMS-IGBT} = I_{L(phase)}\sqrt{90\%} \\ I_{RMS-\mathrm{Diode}} = I_{L(phase)}\sqrt{10\%} \end{cases} \tag{5}$$

The IGBT switching losses are calculated as following:

$$P_{sw}(T_j) = (E_{ON} + E_{OFF})\, f_{sw} \tag{6}$$

where f_{sw} is the switching frequency, E_{ON} and E_{OFF} the switching energies at turn-on and turn-off. These parameters

and their temperature dependancy have been extracted from the data sheet:

$$\begin{cases} E_{ON} = \alpha_0 + \alpha_1 I_L + \alpha_2 I_L^2 + \alpha_3 I_L^3 \\ E_{OFF} = \beta_0 + \beta_1 I_L + \beta_2 I_L^2 + \beta_3 I_L^3 \end{cases} \quad (7)$$

with
$$\begin{cases} \alpha_0(T_j) = 1 \times 10^{-2}\ T_j - 5.14 \times 10^{-1} \\ \alpha_1(T_j) = 4.76 \times 10^{-5}\ T_j + 8.336 \times 10^{-2} \\ \alpha_2(T_j) = 3.296 \times 10^{-6}\ T_j - 7.876 \times 10^{-4} \\ \alpha_3(T_j) = -1.312 \times 10^{-8}\ T_j + 4.6 \times 10^{-6} \end{cases} \quad (8)$$

and
$$\begin{cases} \beta_0(T_j) = 9.32 \times 10^{-3}\ T_j + 3.95 \times 10^{-1} \\ \beta_1(T_j) = 4.44 \times 10^{-4}\ T_j + 9.55 \times 10^{-2} \\ \beta_2(T_j) = -1.52 \times 10^{-7}\ T_j - 6.933 \times 10^{-4} \\ \beta_3(T_j) = -6.76 \times 10^{-9}\ T_j + 3.372 \times 10^{-6} \end{cases} \quad (9)$$

In these relations, E_{ON} and E_{OFF} are in mJ, I_L in Amps and T_j in °C.

In the numerical analysis, the junction temperature (T_j) is computed as the mean temperature value over the active area of the high side IGBT. As electrical boundary conditions, it was injected the following currents, close to the experimental ones: 150A in DC and 94A RMS current in switching simulation in order to generate the conduction losses by Joule effect. In switching mode, during the heating phase (t_{on}) it was inserted an additional power density generation in the volume shown in fig.6 corresponding to the switching losses at 15kHz switching frequency. This latter dissipated power is calculated using eq(6), by taking as input the current level, the DC voltage (600V) and the local temperature in the chip. As thermal boundary conditions, the cooling process by fluid-flow was represented by a convective coefficient of h = 3000 W/m^2.K and a bulk temperature of 30°C. All other boundaries are considered as adiabatic.

B. Simulation results

As results, one can observe in figure 7 the temperature distributions on the top side of the power chips in both cases at the end of the heating phase (t = 3s), i.e., at T_{jmax}.

As expected, the temperature distributions in the high side IGBT are practically the same in both cases. The analysis is focused on the HS-IGBT because the observed degradations and failures are in this chip. As the dissipated power in the DC case is only in conduction, the current flowing through the bonding wires is higher than in the switching case. This leads naturally to higher temperatures supported by the bond wires in the DC case.

This is visible in figure 8 where it can be seen the temperature distribution along a central wire (#3) at the end of the heating time (t = 3s) for both cases. Since the load current generates also joule effect inside the wires, in the DC case, the maximum temperature in the wire is higher than the maximum temperature in the chip surface. Since the RMS current in the switching mode is lower than in DC mode, this effect is much less visible.

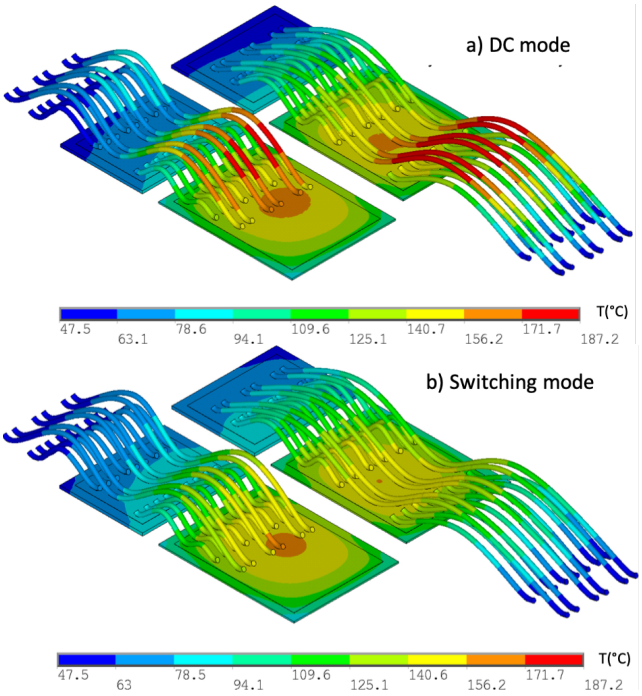

Fig.7. Comparison of results in temperature distribution between a) DC and b) switching modes (ΔT_j=110°C, t_{on}=3s, T_{Jmin} =30°C).

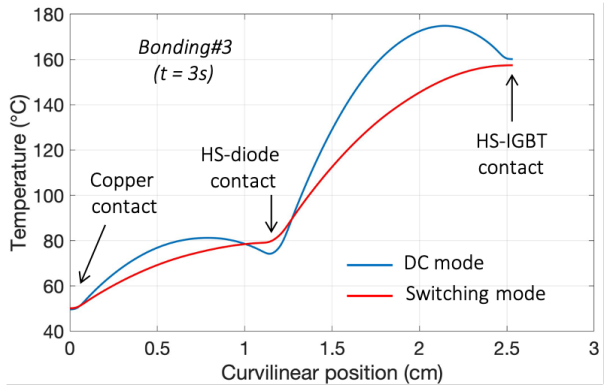

Fig.8. Temperature distribution along wire#3 at t = *3s*.

The figure 9a shows the junction temperature evolutions (T_{J_DC}, T_{J_sw}) during a power cycle. As already said, these junction temperatures are the mean temperatures over the chip area at each instant. The figure 9b gives the dissipated powers (P_{DC}, P_{tot_sw}) respectively in DC mode (blue curves) and in switching mode (red curves). The fig.9b gives also the contributions of switching losses (P_{sw}) and conduction losses (P_{cond}) in the switching mode. As expected, practically the same ΔT_J is reached for both modes. It can be observed that during the heating time, overall, the T_J in switching mode remains below that in DC, even if at the end there is a catch-up to reach the same final value. The cooling curves are identical.

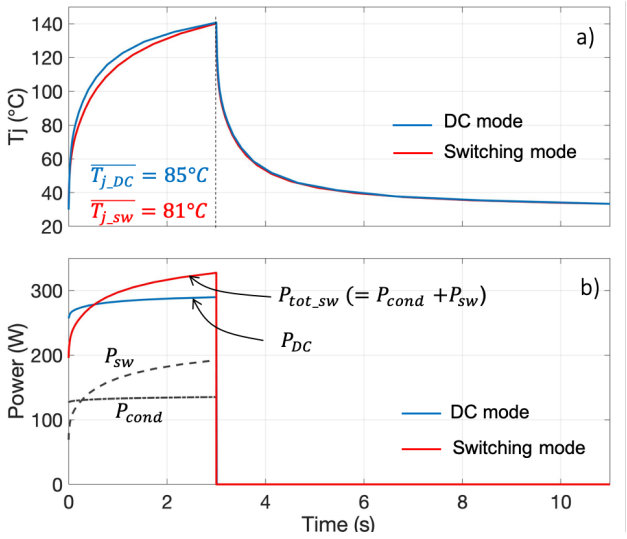

Fig.9. A power cycle simulation result in a) junction temperature, b) dissipated power

This is due to the fact that the switching losses are much more dependent on the junction temperature (T_j) than those in conduction. This is visible in figure 9b where one can see the conduction losses, for the two modes, reaching a quasi-stabilized value increasing only slightly because of the increase in T_j. Thus, at the beginning of the heating period, the losses in switching mode are lower than those in DC, while at the end it is the opposite. The average losses being almost identical. This explains the different growth rates of T_j in the two modes. This makes an observed difference of 4°C between the mean T_j values over the heating period, $\overline{T_{J,DC}}$ = 85°C and $\overline{T_{J,sw}}$ = 81°C.

The figures 10 and 11 show the temperature distributions in the top-surface of the metallization of the HS-IGBT respectively in transversal direction (just under the bond contacts) and in diagonal direction. These temperatures shouldn't be confused with chip temperature just below.

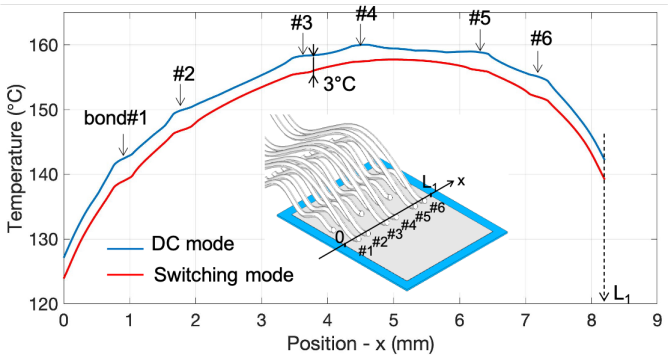

Fig.10. Temperature distribution of the top surface metallization along the transversal line (under the bondwire contacts) at t = *3s*.

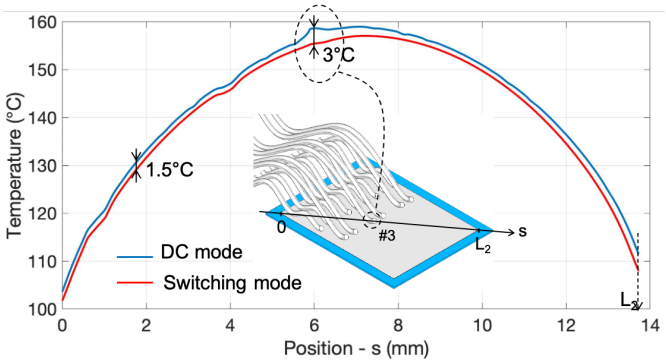

Fig.11. Temperature distribution of the top surface metallization along the diagonal line at t = *3s*.

These results show that at the metallization surface, the temperature is very slightly lower by about 1.5°C in switching than in DC mode. Furthermore, we find that the areas in contact with the bondings are hotter due to the Joule effect in these wires which increase the temperature at these contacts. The difference here is around 3°C between the two modes. This observed difference in thermal stress in the bondwire contacts, especially in the long wires of the HS-IGBT may explain the difference in observed lifetime between DC and switching tests.

We now propose to evaluate the impact of the difference in thermal stresses in the two tests on the lifetime and to corroborate the experimental observations given in figure 4. This difference is given by the mean value of junction temperature during the heating time which is δT_j = 4°C (see fig.9). For this end, we need the stress-life curve variation around ΔT_J=110°C. For this purpose, Table IV gives power cycle test results in DC mode for ΔT_J = 100°C and 90°C conditions, each test condition has been tested with 4 DUTs. The lifetime of each DUT in each condition is visible in the 3rd column.

TABLE IV: PCT RESULTS IN DC MODE

ΔTj (°C)	Ic (A)	Nf (kcycles)	Nf mean value (kcycles)
90	135	[78 72 75 72]	74
110	150	[38 36 38 39]	38

Around these two values of ΔTj, the following Coffin-Manson relationship can be written: $N_f(cycles) \approx A \cdot \Delta T_j^{-m}$, where $A = 2.27 \times 10^{11}$ and $m = 3.32$. The increase in lifetime $N_f + \delta N_f$ due to a small decrease in thermal stress $\Delta T_j - \delta T_j$ around ΔT_j=110°C can be deduced from a limited Taylor series expansion, with $\delta T_j \ll \Delta T_j$:

$$\frac{N_f + \delta N_f}{N_f} \approx \left(\frac{\Delta T_j - \delta T_j}{\Delta T_j}\right)^{-m} \approx 1 + m\frac{\delta T_j}{\Delta T_j} \qquad (10)$$

$$\Rightarrow \quad \delta N_f \approx m\frac{\delta T_j}{\Delta T_j} N_f \qquad (11)$$

From DC results: $N_f = 38$ kcycles at $\Delta T_j = 110°C$, a

decrease in thermal stress of $\delta T_j = 4°C$ in switching mode, leads to a lifetime increase of $\delta N_f \approx 5$ kcycles. This is consistent with the difference in the mean values observed in PCT results in figure 7.

As additional results, fig.12 shows the Von Mises plastic strain distributions at the contact faces of the bondings #3 and #4, for both cases at the end of heating phase (t=3s). The higher level of plastic strain in DC mode is probably due the small difference in ΔT at the contact locations, about 3°C, visible in fig.10. This is consistent with the experimental results.

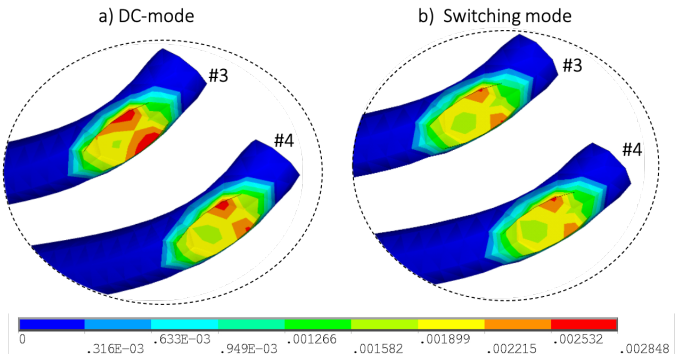

Fig.12. Von Mises plastic strain at the contact faces of bondings #3 and #4 at the end of heating phase (t=3s).

IV. Conclusion

The objective of this paper was to highlight the differences in thermal stress suffered by IGBT power modules during power cycling tests in DC mode and in switching mode.

First, it was found that switch mode power cycle tests do not reveal different failure modes or degradations from DC test modes. From a certain point of view, switching tests validate DC mode testing approaches. Nevertheless, it was found that for the same ΔTj test conditions, due to the higher load current required in DC mode, the bond wires are much more thermally stressed and the bond wire contacts experience a slightly higher ΔT than compared to the switching mode. As results, for same ΔTj stress, the switching mode leads to a slightly higher lifetime. Comparisons of this type are among the earliest in the literature and need to be confirmed by further work.

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