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## FAULT RIDE THROUGH OF DC SOLID STATE TRANSFORMER IN MEDIUM VOLTAGE DC SYSTEMS

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### ABSTRACT

Medium voltage direct current is emerging in distribution and collection networks and the network codes are under construction. This article introduces the MVDC network fault ride-through (FRT) requirement and the response of a DC solid state transformer is analyzed. A novel control of the DC SST suitable in the MVDC PV collection network is proposed. The controls of the boost MPPT converter and the isolated DC-DC converter include a normal operation mode and an FRT mode without any additional hardware circuit components. The performance of the proposed solution is demonstrated in simulation.

### INTRODUCTION

Direct current (DC) systems have been implemented for decades in high voltage DC (HVDC) transmission and railway electrification. Low voltage DC (LVDC) systems can be found in some public and industrial applications including native DC power sources and loads (datacenters, lighting, electric drives, electric vehicle charging etc.). LVDC has been extensively researched for microgrids [1]. Medium voltage DC (MVDC) systems have been researched and implemented in some pilot projects [2], [3]. One can consider that these currently independent DC systems will be eventually connected to form a DC network. The key enabling technology for such a DC network is a DC-DC converter also known as a DC solid state transformer (DC SST). The DC SST fulfills the role of a conventional transformer in AC networks: it adapts the voltage levels, provides galvanic separation and it can limit fault currents. However, the DC SST offers even more: it provides full power control, it breaks fault currents and it is smaller and lighter than a conventional transformer.

This article addresses an MVDC collection network for a photovoltaic (PV) power plant. A comparison of the MVDC architecture to the conventional MVAC architecture is presented in Figure 1. The AC transformers are replaced with DC SSTs. The DC SST offers a noticeable size reduction while maintaining the same energy efficiency as the conventional transformer [4]. Moreover, smaller size results in reduced CO<sub>2</sub> footprint for manufacturing and installation. DC transmission offers

lower power losses [5]. Moreover, cost savings in cables are expected because 2 wires are used in DC instead of 3 in AC (with the same wire cross-section). These present a major advantage in high-power (multi-megawatt) applications where long-distance (tens of kilometers) transmission is required. Multiple PV inverters in AC are replaced in DC with a single multi-megawatt inverter interfacing with the AC grid. The single inverter provides support to the AC grid, for example with reactive power.

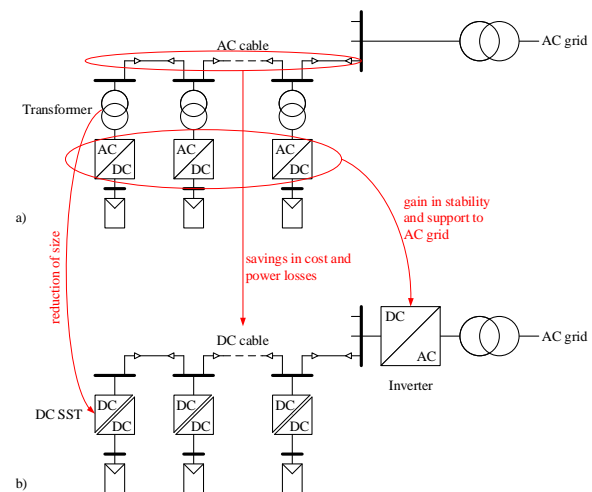


Figure 1: MVAC (a) and MVDC (b) collection network for PV power plant highlighting the structural differences and benefits of MVDC

CIGRE and CIRED have provided some foundations for the MVDC network development [6]–[8] and some further investigations are ongoing, also involving IEEE and IEC. Even if the MVDC network codes are still under construction, one can expect that they will be similar to the AC network codes. This article focuses on the fault ride-through (FRT) requirement (also referred to as under-voltage ride-through or low-voltage ride-through), a common feature in AC systems. The response of the DC SST is analyzed.

The control of DC SST must ensure that in case of a voltage dip at MVDC terminals, the voltage of the LVDC bus remains stable [9]. Control for FRT of a DC-DC converter based on an isolated boost converter is presented in [10]. An inductor is added at the output, on the MVDC

network side, to reduce the speed of discharge of the output capacitor during FRT. This gives time for the control to react. Most of the proposed solutions for achieving FRT with DC SSTs rely on the addition of hardware circuits on the medium voltage grid side of the converter [11]–[13]. In this paper, the selected topology is inherently robust to network faults [14], which enables only adding new control algorithms and no additional hardware.

## FAULT RIDE THROUGH REQUIREMENTS

### Existing AC network

Any electrical equipment must comply with regulations and standards. Fault ride-through (FRT) is one of the requirements applicable to grid-connected generators. FRT ensures that in case of a fault in the network, the power system remains stable. While the network protection clears the fault, power generators stay connected and they restart as soon as the voltage is back. The FRT requirement applies to AC grid-connected converters, including PV. The converter must stay connected in the event of a dip in the AC grid voltage. The voltage levels, time to recover full production, and voltage ramp differ according to local regulations [15]. Figure 2 gives an example of the French DSO Enedis FRT profile [16]: after a voltage dip, the power generation of a unit must come back to its prior level as quickly as possible once voltage has recovered 85% of the nominal grid voltage. It is recommended that the converter provides some reactive current during the FRT.

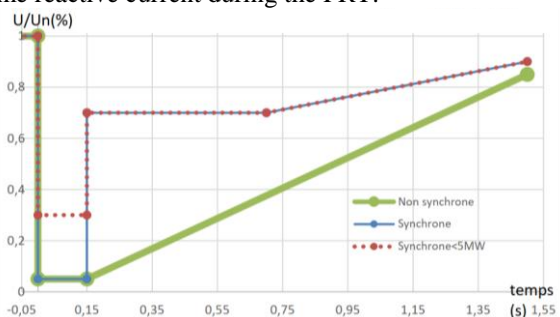


Figure 2: FRT profile defined by the French DSO Enedis [16]

### Future DC network

The regulations and standards for DC networks, including MVDC, are still under construction. One can expect that they will be similar to those of AC networks. In particular, the authors expect that the FRT requirement in MVDC and AC networks will be similar. In this article, it is assumed that the MVDC FRT profile is the same as in AC (Figure 2).

The FRT profile depends on the protection strategy of the MVDC network. In the case of an MVDC short circuit, all generators, converter-interfaced AC grid, and capacitors contribute to the fault current which rises rapidly [17]. The use of fault-blocking converters was studied in [18], [19] to limit the steady-state fault current. In [20], the radial MVDC system was protected by means of a current-limiting device. The authors proposed in [21] the

protection of radial MVDC network based on a single DC circuit breaker (DCCB) and multiple DC fuses (Figure 3). An example of a situation that requires the DC SST FRT is in the case of a DC pole-to-pole short circuit at MVDC terminals of the DC SST 2 (Figure 3). The adjacent DC fuse breaks while all other DC SSTs and DC-AC must remain connected during the transient voltage dip.

During the FRT profile (Figure 2), the authors assume that the DC SST should provide some current to allow the protection system to identify the fault. The value of the current during the FRT profile is expected to be  $\leq 1$  p.u. The DC SST should restart the power transfer as soon as the MVDC voltage is back.

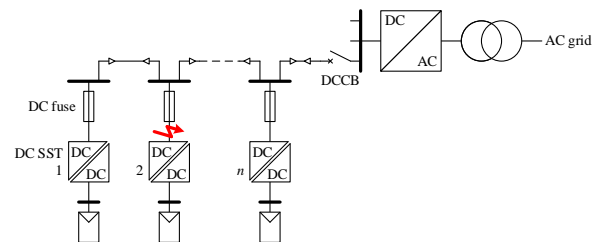


Figure 3: Protection of radial MVDC network based on a single DC circuit breaker (DCCB) and multiple DC fuses [21]. An example DC pole-to-pole fault location at MVDC terminals of DC SST 2 is presented.

## CASE STUDY MVDC NETWORK AND DC SST TOPOLOGY

A  $\pm 10$  kV medium voltage DC radial collection network is selected for a PV power plant rated at 20 MW. The PV strings are at 1.5 kV (maximum open circuit voltage). There are multiple DC SSTs distributed along the collection network (Figure 1b), each rated at 250 kW and interfacing with multiple PV strings. The DC SST includes multiple boost converters for maximum power point tracking (MPPT) and one isolated DC-DC converter for voltage step-up and galvanic separation (Figure 4).

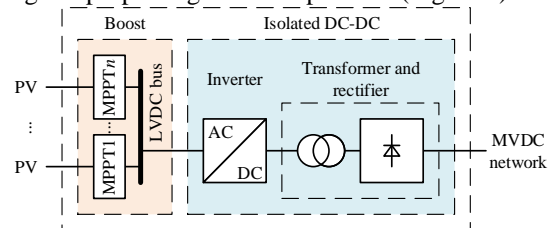


Figure 4: DC solid state transformer for MVDC PV application including multiple boost converters and a single isolated unidirectional step-up DC-DC converter

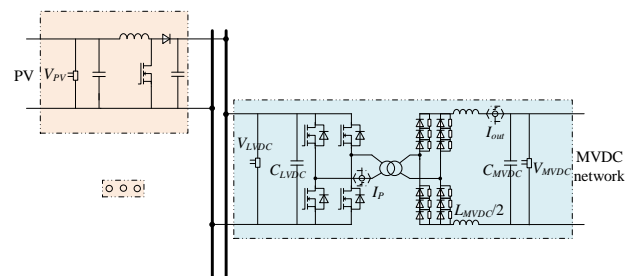


Figure 5: Circuit diagram of the boost and isolated DC-DC converter, with the definition of controlled quantities

The phase-shifted full bridge (PSFB) topology is selected for the isolated DC-DC converter (Figure 5). Indeed, it is shown in [14] that its output filter composed of an inductor and a capacitor is beneficial in case of faults on the MVDC network. The current discharging from the output capacitor  $C_{MVDC}$  is limited by the inductor  $L_{MVDC}$  inside the circuit and the diode rectifier is protected.

The MVDC network is realized with underground cables. The interface with the AC grid is ensured by a voltage-source inverter and a transformer. The MVDC network is in a symmetric monopole line configuration with high-impedance grounding. The PV network is not grounded.

### CONTROL OF DC SST FOR FRT

The control structure of the DC SST is separated between normal operation mode and FRT mode as presented in Figure 6. The switch between the modes is done by an under-voltage detection function. The FRT mode is activated when the MVDC network voltage is lower than 0.85 p.u. In each mode, the boost converters and PSFB have distinct roles.

In normal operation mode, the MVDC network voltage  $V_{MVDC}$  is controlled to a constant value by the central inverter. The PSFB regulates the LVDC bus voltage  $V_{LVDC}$  to a constant value, with disturbances from MVDC voltage and PV power variations. The boost converters achieve the MPPT function by adjusting their input voltage  $V_{PV}$  individually.

In FRT mode the control roles are reversed. The boost converter now regulates the LVDC bus voltage  $V_{LVDC}$  to a constant value. As explained in the Fault Ride Through Requirements section, the PSFB is expected to regulate its output current  $I_{out}$  close to its nominal value. This may not always be possible as the available PV power may not be sufficient to maintain a constant LVDC bus voltage and the nominal output current at all times. Thus, a maximum current tracker is implemented to give the reference to the current control. This ensures that the PSFB is controlling its output current as close as possible to its nominal value, while not interfering with the LVDC bus voltage control.

During the initial phase of the FRT, the decrease of the PSFB transformer secondary voltage leads to a fast rise of the primary current during the transition period where it is only limited by the leakage inductance of the transformer. The current dynamics of this period make it impossible to control and an overcurrent detection is thus necessary to protect the PSFB inverter. It is considered that this function is done by a desaturation protection [22] included in the gate drivers. The control pulses are stopped for  $N_{sw}=5$  switching periods when the protection is triggered. The current is still flowing at the secondary side because of the resonance between the output inductor and capacitor.

The PSFB LVDC bus voltage regulation is presented in detail by the authors in [23]. The PI controller is tuned according to the presence of resonance in the transfer function of the system, dictated by the voltage ratio and leakage inductance of the transformer.

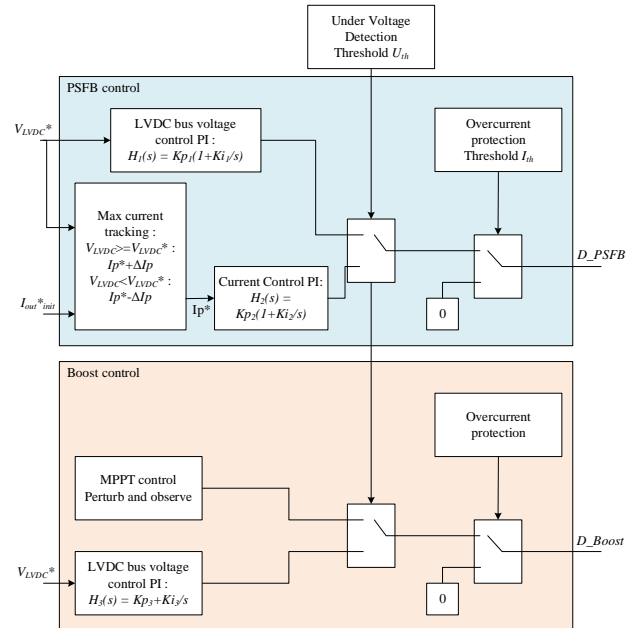


Figure 6: Control structure synoptic of the complete converter including Boost and PSFB converters

The PSFB current control is done with a PI controller based on the RMS current measured at the primary of the transformer  $I_p$ . A maximum current tracking function is added in order not to discharge the LVDC bus capacitor during an FRT event coinciding with low irradiance on the PV. Once the LVDC bus voltage drops below the reference level, the current control reference is incrementally decreased until the bus voltage can be maintained to its reference by the boost converter LVDC bus voltage control.

The MPPT control of the boost converter regulates the PV voltage so as to optimize the extracted power. The search for the voltage corresponding to this maximum power can be done through different algorithms largely discussed in the literature [24]. The “perturb and observe” algorithm [25] is selected for this particular implementation of the MPPT function.

The LVDC bus voltage control of the boost converter is done with a PI controller tuned to be slower than the current control of the PSFB, thus avoiding instabilities. The bandwidth of the Boost LVDC bus voltage control is tuned to a third of the PSFB current control.

### SIMULATION MODEL AND RESULTS

A simulation model is developed under Matlab Simulink Simpower System. The MVDC network is modeled with a voltage source, controlled to follow the FRT profile. The MPPT boost converter is considered a known state-of-the-art and modeled by a controlled current source, with a saturation corresponding to the maximum PV power available. The control of the boost converter acts on the reference current of this source. The PSFB converter is modeled in detail with its switching components. The profile presented in Figure 2 is accelerated (the entire event fits within 14 ms) to keep a reasonable simulation time

using the switching model. The main parameters used for the simulation are given in the table below.

Table 1: Parameters used in the simulation

MVDC network	$P_{MVDC}=20\text{MW}$	$V_{MVDC}=\pm 10\text{kV}$	
DC SST	$P_{SST}=250\text{ kW}$	$V_{PVoc}=1.5\text{ kV}$	$C_{LVDC}= 250\text{ }\mu\text{F}$ $L_{MVDC}= 8\text{ mH}$ $C_{MVDC}= 200\text{ nF}$
FRT parameters	$U_{th}= 17\text{ kV}$	$I_{th}= 415\text{ A}$	$N_{sw}= 5$
PSFB LVDC bus control	$Kp_1= 3.4e^{-4}$	$Ki_1= 1.3e^4$	
PSFB current control	$Kp_2= 7e^{-4}$	$Ki_2= 1e^4$	$\Delta I_p = 200\text{ A/s}$
Boost LVDC bus control	$Kp_3= 5.3e^{-3}$	$Ki_3= 710$	

Two scenarios are studied, representing situations with high irradiance level and low irradiance level. The low irradiance level scenario translates to the boost not being able to regulate the LVDC bus voltage to a constant value if the PSFB is regulating its nominal current. The maximum current search of the PSFB control is activated in this scenario.

The blue curves in Figure 7 show the simulation results of the high irradiance level scenario. One can see that the LVDC bus voltage is regulated to 1 p.u. during the whole process with a deviation of 6% after the initial MVDC voltage dip. The initial output current increase after the voltage dip stays in the operating zone of diodes of typical rating for such a nominal current [26].

The red curves show the simulation results in a low irradiance scenario, with power at the PV side limited to

10% of the nominal power. This results in the PSFB supplying less current than in the previous case, so that the boost converter can maintain the LVDC bus voltage constant. A dip in the LVDC bus voltage can be observed at the moment the PSFB starts to transfer a current superior to the PV power limit, thus discharging the LVDC bus capacitor. The PSFB current is brought back down by the maximum current tracking control and the LVDC bus voltage is regulated to its nominal value. The slight bumps in the LVDC bus voltage and PV power are due to the way the maximum current tracking is done. As in the “perturb and observe” MPPT, there are constant perturbations in the control variable (here the reference current), causing little instabilities. Other algorithms could be explored to avoid this.

In both cases the output current is maintained to a level close to nominal right after the fault, enabling its identification, while the LVDC bus is kept at a constant voltage.

## CONCLUSION

FRT specifications are transposed from existing AC standards to the context of MVDC networks. A control for the FRT of a DC SST in an MVDC PV collection application is proposed. It relies on actions in both the boost and the step-up converter. No additional circuit needs to be added to achieve the FRT requirements. The proposed control strategy is validated in simulations.

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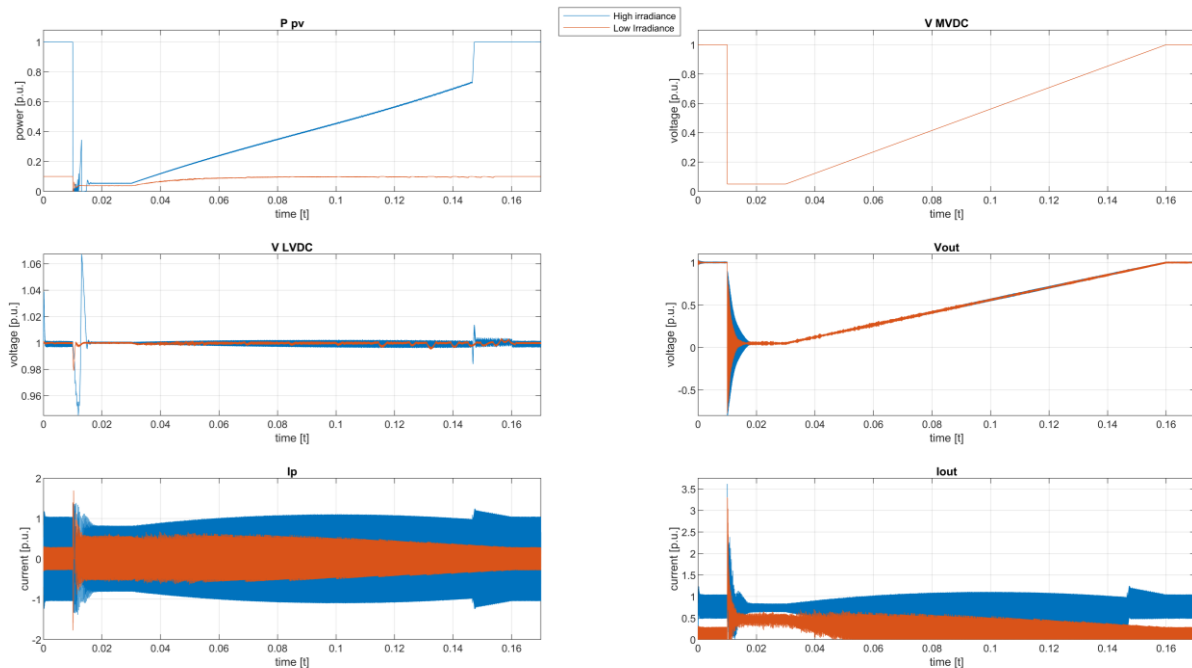


Figure 7: FRT process in high irradiance scenario (blue) and low irradiance (red)



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