Experimental Behavior of Single-Chip IGBT and COOLMOS Devices Under Repetitive Short-Circuit Conditions

Stéphane Lefebvre, Zoubir Khatir, F. Saint-Eve

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Abstract

This paper presents the behavior of single chip IGBT (Insulated Gate Bipolar Transistors) devices under repetitive short-circuit operations. 600V and 1200V NPT (Non Punch Through) IGBTs as well as 600V COOLMOS^{TM} have been tested. The repetition of these severe working conditions is responsible for devices ageing and results unavoidably in the components failures. A serial of experimental tests was made in order to determine the number of short circuit operations the devices can support before failure for different dissipated energies. The temperature influence has been also investigated. Results show two distinct failure modes depending on the dissipated energy during the tests. A critical value of short-circuit energy has been pointed out which separates these failure modes. Experimental and numerical investigations have been carried out in order to analyse these failure modes. A detailed analysis of the physical mechanisms occurring during the short-circuit failures for dissipated energies equal or lightly higher than the critical value is presented.

Index Terms

IGBT, COOLMOS^{TM}, short-circuit, power devices, thermal runaway, thermal modeling, reliability.

I. Introduction

Power semiconductor devices may suffer of extremely hard working operations, resulting from an accident in the case of short-circuit conditions, depending on the application circuit and its environment. So, it is of the first importance to carry out investigations on the behavior of power devices under such severe repetitive working operations. Especially, the questions which are still in abeyance are :

- How many short-circuit pulses can support a given device before failure for given operating conditions ?

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S. Lefebvre is with the Conservatoire National des Arts et Metiers (CNAM) and SATIE laboratory, ENS de Cachan, 61, av. du President Wilson, F-94235 Cachan Cedex (phone: +33.1.47.40.21.08; fax: +33.1.47.40.21.08; e-mail: lefebvre@ satie.ens-cachan.fr).

Z. Khatir is with the French National Institute of Transport and Safety Research, 2, Av. Malleret-Joinville, F-94114 Arcueil Cedex, France (phone : (33).1.47.40.73.34; fax : (33).1.45.47.56.06; e-mail : khatir@inrets.fr).

F. Saint-Eve is with the SATIE laboratory, ENS de Cachan, 61, av. du Prsident Wilson, F-94235 Cachan Cedex (e-mail: saint-eve@satie.ens-cachan.fr).

- Can we observe any ageing effect on the devices and is there any electrical characteristic ageing criterion ?

Many papers have been published on the topic of the behavior of IGBT (Insulated Gate Bipolar Transistors) devices under single short-circuit conditions [1-6], but the influence of repetitive short-circuit operations in device lifetime and reliability have been studied only recently [7-10]. It has been reported that IGBT short-circuit failure mechanisms may be divided in four modes :

- Failure may occur near the peak current at the beginning of short-circuit [6,8]. This mode is called ”power limited failure”.
- Device may fail during the short-circuit [2]. This failure mode is called ”energy limited failure” and is the most often observed failure. It is due to overheating inside the device wich leads to thermal runaway.
- Failure may occur from some microseconds to several hundred of microseconds after a successful short-circuit turn-off [5-9].
- Finally, destruction may happen during the turn-off process after short-circuit pulse without destructive over-voltage. Yamashita *et al.* [**?**] have called this failure mode ”Inhomogeneous operation failure” and looks like dynamic latch-up [6,9].

In this paper, we describe results concerning the effect of repetitive short circuit conditions in the lifetime of IGBT devices and COOLMOS^{TM} transistors according to the dissipated energy level. 600V and 1200V NPT (Non Punch Through) IGBTs and 600V COOLMOS^{TM} transistors have been tested under two case temperature levels : 25^oC and 125^oC. In order to respond to the above questions, we have chosen to perform tests on single chip IGBT devices to avoid any problem linked to the energy distribution in multi-chip devices. Moreover each device under test (DUT) is subjected to repetitive short-circuit pulses with identical operating conditions until failure. Whatever the device or the case temperature, it has been observed only the three last failure modes described above. In this paper, we show that the second failure mode is the same as the third one which is only a limit case. Our experimental conditions (Type 1 short-circuit) did not allow to observe the ”power limited failure” mode. Especially, the last failure mode will be analyzed and discussed on the basis of experimental measurements and thermal simulations. It has been pointed out a critical energy which distinctly separate the above two last failure modes. The thermal runaway due to the positive feedback of heat generation by the leakage current of the device, which appears during the fourth failure mode, will be particularly detailed and discussed.

Even if these behaviors have been reported by some authors [6-8], we propose some hypothesis of the physical mechanisms that should be involved in the third failure mode. Especially, we show the dominating role of the diffusion component among the different components of the leakage current which takes place during the thermal runaway. The abrupt frontier between the two last failure modes is a limit case which should correspond to the critical short-circuit energy.

II. Experimental Protocols

A. Circuit description for short-circuit tests

Short-circuit conditions were produced with the test circuit presented in Fig.1. The devices under test are single chip devices in TO247 package and their main characteristics, voltage breakdown (V_{BR}) and collector current (I_C) at 25^oC are the following ones :

- 600 V NPT IGBTs from Infineon (SGW15N60), $V_{BR} = 600\ V$, $I_C = 31A$.
- 1200 V NPT IGBTs from Infineon (SGW15N120), $V_{BR} = 1200\ V$, $I_C = 30A$.
- 600 V COOLMOS^{TM} from Infineon (SPW20N60C2), $V_{BR} = 600\ V$, $I_C = 20A$.

The short-circuit energy is supplied by a set of capacitors and a circuit breaker (IGBT 1200 V - 400 A) allows to avoid the DUT explosion by an over-current detection (400 A). The device current is measured by a wide bandwidth (10Hz-30MHz) current probe developed in the laboratory, which has been optimised for high pulse current measurements. Measurements of the leakage currents after the opening of the short-circuit current are made by a coaxial shunt resistor (LEM $10\ m\Omega$). A personal computer, equipped with an input/output card, controls the DUT gate drive pulses. A repetitive cycle of 3 seconds is chosen in order to avoid the average overheating of the chip. Finally, a heating plate allows to consider the device packages temperature influence, especially at 25^oC and 125^oC. Short circuit operations are performed with a Gate to Emitter voltage equal to 15V. The influence of gate voltage (V_{GE}) was not investigated.

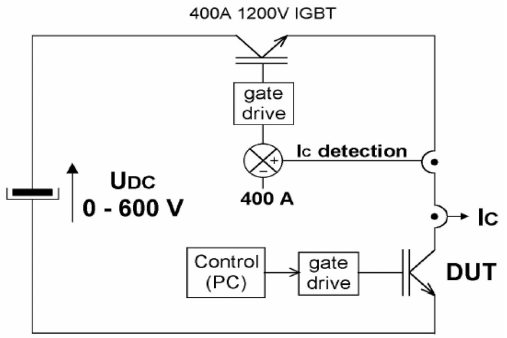

Fig. 1. Short-circuit test work-bench.

B. Test Protocol

In order to determine the origin of the device ageing during short-circuit operations, different electrical parameters have been regularly measured. All of them (forward voltage drop, threshold voltage, drain and gate leakage currents) have been measured for a junction temperature equal to 25^oC. Threshold voltage is measured for emitter current I_E = 1 mA, gate leakage current by a Keithley 6430 SMU and the collector leakage current I_{CES} is measured for a collector to emitter voltage equal to the breakdown voltage V_{BR} (600V or 1200V). In order to avoid self-heating, on-state voltage is measured for short time (10 μs) current pulse equal to the device specified current at 25^oC.

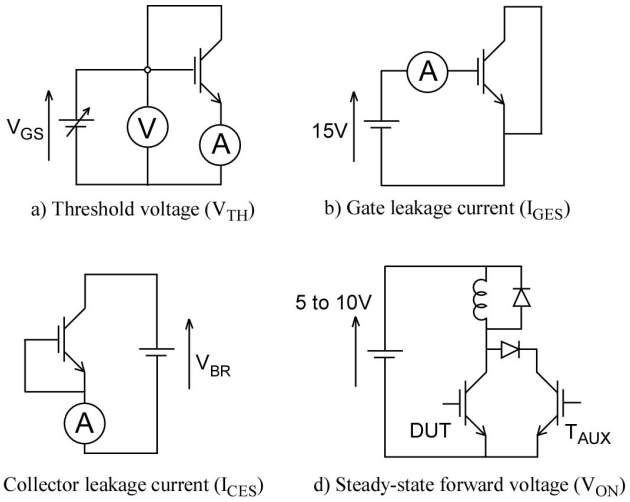

Fig. 2. Electrical characteristics measurements.

III. Experimental Results

For each repetitive short-circuit test, the same energy has been consumed by the DUT repetitively until destruction. We proceeded like this to many tests at different energy levels and package temperatures and we observed the number of cycles supported by the devices until failure. The dissipated energy is controlled by supply voltage U_{DC} of the test circuit and by the short circuit duration t_{SC}.

A. Short-Circuit Robustness

The obtained results, concerning the robustness in short-circuit repetitive conditions for SGW15N60 devices under 400 V at 25^oC and 125^oC case temperature are plotted in Fig.3. Similar results are presented in Fig.4 concerning the effect of short-circuit voltage on SGW15N120 devices at 125^oC, sustained voltages were 250 V and 540 V. It should be noted that the evaluated short-circuit pulse times are above specified value in the IGBT datasheets which is less than $10\mu s$ and from this point of view, the tested IGBT devices have shown robustness largely beyond their specifications. Fig.5 shows the obtained results for the tested COOLMOS^{TM} transistors.

In these Figures, each point is the result of repetitive tests on a given device, with on the X-axis the dissipated energy and on the Y-axis the number of short-circuit tests until destruction occurs. For all tested devices, it can be seen the same general behavior : just below a critical energy E_C, devices are able to support a very large number of short-circuit operations (up to 10000) and beyond which only one test leads to failure. For the critical energy, points are randomly distributed between 1 and about 10000. The critical energy E_C depends on the tested device and on test conditions (Table I). In order to compare these values, the critical energy density is also given in this table relatively to the device active areas.

The critical value (E_C) define clearly and abruptly two failure modes depending whether the short-circuit energy is greater or lower than this singular value.

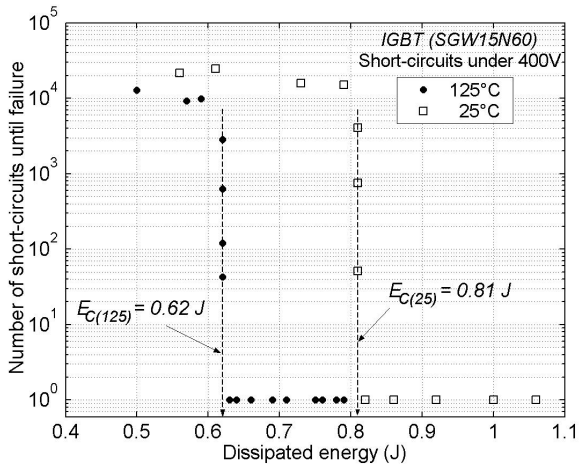

Fig. 3. Robustness in repetitive short-circuit conditions of 600V NPT IGBT (SGW15N60).

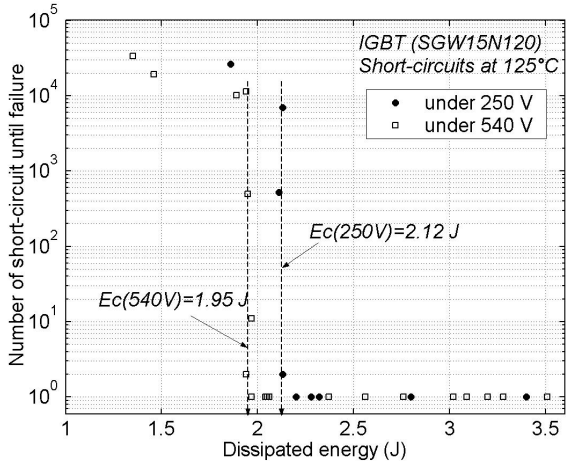

Fig. 4. Robustness in repetitive short-circuit conditions of 1200V NPT IGBT (SGW15N120).

B. Energies $E < E_C$

For short-circuit energies below the critical value ($E < E_C$), a large number of short-circuits is necessary to reach failure (Figs. 3 to 5). These results show that a cumulative damaging mechanism takes place which leads to an ageing effect and consecutively to failure after at least 10^4 short-circuit cycles. In these conditions, failures systematically appear at turn-off when trying to switch-off the short-circuit current (Fig.6) with a destruction phenomenon which looks like dynamic latch-up. These results occur to all the tested devices whatever their technology.

C. Energies $E > E_C$

As visible in Figs. 3 to 5, for short-circuit energies beyond the critical value ($E > E_C$), only one short-circuit is supported by the devices during which failure occurs. For high short-circuit durations, e.g. energies $E \gg E_C$,

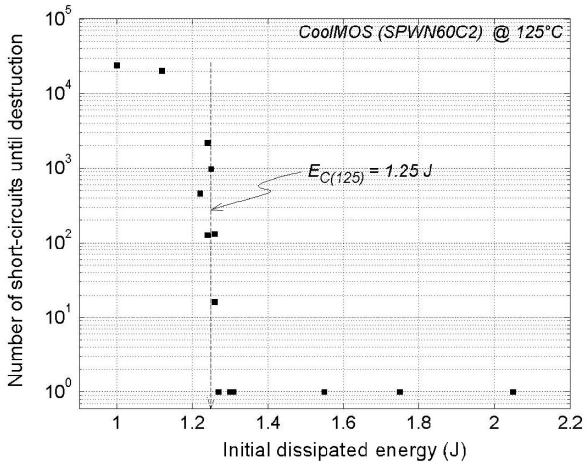

Fig. 5. Robustness in repetitive short-circuit conditions of 600V COOLMOS^{TM} transistor (SPW20N60C2).

TABLE I

MEASURED CRITICAL ENERGIES.

Devices	*Conditions*	*Crit. energy* $E_C(J)$	*Crit. energy density* $E_C^*(J/cm^2)$
600V NPT IGBT	T_c = 25°C	0.81	7.36
V_{cc} = 400V	T_c = 125 °C	0.62	5.64
1200V NPT IGBT	V_{cc} = 250 V	2.12	11.15
T_c = 125°C	V_{cc} = 540 V	1.95	10.25
600V	V_{cc} = 400V	1.25	6.9
COOLMOS	T_c = 125°C		

destruction appears during the short-circuit because of thermal runaway (Fig.7).

When the short-circuit energy is higher but close to E_C, at the first test, a tail current takes place after the turn-off process of the device and leads to a thermal runaway phenomenon. The failure occurs after a delay time (t_{df}) (see Fig.8) from the device switching off, which can vary from a few microseconds to several hundreds of microseconds, depending on test conditions. In the following, we will call this failure mode the ”delayed failure mode”. This phenomenon has been observed by some authors [5-9]. We observed that the initial tail current level (I_{lo}), just after the device is turned-off, and the delay time to failure (t_{df}) are energy dependent or more precisely device temperature dependent at the turn-off time. The higher the energy is, the higher the tail current level is and the shorter the delay time to failure is.

As illustration, Fig.9 shows experimental short-circuit current waveforms for SGW15N60 devices under 400 V at 125^oC and for different short-circuit durations. The longer t_{df} (120 μs) corresponds to the shorter t_{SC} (19 μs)

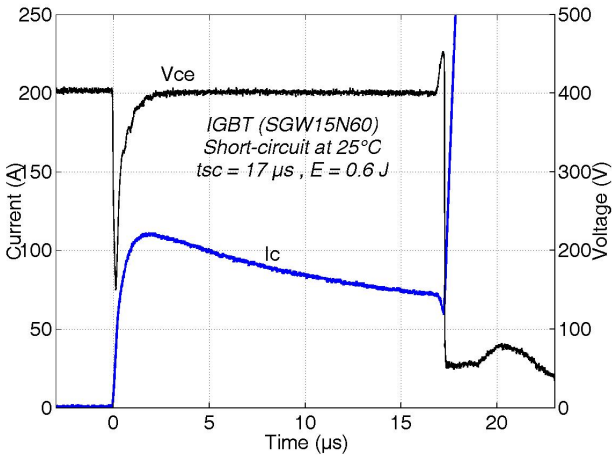

Fig. 6. Failure with $E < E_C$ conditions, example for a 600V NPT IGBT.

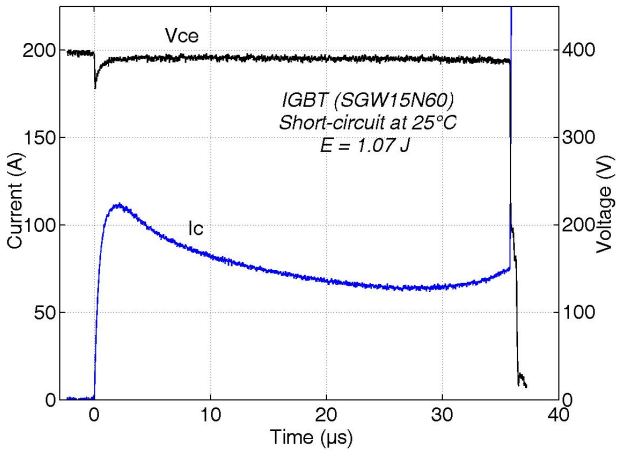

Fig. 7. Failure with $E \gg E_C$ conditions, example for a 600V NPT IGBT.

and the lower dissipated energy (0.63 J) to be compared to the critical value (0.62 J). On the contrary, the shorter t_{df} corresponds to the longer t_{SC} (25.5 μs) and the higher energy (0.76 J).

Fig.9 shows similar results concerning SGW15N120 devices under 540 V at 125^{o}C for different short-circuit durations. It can be seen in this figure, for the higher energy test (t_{SC} = 60 μs), that tail currents may be very high and the t_{df} tends to very short values. The limiting case should looks like the current waveform shown in Fig.7, where the short-circuit duration is too high for switching-off the device, which is out of control.

For both devices, results concerning the dependence between delay time to failure and the density of dissipated energy during short-circuit pulse are given in Fig.11. We can observe, for both devices, that the curves have vertical asymptotic limit corresponding to the critical values of energy density (E_C^*, see table I) for which t_{df} have the more important values. On the other hand, for high energy values, t_{df} tends to zero which is the limit case that

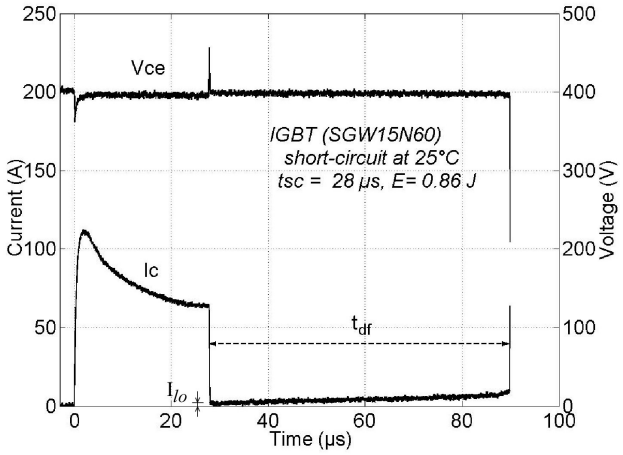

Fig. 8. Delayed failure mode and definition of delay time to failure (t_{df}) and initial leakage current (I_{lo}).

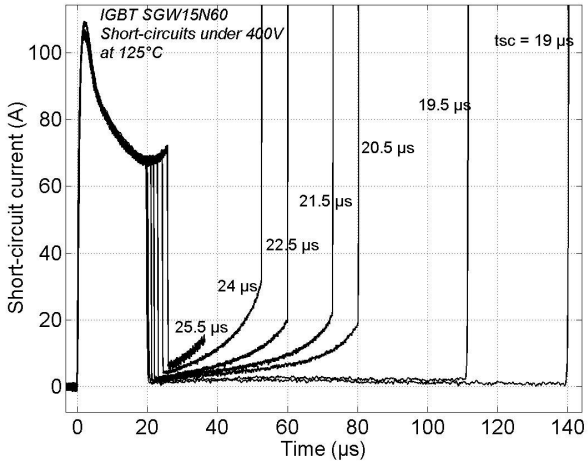

Fig. 9. Experimental short-circuit current waveforms for 600V NPT IGBT under 400V at 125^oC and for different short-circuit durations (t_{SC}).

corresponds to the failure shown in Fig.7. Otsuki et al. [**?**] have shown that this curve is rather linear. But for their measurements, the short-circuit energy variations were done with different short-circuit currents by varying the gate bias, dc bus voltage and short-circuit duration. Now, we have shown that critical energy depends on the test conditions.

D. Energies $E = E_C$

In case of short-circuit energy equal to the critical value, the number of tests that the device is able to withstand before failure is randomly distributed, between 1 and about 10^4 (Figs. 3, 4 and 5). This singular value of energy makes the failure mode unstable for the devices. Indeed, it is very difficult to insure rigorously the same short-circuit

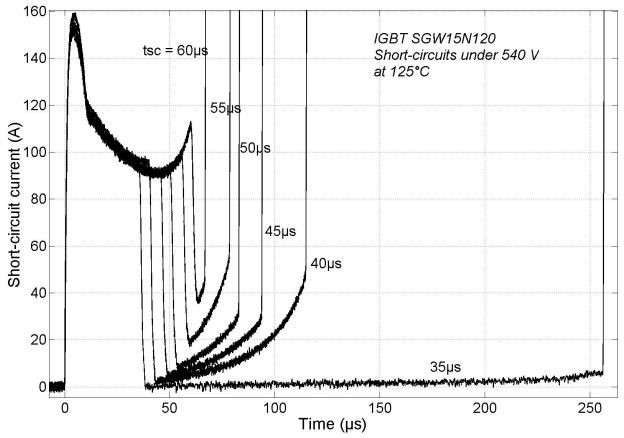

Fig. 10. Experimental short-circuit current waveforms for 1200V NPT IGBT under 540V at 125^oC and for different short-circuit durations (t_{SC}).

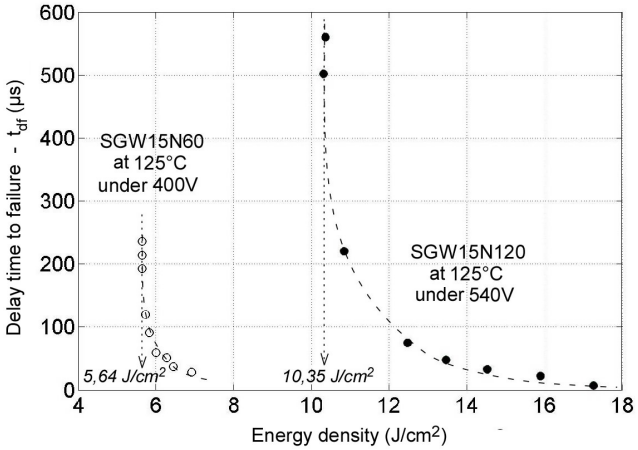

Fig. 11. Dependance of delay time to failure vs. short-circuit energy density.

energy during all the repetitive short-circuits tests. This is without consequence for $E > E_C$ or $E < E_C$ where the failure modes are stables, but the unstability occurs for $E = E_C$. In this case, the device should withstand repetitive short-circuits and the failure mode should be given by the ageing effect after some 10^4 test cycles (Fig.6). But, during this repetitive tests, if, the short-circuit energy of the last cycle is imperceptibly higher than the previous one (due to a low increase in the voltage supply for example), then the ”delayed” failure mode occurs at this last cycle (as shown in Fig.8). So, it is always in this last mode that failures occur for the tests results given at $E = E_C$ in figures 3, 4 and 5.

For the failures occurred in this particular test conditions ($E = E_C$), the delay times to failure (t_{df}) are the highest possible and the initial tail currents (I_{lo}) are very low.

E. Ageing indicators

Two 600 V NPT IGBT were regularly characterized during the repetition of the short-circuit operations and electrical parameters were measured in order to find ageing indicators. Figure 12 shows for example the results of on-state (V_{ON}) and threshold (V_{TH}) voltages and measurements evolution during the repetition of the short-circuit tests. Only one among the two devices shows a slight variation of V_{TH} the other one has no significant variation. Further measurements must correlate these results. On the other hand, no significant variation of the gate and collector leakage currents have been found. These results apply for all the tested IGBTs. So, actually, it is difficult to foresee the IGBT end of life.

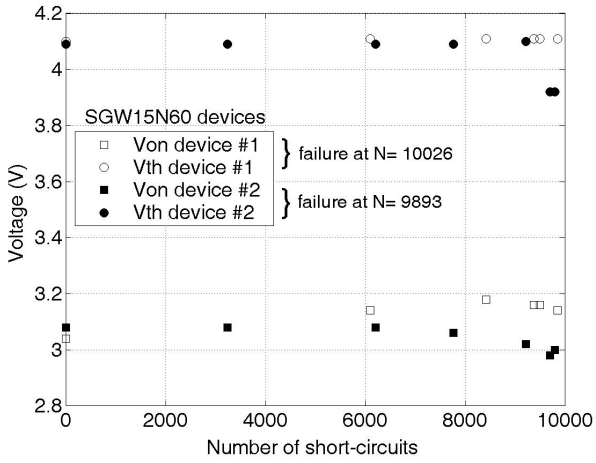

Fig. 12. On-State and threshold voltages measurements during the repetition of the short-circuit operations for two tested IGBTs (SGW15N60).

Only ageing on COOLMOS^{TM} transistors have been detected. For these devices, the short-circuit waveforms regularly stored during the repetitive short-circuit tests show a significant decrease of the short-circuit current before the failure appears like shown on Fig.13.

This result is correlated with the on-state voltage evolution shown in Fig.14. This parameter is a good ageing indicator for this particular device.

The dissipated energy deceases during the repetition of the short-circuits with a fixed short-circuit time. For this reason, the dissipated energy indicated in Fig.5 is the initial dissipated energy. The other electrical characteristics regularly measured are not varying during the tests.

IV. Discussion

Fig.15 is an enlarged view of figure 10 with an additional current waveform for $t_{SC} = 33\mu s$ leading to no delayed failure mode ($E < E_C$). When observing the short-circuit current waveforms, it can be seen that it decreases from the peak value because of the mobility reduction in the MOSFET channel due to temperature rise. Then, after the current has reached a minimum value, it rises again until it is turned-off as shown in Fig.15 or the device fails as in

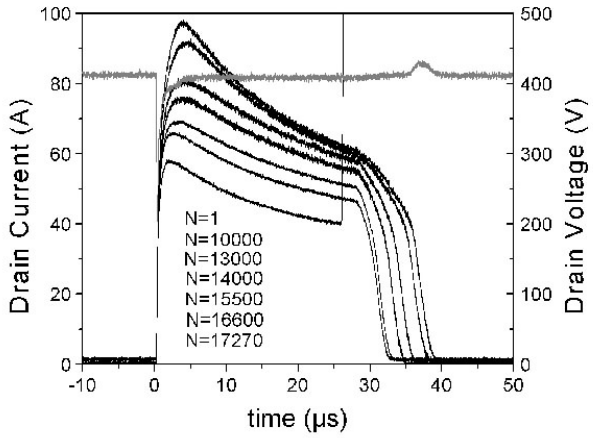

Fig. 13. Drain current evolution of the tested CoolMOS during successive short-circuit operations ($T_C = 125^oC, U_{DC} = 405V, E_{SCINI} = 1.05J$).

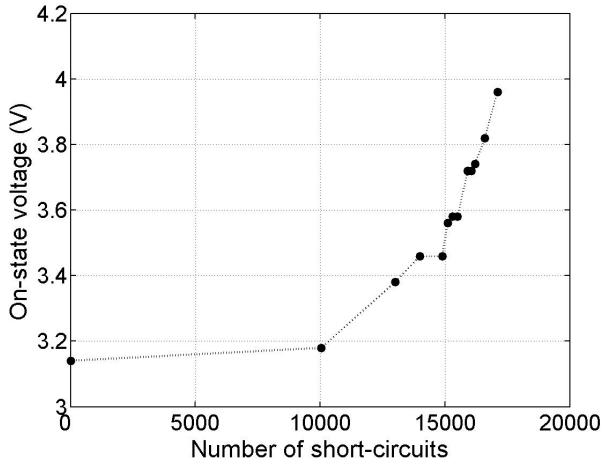

Fig. 14. Increase of the on-state resistance for COOLMOS transistors (measured at $T_C = 25^oC, I_D = 20A$) during short-circuit repetitions (at $T_C = 125^oC, U_{DC} = 405V, E_{SCINI} = 1.05J$)

Fig.7. The reduction of the decrease and then the rise of the current is due to the additional current component due to the leakage current which is generated by the temperature rise. The initial leakage current value (I_{lo}) at turn-off time is given, for each short-circuit test, by dots resulting in the extrapolation of the tail current at the considered time (t_{SC}) as visible in figure 15 for $t_{SC} = 60\mu s$ and $55\mu s$. Then, the dotted curve, in this figure, gives the value of the leakage current, flowing trough the device and which must be added to the short-circuit current, at any time during the short-circuit process.

If the device is turned-off sufficiently before the short-circuit current has reached the minimum value ($t_{SC} = 33\mu s$), it seems that no significant leakage current flows and no delayed failure will occur. So, only a cumulative

damaging mechanism will lead to failure as it is the case for $E < E_C$. If the device is turned-off while a significant leakage current is flowing (from $t_{SC} = 35\mu s$), thermal runaway will occurs leading to the delayed failure mode.

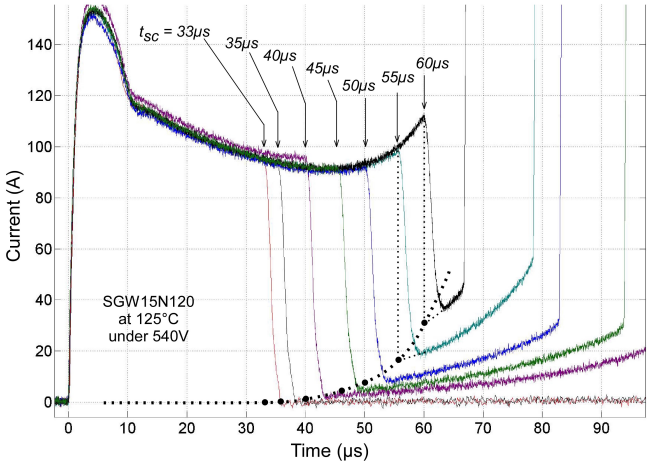

Fig. 15. Experimental short-circuit current waveforms for SGW15N120 for different short-circuit durations (t_{SC}) and estimation of the leakage current.

In order to estimate the temperature distribution within the device during short-circuit operations, and especially at the end of the short-circuit process shown in Fig.15, a simplified 1D thermal model has been developed and described below.

A. Thermal Model

As already mentioned, we have used single chip devices in TO247 package where silicon die is attached to the case by a solder material. The die width (W_{Si}) and the solder layer width (W_{Sld}) are visible in the schematic model shown in Fig.16.

The 1D approximation is justified because the thermal flow essentially occurs in one dimension and can affect the silicon chip and possibly the underneath solder layer if the heat transfer is long enough. During the short-circuit operations, the chip can reach very high temperature values and the temperature dependence of the thermal conductivity and heat capacity of silicon must be taken into account in the thermal model whereas constant thermal properties are kept for the solder layer. This last assumption is justified by a relatively lower temperature variation than silicon. The classical heat equation is solved over the thermal system composed by silicon die and the solder layer :

$$\frac{\partial}{\partial x}\left(\lambda(T)\frac{\partial T}{\partial x}\right) + Q(x,t) = \rho\, c(T)\, \frac{\partial T}{\partial t} \tag{1}$$

where $T(x)$ is the temperature distribution along the x axis, ρ, λ and c are respectively material density, local thermal conductivity and thermal capacity. $Q(x,t)$ is the heat generation source due to the power dissipation responsible for the thermal increase in the silicon chip. For silicon region, the density is constant $\rho_{Si} = 2320 Kg.m^{-3}$

whereas thermal conductivity and capacity are temperature dependent and given in appendix. Concerning the solder region, we used the following parameters $\rho_{Sld} = 7400\ Kg.m^{-3}$, $\lambda_{Sld} = 50\ W.m^{-1}.K^{-1}$ and $c_{Sld} = 190\ J.Kg^{-1}.K^{-1}$ [**?**]. The chip depth, active area and total area, given in table I, have been obtained from the device datasheets [**?**] for SGW15N120 devices.

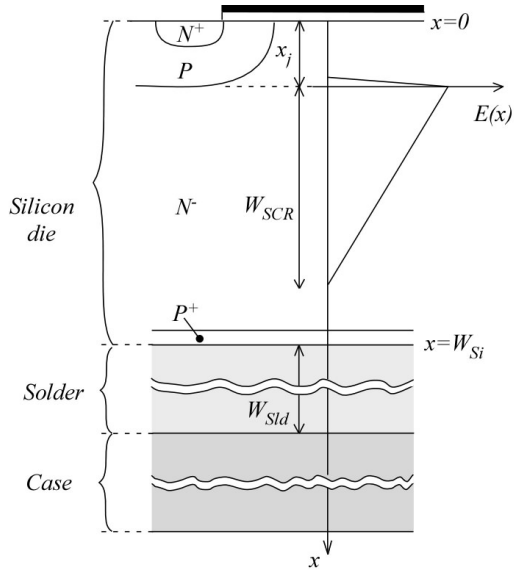

Fig. 16. Thermal model.

TABLE II

GIVEN DATASHEET PARAMETERS [?].

Parameter	SGW15N120
W_{si} (μm)	180
Die active area (mm^2)	18.7
Die total area (mm^2)	25.9

The heat source is $Q(x,t) = E(x,t) \cdot J(t)$, where $E(x,t)$ is the electric field distribution in the space charge region (voltage dependant) and $J(t)$ is the time dependent current density, given by experimental measurements. In spite of high current densities during short circuit operations, we suppose that the electric field distribution is not perturbed by the carrier flows. This assumption, verified in the literature by 2D physical simulations [**?**], assumes that holes and electrons flows are quite equal during the short-circuit operation. Unfortunately, we had no information concerning the internal structure data parameters, junction depth and N-base impurity concentration. Nevertheless, the blocking voltage of the NPT devices allows us to estimate in one hand x_j at about $15\mu m$ and on

the other hand base doping (N_D) at about $10^{14}\,cm^{-3}$ for the SGW15N120.

The heat equation (1) is completed with initial and boundary conditions. The heat flux is assumed to flow from the heated device to the thermal heat-sink and thus we assume that no heat transfer occurs through the top surface of the silicon die. In addition, the case temperature of the device is assumed to be isothermal at T_c during the short-circuit process. These conditions may be written as follows :

$$\lambda_{Si}\left(\frac{\partial T}{\partial x}\right)_{x=0} = 0 \tag{2}$$

$$T(x = W_{Si} + W_{Sld}, t) = T_c \tag{3}$$

$$T(x, t = 0) = T_c \tag{4}$$

Then the heat equation is solved by using the finite difference method.

B. Simulation Results

Fig.17 gives the temperatures at the junction location (T_j at $x = x_j$) for the short-circuit operations shown in Fig.15 applied to the SGW15N120 devices. The case temperature is 125^{o}C. It can be seen that for a short-circuit duration of 33 μs, which corresponds to the critical energy value (1.95 J), the junction temperature is about 640^{o}C. Whereas for t_{SC} = 60 μs, corresponding to a high short-circuit energy value (Fig.15), this temperature (T_j) rises until 960^{o}C.

For each experimental short-circuit cases of figure 15, Table I gives the calculated junction temperature (T_j) as visible in Fig.17 as well as the measured initial leakage current (I_{lo}) at the turn-off time. The dependance of I_{lo} with temperature may be approximated by the dependance with the intrinsic carrier concentration ni. So, ratios I_{lo}/n_i and I_{lo}/n_i^2 for each experimental case have been plotted in figure 18. Results show that the leakage current varies with n_i^2 rather than n_i. As a result, the dominating component of leakage current seems to be the diffusion component rather than the thermal generation component.

V. CONCLUSION

This paper has presented experimental results on the behavior of 600V and 1200V NPT IGBT and 600V COOLMOS^{TM} transistors under repetitive short-circuit operations. All the tested devices have shown the same behavior regarding their robustness against repetitive short-circuit tests. A critical value of short-circuit energy (E_C) has been found which separates two distinct stable failure modes. For energy below the critical value, devices can withstand a large number of short-circuits before failure with a cumulative damaging mechanism and a destruction phenomenon which looks like dynamic latch-up. When the short-circuit energy is higher but close to E_C, devices fails at the first short-circuit test in a ”delayed failure mode”. A tail current takes place after the turn-off process of the device and leads to a destructive thermal runaway phenomenon after several hundreds of microseconds. The

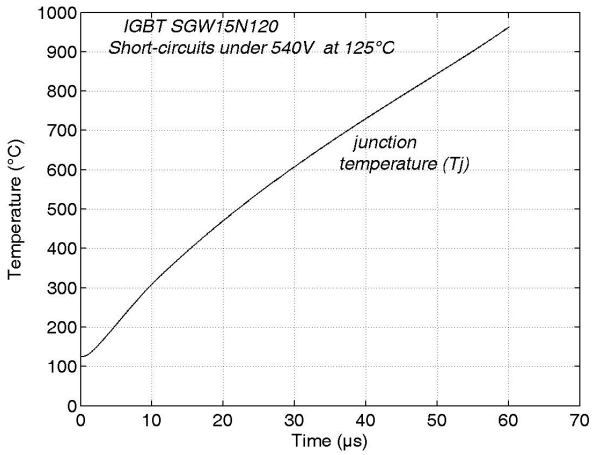

Fig. 17. Calculated junction temperature for the short-circuit conditions of Fig.15.

TABLE III

MEASURED INITIAL LEAKAGE CURRENT AND ESTIMATED JUNCTION TEMPERATURE FOR THE SHORT-CIRCUIT CONDITIONS OF FIG.15.

$t_{SC}(\mu s)$	$T_j(^oC)$	$I_{lo}(A)$
35	670	0.7
40	730	2
45	790	5
50	845	8
55	900	19
60	960	35

significance of this critical energy value (E_C) is related to the reach of high enough temperature values inside the device leading to a significant leakage current. It has been found that the leakage current is dominated by diffusion component rather than thermal generation. The classical short-circuit ”energy limited” failure mode has been found to be a limit case of the ”delayed failure mode” with a delay time to failure equal to zero. As prospectives, more analysis are under investigations such as detailed electro-thermal numerical simulation of the ”delayed failure mode” behavior and the chip physical analysis.

APPENDIX I

The temperature dependence of thermal conductivity $\lambda_{Si}(T)$ and capacity $c_{Si}(T)$ of the silicon are given below [?].

$$\lambda_{Si}(T) = \frac{1}{a + bT + cT^2} \qquad (W.m^{-1}.K^{-1}) \tag{5}$$

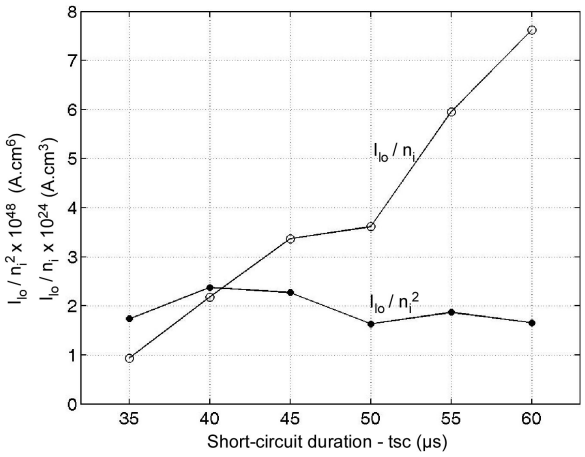

Fig. 18. Leakage current (I_{lo}) dependance with intrinsic carrier concentration (n_i) and short-circuit duration (t_{SC}).

with $a = 3 \times 10^{-4}\ m.K.W^{-1}$, $b = 1.56 \times 10^{-5}\ m.W^{-1}$ and $c = 1.65 \times 10^{-8}\ m.K^{-1}.W^{-1}$.

$$c_{Si}(T) = a + bT + \frac{c}{T^2} \qquad (J.Kg^{-1}.K^{-1}) \tag{6}$$

with $a = 8.49 \times 10^2\ J.Kg^{-1}.K^{-1}$, $b = 0.155\ J.Kg^{-1}.K^{-2}$ and $c = -1.6 \times 10^7\ J.Kg^{-1}.K$.

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Stephane Lefebvre received his Ph.D. degree in Electrical Engineering from the Ecole Normale Superieure de Cachan, France, in 1994. He is currently working in the Power Electronics and Integration team of the SATIE (UMR CNRS 8029).

Since 2000, he has been a senior lecturer at the Conservatoire National des Arts et Metiers (CNAM), Paris, France, where he teaches Power Electronics. He his currently interested in the behavior of power semiconductor in hard working conditions and at high operating temperature.

Zoubir Khatir received the Dipl. Ing. degree in physics of solids in 1984 from INSA Toulouse, France, and the Ph.D. degree in electronics in 1988, prepared in the LAAS-CNRS laboratory, Toulouse, France.

From 1988 he joined the Laboratory of New Technology (LTN) of the French National Institute of Transport and Safety Research (INRETS) where he was in charge for high power semiconductor devices modelling and CAD tools development. His actual interests are the thermal fatigue of high power electronic modules and their thermal management in the field of transport applications.

Frederic Saint-Eve received his degree of Electrical and Mecanical Engineer at ENSEM Nancy (France) in 1998 and his Ph.D. degree in Electrical Engineering from the Ecole Normale Superieure de Cachan (France) in 2004. He is currently working in the Power Electronics and Integration team of the Laboratory SATIE, and his research interests include semiconductor reliability and power electronics.