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Normally-off Diamond Reverse Blocking MESFET

J. Cañas§, A. C. Pakpour-Tabrizi§, T. Trajkovic, F. Udrea, D. Eon, E. Gheeraert and R. B. Jackman*

Abstract*—Schottky contacts have been used to fabricate normally-off lateral reverse-blocking MESFETs on p-type (boron doped) O-terminated monocrystalline diamond. The devices utilized an ohmic source contact but both gate and drain contacts were Schottky in nature. Boron-doped p-channel diamond MESFETs reported to-date display the less-attractive normally-on characteristics. Here, the normally-off transistor delivered a current level of ~1.5 μAmm^{-1} at a negative V_{GS} of 0.8V and a transconductance (g_m) of 16 μSmm^{-1}, measured at room temperature; at a temperature of 425 K with these values rose to ~70 μAmm^{-1} for I_{DS} and a g_m value of 260 μSmm^{-1}. In both cases a negligible gate leakage current was measured with no breakdown apparent at the maximum field investigated here ($3.7x10^5$ V/m^{-1}). The Schottky gate demonstrates a well-behaved control of the channel even at higher temperatures. The high temperature operation, normally-off behavior and diamond's inherent radiation hardness make this transistor promising for harsh environment applications.

***Index Terms*—Diamond, MESFET, Molybdenum, Schottky**

I. Introduction

DIAMOND transistors are promising for high temperature, power and frequency applications in harsh environments, including those with high radiation levels. This is due to the unique properties of diamond as a wide band-gap (5.5eV) semiconductor. The majority of Diamond field-effect transistors (FETs) fabricated to-date use a 2D hole gas that emerges when an H-terminated diamond surface comes into contact with a range of adsorbates and/or selected metal oxides [1-8]. However, this unconventional manner of creating a p-type region in a semiconductor suffers from instability and reproducibility problems [9] and low operational mobility issues [10-11], although recent progress with the use of metal-oxide passivation/gate structures have considerably reduced these problems. For example, Kawarada and co-workers have demonstrated both impressive power characteristics [12] and normally-off performance using careful device design with surface-transfer doping [13]. None-the-less, device fabrication strategies that rely upon a conventional doping approach must also be explored; both to ensure optimized compatibility for ultimate device integration with existing technology along, with the full realization of the potential for operation in harsh environments. The primary alternative is to use diamond bulk conduction with a conventional dopant to fabricate transistors. The most reliable dopant, boron, displays relatively deep acceptor state levels (~0.37eV at conventional doping concentrations), which causes only partial ionization at room temperature [14]. Despite this limitation, by using bulk conduction, surface stability problems can be easily solved by using insulating O-terminations [15]. The breakdown voltage

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will likely be improved due to the higher band gap present when surface band bending is not present and the on-current limitation caused by boron's acceptor state level can be resolved using higher temperatures, reaching its maximum at around 550K [16]. Additionally, the radiation resistance of bulk transistors is arguably better than surface FET's due to the low stability of the H-Diamond interface, it being vulnerable to increased C-H bond breaking under various radiation sources [17,18].

Several lateral O-terminated diamond FET concepts and architectures have been recently fabricated [19]–[22] while for vertical FETs, traditionally favored for high power devices, fabrication is still challenging despite the recent efforts of the diamond device community. The reported lateral devices display 'normally-on' characteristics, which are not ideal for high power applications. Further, reported breakdown voltages are typically poor in comparison to diamond's full potential mainly due to limitations in substrate and epilayer quality alongside existing processing capabilities [23].

In this work, these problems are addressed. A novel and a *normally-off* lateral Schottky-drain (SD) MESFET based on molybdenum Schottky contacts on O-terminated boron doped diamond has been fabricated. While the source of the device is ohmic, both drain and gate electrodes are Schottky. Having a Schottky drain aims to make the reverse blocking capability of the MESFET improve by the formation of a depletion region around the contact, effectively suppressing the leakage current [24]. Here, this type of device is referred to as a reverse-blocking (RB) FET.

Normally-off FET operation is usually required to ensure full control of device operation and robust performance in transient modes of operation when devices are most vulnerable. In general, MESFET transistors are normally-on. The dopant level and thickness of the channel typically grown mean that an unbiased Schottky gate contact leads to a depletion layer thickness which is insufficient to close the channel, i.e., the structure is conducting. In operation, the Schottky gate is reverse biased to extend the depletion region across the channel, turning the device off. This is conventionally circumvented to produce a normally-off MESFET device by fine tuning the channel thickness under the gate using gate recess technology. This can result in full closure of the depletion region under the channel. A small forward bias is then required to reduce the channel depletion under the gate and turn the device on. Such precise control has been lacking in current diamond technology; here the precise conditions for normally-off operation are achieved by direct low-doping level and thickness control of the p-diamond layer on top of the n-type diamond substrate.

However, this forward gate bias needed for an on-condition creates a challenge in terms of the gate-to-drain leakage current level which is especially acute for power applications. A further design refinement is implemented here to reduce this problem; the use a Schottky drain. This Schottky drain leads to improvements in gate to drain breakdown voltage, since a Schottky diode drain prevents minority carrier injection in the active layer. Further, the current in the drain region should be more uniform as compared to that of a standard ohmic drain. [25].

Thus, the major challenge in the fabrication of such a normally-off MESFET is thus to deliver the correct layer thickness with precise doping. Based on knowledge acquired by previous work with molybdenum Schottky contacts on p-type diamond [26]–[28], the space charge region thickness has been estimated for both the Schottky gate and back p-n junction between the p-drift layer and the n-type substrate, ideally to offer a normally-off channel. However, the requirements for the control of doping and layer thickness are demanding; progress in the precise control of epitaxial growth of lightly boron doped diamond layers on single crystal substrates in the author's laboratories has now allowed the fabrication of the device structures with the required precise control of doping and p-layer thickness. Normally-off devices with encouraging characteristics have been fabricated and measurement results are reported here.

II. DEVICE DESIGN AND EXPERIMENTAL METHODS

The devices fabricated here use a High-Pressure High Temperature (HPHT) synthesized type-Ib type monocrystalline (100) oriented diamond substrate (4mmx4mm) substrate. The presence of nitrogen impurities in this material, where nitrogen forms a deep substitutional donor state at ~1.7eV makes the material weakly n-type [29]; this creates device isolation from parasitic capacitance effects through the presence of a p-n junction between the substrate and the p-type active device regions. Epitaxial growth of a lightly boron doped diamond layer, is followed by the patterned growth of a heavily boron doped diamond layer. The former is used to establish a Schottky-type contact, whilst the latter facilitates ohmic contact fabrication. The resulting device structure is shown schematically in figures. 1 (a) and 1 (b). The schematic in fig. 1 (a) shows operation as a lateral diode-like structure (source to drain) when $V_{GS} < V_{TH}$, where V_{TH} is the threshold voltage for the onset of depletion under the gate. The condition $V_{GS} > V_{TH}$ is represented schematically in fig. 1 (b), where the expected short channel region of the transistor in operation is also represented.

In practical terms, a 500nm thick and $3x10^{16}cm^{-3}$ boron doped epilayer was grown using Microwave Plasma Enhanced Chemical Vapour Deposition (MWPECVD) (B_2H_6/H_2 60ppm, CH_4/H_2 2%, O_2/H_2 0.5%, 1150K) on the HPHT substrate. It was essential to carefully control the diborane gas flow and the condition of the growth chamber, in terms of boron-usage in

previous experiments, to achieve low-B doping levels. A 400nm thick titanium hard mask was patterned by photolithography and e-beam evaporation in order to define the heavily boron doped regions ($5x10^{20}$ cm^{-3}), selectively grown by MWPECVD (B_2H_6/H_2 0.2%, CH_4/H_2 8%, 1150K) for ohmic contact formation. The source ohmic contact was then fabricated with a Ti/Pt/Au stack, the sample being then annealed for 30 minutes at 500°C under vacuum. A 300°C, low pressure ozone treatment was then applied to the exposed diamond surface creating adsorbed oxygen moieties. These act to pin the surface Fermi level stopping any surface conductivity effects [30] and hence maximizing the Schottky barrier at the metal-semiconductor interface. A lift-off photolithography process was used to pattern sputtered molybdenum for definition of the Schottky drain and gate contacts. A Corbino (circular-like) type structure, which does not require device isolation, was utilized. This is shown in figure 1(c) where an optical micrograph of an array of fabricated devices can be seen, along with a schematic indicating the ohmic source region along with the Schottky gate and drain metallization. The device shown in figure 1(c), has a gate to source distance of L_{GS}=8μm and a drain to source distance of L_{DS}= 68 μm while the drain perimeter is L_{DW}=615 μm and the gate perimeter is L_{GW}=2500 μm.

The DC current-voltage (I-V) characteristics were measured using a Keithley 2612B source-ammeter. Small-signal measurements [C(V), C(f), impedance, and admittance] were performed with a constant AC voltage of V_{AC} = 50 mV by a Solartron Modulab impedance analyser. Temperature was controlled using a Linkam LNP 95 controller and measured using a PT100 resistance thermometer inside the sample holder. All measurements were performed under dynamic vacuum at 10^{-4} mbar. Capacitance characteristics presented represent the measured capacitance of the equipment which is $C_m = 1 / 2\pi fZ$, where Z is the modulus of the measured impedance. To perform the conductance method, the parallel capacitance-conductance circuit ($C_p - R_p$) can be evaluated by using the real part and imaginary part of the measured impedance. Interface trap densities were extracted using the conductance method, details of which will be provided in section III.

III. RESULTS

A. Transfer Characteristics at RT

In figure 2, room temperature measurements of the drain current I_{DS} are shown for V_{DS} = -25V to V_{DS} = +25V, with the gate voltage ranging from V_{GS} = 0V to -1.2V.

For V_{GS} = 0V no drain current is observed, hence the transistor is normally OFF; the threshold voltage (V_{TH}) is thus V_{TH}=0 V as current starts flowing at higher negative values of V_{GS}. The upper level of the gate voltage is limited to -1.2V because the gate-source Schottky region becomes conductive leading to excessive I_{GS}. While the transistor is off at V_{GS}=0, it reaches ~1.5 μA mm^{-1} at V_{GS} = -0.8V and V_{DS}=-25 V. The leakage current under reverse bias conditions is less than the detection limit of the system (pA). Due to its RB nature, the transistor characteristics are described by the thermionic emission of the Schottky drain with a gate and drain modulated channel resistance. The turn-on voltage for the Schottky drain is V_{DS} = -0.8V. From this voltage, the current increases are limited by thermionic emission until the channel (variable) resistance becomes relevant and, at greater V_{DS}, dominant. Due to the normally-off character of the transistor with V_{TH}=0V, the pinch-off voltage (V_p) must be equal to the Schottky contacts built-in voltage V_p=1.72V (see subsection C). Therefore, the channel is pinched-off for the V_D values where I_D starts to be also limited by the channel resistance.

The drain current, in the μA/mm range is modest, but this is to be expected given the activation energy of ~0.37eV for boron acceptor states at the doping level present in the channel. Indeed, at the room temperature measurements reported in figure 2 less than 1% of the boron acceptor states will be activated and contributing to conduction [31].

This successful implementation of a normally-off regime RB-MESFET here was obtained by combining the top depletion region induced by the Schottky gate contact with the back depletion region induced by the p-n junction between the lightly n-type substrate and the p-type channel. The thickness and the doping level of the epilayer were carefully chosen such that the channel would be fully depleted in the off condition. A further design criterion was that a channel would be opened with a small threshold voltage, advantageous for device operation.

The effective transconductance in the saturation regime is calculated as 16 μS/mm for V_{GS} = -1V. This value is similar to the value obtained by Umezawa et al. [19] for a normally-on diamond MESFET, with an effective measured room temperature transconductance of 10 to 18 μS/mm depending on L_{DG} distance, and with those of Liu et al. [5,7].

B. Transistor Transfer Characteristics at higher Temperatures

As noted above the boron dopant atoms become activated as acceptor states with an energy of ~0.37eV. Thus, to improve the device output performance, measurements at higher temperatures have been made. The drain current I_{DS} has been measured in the range 300K to 425K, again for V_{DS} = -25V to V_{DS} = +25V, with a fixed gate voltage of V_{GS} = -0.8V. This data is plotted in figure 3. Once again FET I-V curves can be understood as lateral Schottky diodes with gate and drain

modulated channel resistance. At elevated temperatures, increased diamond conductivity and earlier drain turn-on voltages are recorded due to carriers thermal ionization and increased thermionic emission, respectively. The devices remain normally-off in character, with no measurable leakage current up to 425K in reverse bias. Whereas at V_{GS} = - 0.8V at room temperature an I_{DS} of around 1.5 μA/mm was observed, the same V_{GS} value now yields an I_{DS} of ~70μA/mm at 425K. The maximum transconductance in the saturation regime at this temperature is 260 μSmm^{-1}. This is a high value for this normally-OFF device with band conduction; for example, even for a normally-ON MESFET, Umezawa and co-workers [21] reported a significantly lower transconductance of 61μSmm^{-1} at 573K. This is attributed to the superior doping level used in this work's sample while the value of the Schottky barrier for the molybdenum gate used here (see below), and the molybdenum contact stability at high temperatures contribute to this success. For comparison, a significantly higher transconductance value of 11.6 mS/mm at V_{GS} of −12 V has been reported for a normally-OFF H-terminated device [13]. This form of device with surface-transfer doping, whereby surface diamond electrons accumulate in the (adsorbate or metal oxide covered) C-H layer leads to a 2D-like p-layer in the diamond surface which is inevitably easier to deplete than a channel region comprising a fraction of a micron of p-type material. However, reproducibility, long term stability and propensity to thermal degradation issues hamper the application of devices using surface-transfer doping. The full effect of temperature on the transconductance measured here for the normally-off RB-MESFET at V_{DS}=-10V and for V_{GS} between -0.8V and 0V is shown in figure 4; the transconductance at V_{GS} =-0.8V changes from 16µS/mm at RT to 260µS/mm at 425K.

The improvement in the current level when higher temperatures are used is primarily due to the ionization of boron acceptor impurities in the p-layer and the reduced compensation effect; the boron impurity level is rather deep (0.37eV) and not fully ionized at RT, as mentioned above. This increase in the on-current can be explained by the semi-empirical mobility model [16] plus the carrier density increase at higher temperatures. The operation at high temperature shows the potential for boron-doped diamond bulk conduction while the gate control over the channel remains stable. This fact shows the significant advantage of working with a bulk-type conduction for high temperature operation versus H-terminated diamond (surface-transfer doping) FETs, which typically display thermal instability.

C. Molybdenum Schottky Gate Characteristics

The molybdenum Schottky gate used here allows the control of the channel conductivity in the device by depletion of channel carriers. The gate-source I-V and 1/C^2-V (at 1kHz) characteristics of the Schottky gate are shown in figure 5, measured at 425K. The 1/C^2 curve is expected to show a linear behavior in the depletion region of the C-V curve described by:

$$C^{-2} = \frac{2}{q\varepsilon S^2 N_D}\,(V + V_{BI}) \qquad (1)$$

Where q is the electron charge, ε the dielectric constant, S the depletion surface area, N_D the donor concentration and V_{bi} the built-in voltage of the Schottky contact [32].

At 0V the channel is completely depleted under the gate and as +V_{GS} increases further depletion happens laterally from around the gate perimeter. As V_{GS} becomes increasingly negative, lateral expansion is absent and the vertical depletion, directly under the Schottky contact represents the entirety of the space-charge-region (SCR), itself diminishing with increasing -V_{GS}. In the 1/C^2 (Mott-Schottky) plot (fig. 5(a)), both lateral and vertical depletion capacitance regions under the gate can be distinguished and are fitted with dashed lines. Taking a linear fit for the capacitance over the first (laterally dominated) region considering the gate perimeter and channel thickness, a doping level of 4x10^{16} cm^{-3} can be deduced. In the range of voltages lower than 0V, from ~ -0.4 to -0.9 V, the vertical depletion regime in which the SCR expands directly under the Schottky gate is distinguished (the second dotted region). Here, a linear fit shows a free carrier density of ~1x10^{16} cm^{-3} from the slope and a V_{Bi} = 1.72V is deduced from the intercept with the x-axis. For this doping level, the distance from the Fermi level to the valence band of diamond is E_F - E_{VB} = 0.29 eV. The Schottky barrier height deduced from the built-in voltage is thus 2.01 V. In figure 5(b) the Schottky gate I-V characteristics are shown at RT, 350K and 400K. The Schottky gate shows no measurable leakage current at positive bias, while the current at negative bias starts increasing above -0.75V, reaching -10nA (~10% of the on-channel current) at -1.2V. The Schottky barrier height and ideality factor extracted from the measured data is also represented in the figure. This suggests the Schottky barrier grows from 1.02 at RT to 1.2 at 400K while the ideality factor decreases from 1.67 at RT to 1.28 at 400K

If an n-type carrier density of ~10^{19} cm^{-3} for the (N-doped) substrate is assumed [29], a 300nm SCR can be estimated for the p-n junction that forms between the channel epilayer and the substrate. From the extracted value of V_{BI}, a Schottky SCR of ~200 nm is estimated at 0V. Therefore, as the Schottky SCR joins the p-n SCR at approximately 0V a total p-type layer thickness of 500 nm is extracted. This calculation can only be an estimate since the actual carrier concentration in the n-type substrate at the temperatures concerned is unknown, given the E_a for substitutional N of ~1.7eV and an unknown level of defect-induced compensation. However, the high difference in doping level between drift layer and substrate makes this depletion region rather independent of small variations to the substrate doping and compensation levels.

The disparity between the barrier height derived from

capacitance and current measurements is attributed to inhomogeneities over the interfacial region; the capacitance extraction tends to give an averaged value while the current extraction will be influenced by regions which display a lower barrier. These are likely attributable to local inhomogeneities of the interface chemical bonding configuration between O-terminated diamond and molybdenum. The ideality factor of 1.67 may arise due to the formation of an ultra-thin insulating layer between diamond and molybdenum. However, here this relatively high ideality factor can be an advantage for the Schottky gate, as it allows the V_{GS} values to be high (up to -1.2V) toward the Schottky ON-state, effectively retracting the space charge region under the gate and opening the channel without having a high value of I_{GS}.

The electrical properties of interface states are characterized by their density, their position in the energy gap, and their capture cross section. Measurements of the equivalent parallel conductance are capable of giving more detailed information about interface states than capacitance measurements [30]. In capacitance measurements the interface state capacitance must be extracted from the measured capacitance which consists of oxide capacitance, depletion layer capacitance, and interface state capacitance. This difficulty does not apply to the equivalent parallel conductance because conductance arises solely from the steady-state loss due to the capture and emission of carriers by interface states and is, thus, a more direct measure of these properties. Carrier density can respond to an applied signal frequency by diffusion from the bulk to the interface and by recombination-generation processes through interface states and states in the diamond space charge region. However, these processes are typically too slow to allow the minority carrier density to follow high frequency measurements; in this case interface state loss is solely responsible for the measured equivalent parallel conductance. The so-called 'conductance method' has proved highly effective at extracting trap densities at interfaces even in 2D systems [34].

The capture cross sections of the traps and the interface trap time constant τ_{it} can be extracted using this approach. The technique for the conductance method relies on measuring the equivalent parallel capacitance as a function of bias voltage and frequency. The conductance gives an idea of the interface trap density as it fluctuates with the capture and emission of carriers by the traps at the interface between the channel and the dielectric. In figure 6(a), the parallel conductance over frequency (G_P/ω in f) for different gate voltages, V_{GS}, are plotted versus frequency for the gate Schottky diode, as its high value of ideality factor was attributed to the formation of a thin oxide layer and can be thus analyzed as a MIS diode. The G_P/ω peak positions can be seen to be voltage dependent. [35].

Conductance is calculated from the interface insulating layer capacitance and the DC conductance to obtain the parallel conductance of the interface states [36]. The C_{int} value is extracted from the maximum capacitance at high frequency (here, $5x10^4$ Hz) [37], as at this high frequency the interface states have insufficient time to follow the AC signal.

The carrier energy loss in the transfer between diamond valence band and interface states following the AC signal are minimized when the signal frequency fits the reciprocal time constant of interface states. From the equivalent conductance, the continuum interface states density can be calculated as:

$$\frac{G_p}{\omega} = \frac{qD_{it}}{2\omega\tau_{it}} ln(1 + (\omega\tau_{it})^2) \qquad (3)$$

Where D_{it} is the interface states density and τ_{it} the interface states time constant [31].

Fitting $\frac{G_p}{\omega}$ using equation (3) for each V_{GS} the density of states can be estimated over a small region of diamond bandgap, as plotted in figure 6(b). Assumptions have been made of a dielectric constant of $\varepsilon = 2$ and a thickness of 0.5 nm for the interfacial oxidized layer at the molybdenum/p-diamond interface. Within this energy range within the band gap, an essentially continuous density of interface states are shown in the figure 4(c), with values of $\sim 2.5x10^{13} eV^{-1}cm^{-2}$ is found. These values are in a similar range to those previously reported for molybdenum-Diamond Schottky contacts [27].

IV. CONCLUDING REMARKS

Normally-off lateral reverse-blocking (Schottky Drain) MESFETs based on molybdenum Schottky contacts on O-terminated boron doped diamond have been fabricated. Precise control over epilayer thickness and doping level have been achieved such that full depletion of the channel arises without an applied gate bias. The devices display undetectable leakage current and a current of ~1.5 μA/mm in the on state at RT. Higher temperature characterization (425K) reveals augmented transistor capabilities due to fuller ionization of the boron dopant atoms, with the transistor reaching a current level of 70μA/mm and a transconductance of 260 μS mm^{-1}. Importantly leakage currents remain immeasurably low.

Further improvements in device performance will require reduction in the interface state trap density which, measured here at ~ $2x10^{13} eV^{-1}cm^{-2}$ are comparatively high. Surface defects in the epilayer forming the channel prior to metallization and partial oxidation/contamination at the metal-epilayer interface following metallization may both be responsible and warrant further study. In addition, the introduction of field plates to the design may beneficially affect the field profile in the Schottky contact regions to enhance device performance.

The high temperature operation capabilities, normally-off

behavior and diamond's inherent radiation hardness as a semiconductor, make these devices an excellent approach towards the goal of achieving diamond transistors for high temperature and harsh environment applications.

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REFERENCES

[1] Y.F. Wang, W. Wang, X. Chang, H.N. Abbasi, X. Zhang, R. Wang and H.X. Wang, "Performance of hydrogen-terminated diamond MOSFET with bilayer dielectrics of YSZ/Al_2O_3," *Diam. Relat. Mater.,* vol. 99, p. 107532, 2019.

[2] C.J. Zhou, J.J. Wang, J.C. Guo, C. Yu, Z.Z. He, Q.B. Liu, X.D. Gao, S.J. Cai and Z.H. Feng, "Radiofrequency performance of hydrogenated diamond MOSFETs with alumina," *Appl. Phys. Lett.,* vol. 114, no. 6, 2019.

[3] J. Liu, M. Liao, M. Imura, A. Tanaka, H. Iwai, and Y. Koide, "Low on-resistance diamond field effect transistor with high-k ZrO2 as dielectric," *Sci. Rep.,* vol. 4, no. 1, p. 6395, 2015.

[4] Z. Rena, D. Lva, J. Xua, K. Sua, J. Zhang, D. Wang, Y. Wu, J. Zhang, Y. Hao, "Performance of H-diamond MOSFETs with high temperature ALD grown HfO 2 dielectric," *Diam. Relat. Mater.,* vol. 106, no. March, p. 107846, 2020.

[5] J. Liu, T. Teraji, B. Da, H. Ohsato, and Y. Koide, "Effect of Annealing Temperature on Performances of Boron-Doped Diamond Metal-Semiconductor Field-Effect Transistors," *IEEE Trans. Electron Devices*, vol. 67, no. 4, pp. 1680–1685, 2020.

[6] J. Liu, H. Ohsato, B. Da, and Y. Koide, "High current output hydrogenated diamond triple-gate MOSFETs," *IEEE Trans. Electron Devices*, vol. 7, no. May, pp. 561–565, 2019.

[7] J. Liu, T. Teraji, B. Da, and Y. Koide, "High Output Current Boron-Doped Diamond Metal-Semiconductor Field-Effect Transistors," *IEEE Electron Device Lett.,* vol. 40, no. 11, pp. 1748–1751, 2019.

[8] Y. Sasama, K. Komatsu, S. Moriyama, M. Imura, T. Teraji, K. Watanabe, T. Taniguchi, T. Uchihashi and Y. Takahide, "High-mobility diamond field effect transistor with a monocrystalline h-BN gate dielectric," *APL Mater.,* vol. 6, no. 11, 2018.

[9] C. Verona, M. Benetti , D. Cannatà , W. Ciccognani , S. Colangeli , F. Di Pietrantonio, E. Limiti , M. Marinelli, and G. Verona-Rinati, "Stability of H-Terminated Diamond MOSFETs With V_2O_5/Al_2O_3 as Gate Insulator," *IEEE Electron Device Lett.,* vol. 40, no. 5, pp. 765–768, 2019.

[10] G. Daligou and J. Pernot, "2D hole gas mobility at diamond/insulator interface," *Appl. Phys. Lett.,* vol. 116, no. 16, p. 162105, 2020.

[11] Y. Sasama, T. Kageura, K. Komatsu, S. Moriyama, J. Inoue, M. Imura, K. Watanabe, T. Taniguchi, T. Uchihashi, and Y. Takahide, "Charge-carrier mobility in hydrogen-terminated diamond field-effect transistors" *J. Appl. Phys.,* vol. 127, p.185707, 2020.

[12] H. Kawarada, T. Yamada, D. Xu, Y. Kitabayashi, M. Shibata, D. Matsumura, M. Kobayashi, T. Saito, T. Kudo, M. Inaba, A. Hiraiwa, "Diamond MOSFETs using 2D Hole Gas with 1700V Breakdown Voltage", *28th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, 2016. DOI: 10.1109/ISPSD.2016.7520883

[13] Y. Kitabayashi T. Kudo, H. Tsuboi, T. Yamada, D. Xu, M. Shibata, D. Matsumura, Y. Hayashi, M. Syamsul, M. Inaba and H. Kawarada, "Normally-Off C–H Diamond MOSFETs With Partial C–O Channel Achieving 2-kV Breakdown Voltage," *IEEE Electron Device Letters*, vol. 38, no. 3, p. 363, 2017

[14] K. Thonke, "The boron acceptor in diamond," *Semicond. Sci. Technol.,* vol. 18, no. 3, 2003.

[15] J. Navas, D. Araujo, J.C. Pinero, A. Sanchez-Coronilla, E. Blanco, P. Villar, R. Alcantara, J. Montserrat, M. Florentin, D. Eon and J. Pernot, "Oxygen termination of homoepitaxial diamond surface by ozone and chemical methods: An experimental and theoretical perspective," *Appl. Surf. Sci.,* vol. 433, p. 408, 2018.

[16] P-N. Volpe, J. Pernot, P. Muret, and F. Omnès, "High hole mobility in boron doped diamond for power device applications". *Appl. Phys. Letts.,* vol. 94, p. 92, 2009.

[17] H. Umezawa, S. Ohmagari, Y. Mokuno and J. H. Kaneko, "Characterization of X-ray radiation hardness of diamond Schottky barrier diode and metal-semiconductor field-effect transistor," *29th International Symposium on Power Semiconductor Devices and IC's (ISPSD),* 2017, p. 379, doi: 10.23919/ISPSD.2017.7988983.

[18] Ilya Obodovskiy, Chapter 16 - Chemical Processes Under the Influence of Radiation, Editor(s): Ilya Obodovskiy, *Radiation*, Elsevier, 2019, p. 247-255, ISBN 9780444639790

[19] C. Masante, J. Pernot, J. Letellier, D. Eon, and N. Rouger, "175V, > 5.4 MV/cm, 50 mΩ.cm2 at 250°C Diamond MOSFET and its reverse conduction," *Proc. Int. Symp. Power Semicond. Devices ICs*, vol. 2019-May, pp. 151–154, 2019.

[20] T. T. Pham, N. Rouger, C. Masante, G. Chicot, F. Udrea, D. Eon, E. Gheeraert and J. Pernot, "Deep depletion concept

for diamond MOSFET," *Appl. Phys. Lett.,* vol. 111, no. 17, 2017.
[21] H. Umezawa, T. Matsumoto, and S. I. Shikata, "Diamond metal-semiconductor field-effect transistor with breakdown voltage over 1.5 kV," *IEEE Electron Device Lett.,* vol. 35, no. 11, pp. 1112–1114, 2014.
[22] N. Donato, N. Rouger, J. Pernot, G Longobardi and F. Udrea, "Diamond power devices: State of the art, modelling and figures of merit," *J. Phys. D: Appl. Phys.,* vol. 53, p. 093001, 2020
[23] P-N. Volpe, P. Muret, J. Pernot, F. Omnes, T. Teraji, F. Jomard, D. Planson, P. Brosselard, N. Dheilly, B. Vergne and S. Scharnholtz, "High breakdown voltage Schottky diodes synthesized on p-type CVD diamond layer", *Physica Status Solidi (a)* vol 207, no. 9, p. 2088, 2010.
[24] W. Mao, W-B. She, C. Yang, J-F. Zhang, X-F. Zheng, C. Wang and Y. Hao, "Reverse blocking characteristics and mechanisms in Schottky-drain AlGaN/GaN HEMT with a drain field plate and floating field plates" *Chinese Phys. B,* Vol. 25, p. 017303, 2016.
[25] D. Meignant and D. Boccon-Gibod, "Schottky drain microwave GaAs field effect transistors", *Elec. Letts.,* vol. 3, p.17, 1981.
[26] H. Umezawa, S. I. Shikata, and T. Funaki, "Diamond Schottky barrier diode for high-temperature, high-power, and fast switching applications," *Jpn. J. Appl. Phys.*, vol. 53, no. 5 p. 6, 2014.
[27] A. Nawawi, K. J. Tseng, G. A. J. Amaratunga, H. Umezawa, and S. Shikata, "Characterization of vertical Mo / diamond Schottky barrier diode from non-ideal I – V and C – V measurements based on MIS model," *Diam. Relat. Mater.,* vol. 35, p. 1, 2013.
[28] H. Umezawa, T. Saito, N. Tokuda, M. Ogura, S. Ri, and H. Yoshikawa, "Leakage current analysis of diamond Schottky barrier diode," *Appl. Phys. Letts.,* vol. 90, p. 073506, 2007.
[29] R.G. Farrer, "On the substitutional nitrogen donor in diamond", *Sol. Stat. Comms.,* vol. 7 p. 685, 1969.
[30] S-G. Ri, D. Takeuchi, H. Kato, M. Ogura, T. Makino, S. Yamasaki, and H. Okushi, "Surface conductive layers on oxidized (111) diamonds", *Appl. Phys. Letts.*, vol. 87, p. 262107, 2005
[31] T. H. Borst and O. Weiss, "Boron-Doped Homoepitaxial Diamond Layers: Fabrication, Characterization, and Electronic Applications", *Phys. Sta. Sol. (a),* vol. 154, no. 1, p. 423, 1996.
[32] S.M. Sze and K.K. Ng, "Physics of Semiconductors", 3rd Edn., J. Wiley and sons, 2007, ISBN-10: 0-471-14323-5
[33] E. H. Nicollian and A. Goetzberger, "The Si-SiO_2 interface – electrical properties as determined by the metal-insulator-silicon conductance technique," *Bell System Technical Journal*, vol. 46, no. 6, p. 1055, 1967
[34] D. Dev, A. Krishnaprasad, H. Kalita, S. Das, V. Rodriguez, J.C. Flores, L. Zhai and T. Roy, "High quality gate dielectric/MoS_2 interfaces probed by the conductance method", *Appl. Phys. Letts.,* vol. 112, p. 232101, 2018.
[35] R. Engel-Herbert, Y. Hwang, and S. Stemmer, "Comparison of methods to quantify interface trap densities at dielectric/III-V semiconductor interfaces", *J. Appl. Phys.,* vol. 108, no. 12, p. 124101, 2010.
[36] T. T. Pham, A. Maréchal, P. Muret, D. Eon, E. Gheeraert, N. Rouger, and J. Pernot. "Comprehensive electrical analysis of metal/ Al_2O_3/O-terminated diamond capacitance", *J. Appl. Phys.,* vol. 123, p. 161523, 2018.
[37] E. Vincent, G. Ghibaudo, G. Morin, and C. Papadas, "On the oxide thickness extraction in deep-submicron technologies", *IEEE Int. Conf. Microelectron. Test Struct.,* vol. 10, p. 105, 1997.

FIGURE CAPTIONS [ORGINALS OF FIGURES SUPPLIED SEPERATELY]

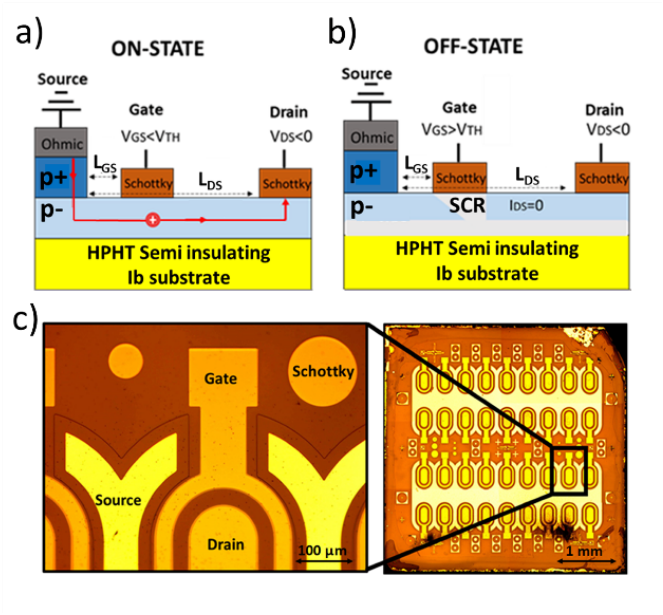


Fig. 1. a) Device scheme of the on-state operation. The current is only able to flow from source to drain under negative V_{DS} due to the diode behavior of the Schottky drain.
b) Device scheme of the off-state operation. The off-state is reached by the depletion of the channel underneath the gate under positive V_{GS}.
c) Device picture showing the ohmic source over the p+ diamond layer and the molybdenum Schottky Drain, Gate and test structure on the left. On the right, a full picture of the sample.

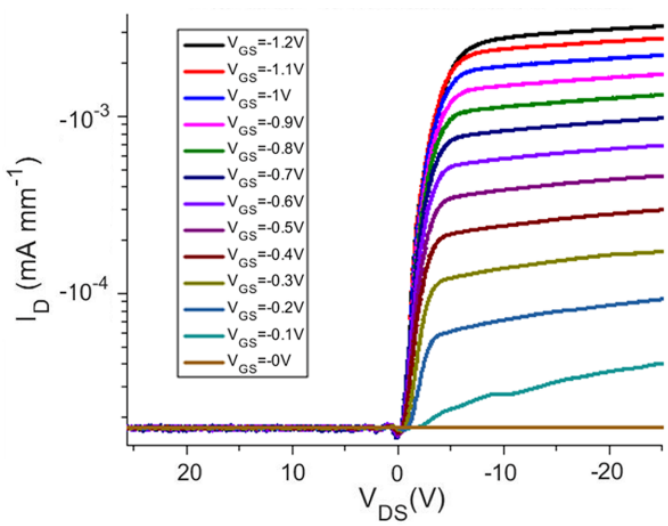


Fig. 2. Room temperature transfer characteristics of the normally-off RBMESFET at different gate voltages. The transistor is off at V_{GS}=0 and reaches ~1.5 µA mm^{-1} at V_{DS}=-25 V and V_{GS}=-0.8 V. No leakage current is observed in reverse.

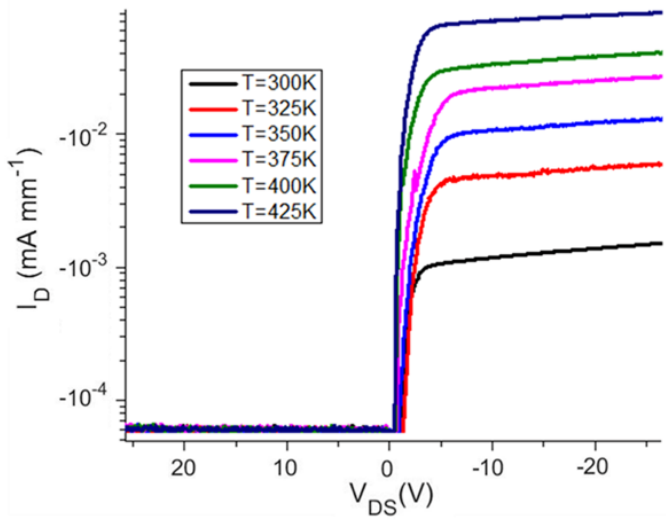


Fig. 3. Transfer characteristics of the normally-OFF RB-MESFET at V_{GS}=-0.8V versus temperature. No leakage current is observed in reverse BIAS. The current at 425K is increased by a factor ~50 compared to RT, reaching 70 μA mm^{-1} at -25V.

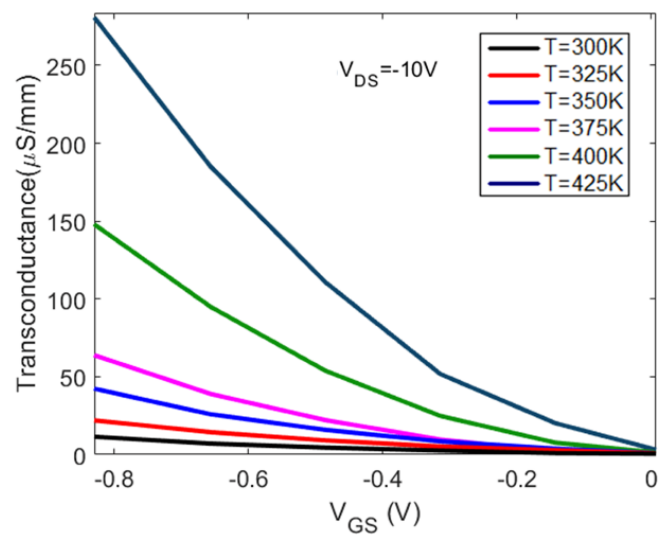
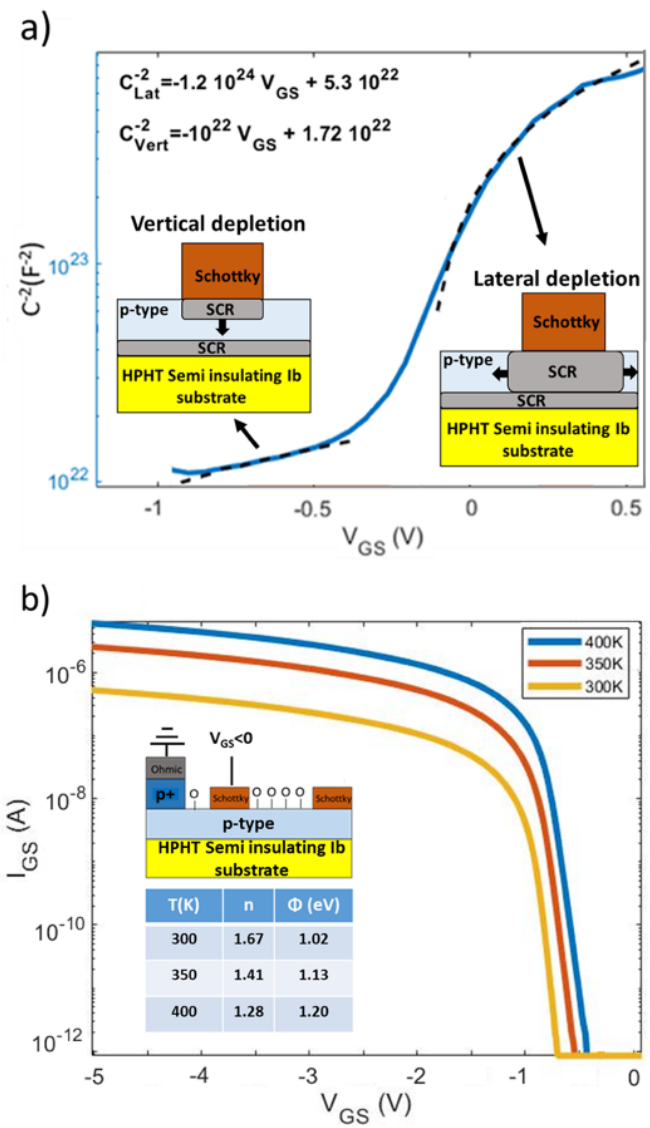


Fig. 4. Normally-off RB-MESFET transconductance at V_{DS}=-10V for V_{GS} between -0.8V and 0V and temperatures between RT and 425K. The transconductance at V_{GS} =-0.8V scales from 16µS/mm at RT to 260µS/mm at 425K.



T(K)	n	Φ (eV)
300	1.67	1.02
350	1.41	1.13
400	1.28	1.20

Fig. 5. a) Schottky Mott Plot for the capacitance data extracted from measurements performed on the molybdenum Schottky gate. Lateral and vertical depletion capacitance under the gate are fitted with dashed line. N_A extracted from the slope of the $1/C^2$ plot and is 10^{16} cm^{-3} for the vertical depletion region and 4 10^{16} cm^{-3} for the lateral. From the intercept with the x axis a V_{BI}= 1.72V is extracted.
b) Schottky Gate I-V characteristics at RT, 350K and 400K. The Schottky barrier height and ideality factor extracted from the measured data is also represented in the figure. The Schottky barrier grows from 1.02 at RT to 1.2 at 400K while the ideality factor decreases from 1.67 at RT to 1.28 at 400K.

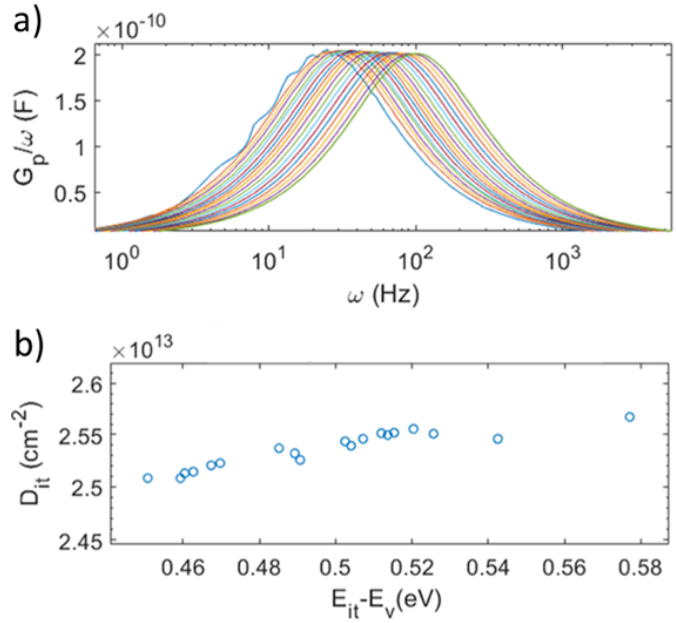


Fig. 6.
a) The parallel conductance over the frequency versus the frequency for different gate to source voltages are represented for the Schottky Gate.
b) The extracted density of continuum interface states using conductance method assuming a dielectric constant of ε=2 and a thickness of 0.5nm for the interfacial oxidized layer.